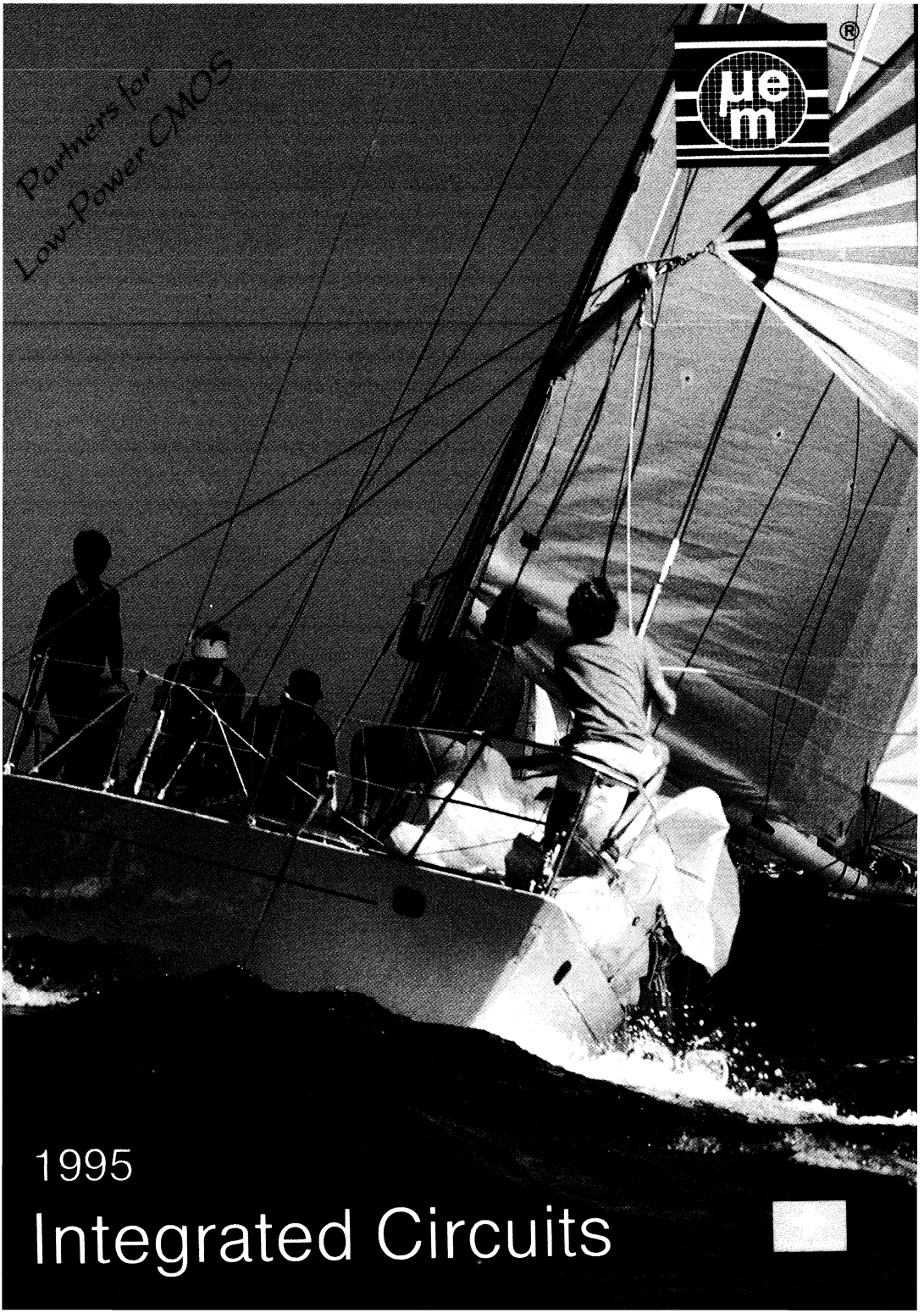

1995

Integrated Circuits

EM Microelectronic-Marin SA

A Company of SMH

EM Microelectronic-Marin S.A.'s production and design facilities in Marin / Neuchâtel

History

Microelectronic-Marin was founded in 1975 as a division of the Swiss Ebauches Electronics S.A., which was a member of the ASUAG group of companies. It was the first major step this large Swiss watch manufacturing group took into the world of sophisticated microelectronics. Almost 10 years later this group merged with the SSIH group to form the new SMH, the largest Swiss group of companies manufacturing watches and microelectronics.

At the same time, the Microelectronic-Marin division was formed into an independent company, EM Microelectronic-Marin SA. With strong financial backing from this large industrial group, it has successfully developed into a leading position and is now considered one of the world's leading low-power, low-voltage CMOS manufacturers, 100% financed by Swiss capital. Investing enormous effort into research and development as well as into the continuous up-dating of production methods and equipment, EM has reached a high technological standard in low-power, low-voltage CMOS technology, which has been the key to the success of its products. Considering that integrated circuits have not only innovated watches and computers, but also dominate machine controls, industrial robots, medical, measuring, and chemical instrumentation, as well as processing controls, telecommunications, toys, and entertainment products, it has been a logical step forward for EM to increasingly expand its semiconductor activities from watch ICs into the field of industrial circuits. EM is striving to become a major supplier in the field of user-specific, customized and standard low-power, low-voltage CMOS circuits for the electronics industry, putting its design capabilities and its specific advanced technologies to good use.

However, being one of the world's leading manufacturers of watch circuits, with a world market share of over 20% in analog watch ICs, EM will also continue to grow in this, its traditional, market.

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Important Notice

EM Microelectronic-Marin SA cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an EM Microelectronic-Marin SA product. EM Microelectronic-Marin SA reserves the right to change the circuitry and specifications without notice at any time. You are strongly urged to ensure that the information given has not been superseded by a more up-to-date version.

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EM MICROELECTRONIC-MARIN SA

Une société de SMH

QUALITY POLICY

BY TOTAL COMMITMENT WE WILL IMPROVE TOWARDS THE HIGHEST QUALITY FOR PRODUCTS AND PROVIDE SERVICES THAT MEET OR EXCEED THE REQUIREMENTS OF OUR CUSTOMERS AND THE STANDARDS OF OUR COMPETITION.

The mission shall be accomplished within the framework of five underlying principles for continued emphasis on quality that shall guide company objectives, plans and activities.

1. Our aim is the total satisfaction of our customers' needs.
2. Management fixes the goals and supports the actions of quality improvement.
3. Quality is everyone's job.
4. Our goal is "zero defects".
5. We do it right the first time.

Quality & Reliability Manager | Marketing & Sales Manager | Design V.P.

Front End Operations Manager | Back End Operations V.P. | Administration V.P.

President & General Manager

Rev. B / 26.11.90

Display Driver

EM Type	Features	Applications	Supply Voltage	Typ. current Consumption	Package
M 6003 01	• **Static LCD Driver,** any layout • 1-bit interface • 32 segments • On-chip oscillator	Automotive displays Utility meters Balances Battery powered products	$3 \leq V_{DD} \leq 15$ V	1.5 μA at 5 V	DIP40 PLCC44
M 6004 02	• **Static LCD Driver,** any layout • 1-bit interface • 40 segments • Crossfree cascadable	Automotive displays Utility meters Balances Battery powered products	V_{DD}: 5 V ± 10% $5 \leq V_{LCD} \leq 12$ V	10 μA max. at 5 V	PLCC52
V 6118 8	• **Multiplex LCD Driver,** any layout • 1-bit interface • 8-way max. (8 rows, 32 columns) • Standby current: typ. 100 nA at 5 V • Crossfree cascadable • Independent LCD supply voltage • Waveforms generated on chip, no external components required • Display refresh on chip, 8 x 40 RAM for display storage • Column driver only mode • LCD updating synchronized to the LCD refresh signal • BLANK function	Automotive displays Utility meters Balances Pagers	$2 \leq V_{DD} \leq 6$ V $2 \leq V_{LCD} \leq 7$ V	100 μA at 7 V	QFP52 TAB
4	Same as V6118 8 except: • 4-way mux (4 rows, 36 columns) • 4 x 40 RAM for display storage				QFP52 TAB
2	Same as V6118 8 except: • 2-way mux (2 rows, 38 columns) • 2 x 40 RAM for display storage				QFP52 TAB

Real Time Clock

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumption	Package
M 3002	• **RTC, 4-bit** interface • 32 kHz quartz oscillator • Clock: counts from seconds to 99 years • Alarm: counts from seconds to 31 days • Timer: counts from seconds to 24 hours • Low current consumption: typ. 5 μA at 3 V • Access time 150 ns typical • Battery pin	POS terminals Telecom systems Control systems Data loggers	$2.4 \leq$ Bat. ≤ 5.0 V $2.4 \leq V_{DD} \leq 5.5$ V	6 μA at 5 V 5 μA at 3 V	DIP 16 SO16
M 3003	• **RTC, 4-bit** interface • 32 kHz quartz oscillator • Clock: counts from seconds to 99 years • Alarm: counts from seconds to 31 days • Timer: counts from seconds to 24 hours • Low current consumption: typ. 5 μA at 3 V • Access time 150 ns typical • Power fail connection	POS terminals Telecom systems Control systems Data loggers	$2 \leq V_{DD} \leq 5.5$ V	12 μA at 5 V 5 μA at 3 V	DIP16 SO16
V 3021	• **RTC, 1-bit** interface • 32 kHz quartz oscillator • Very low current consumption: typ. 800 nA at 3 V • Max. 60 ns access time • No busy states • Clock: counts from seconds to 99 years • No external capacitor required	White/Brown goods Pay phones POS terminals Hand-held systems	$2 \leq V_{DD} \leq 5.5$ V	800 nA at 3 V 1.3 μA at 5.5 V	DIP8 SO8
V 3022	• **RTC, 8-bit** interface • Built-in 32 kHz crystal with digital trimming and temperature compensation facilities • Sleep mode current consumption: typ. 1.2 μA at 3 V • Max. 60 ns access time • Universal interface compatible with both Intel and Motorola • No busy states • Power fail input • BUS can be tri-state when $\overline{PF}$ active • 12 or 24 hours data formats • Time to 1/100 of a second • Programmable interrupts • Alarm programmable up to one month	Industrial controllers Alarm systems PABX and telecom systems Hand-held systems Data loggers	$2 \leq V_{DD} \leq 5.5$ V	1.2 μA at 3 V 2 μA at 5.5 V	DIP18 SO28

Real Time Clock

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumption	Package
V 3023	• **RTC, 8-bit** interface • Built-in 32 kHz crystal with digital trimming and temperature compensation facilities • 16 bytes of user RAM • Can be synchronized to 50 Hz or nearest sec./min. • Sleep mode current consumption: typ. 1.2 μA at 3 V • Max. 60 ns access time • Universal interface compatible with both Intel and Motorola • No busy states • Power fail input • BUS can be tri-state when $\overline{PF}$ active • 12 or 24 hours data formats • Time to 1/100 of a second • Programmable interrupts • Alarm programmable up to one month	Industrial controllers Alarm systems PABX and telecom systems Hand-held systems Data loggers	$2 \leq V_{DD} \leq 5.5$ V	1.2 μA at 3 V 2 μA at 5.5 V	DIP18 SO28

Watch

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumption	Package
H 1063	• 32 kHz quartz oscillator • Digital trimming • Low current consumption: typ. 800 nA • Low output impedance for bipolar stepping motor • Programmable alarm functions	Analog clocks	$1.1 \leq V_{DD} \leq 1.8$ V	2 μA max. at 1.8 V	CHIP
H 1137	• 32 kHz quartz oscillator • High oscillator stability • Very low current consumption: typ. 250 nA • Low output impedance for bipolar stepping motor • Programmable motor period and motor pulse width	Analog watches	$1.2 \leq V_{DD} \leq 1.8$ V	350 nA max. at 1.55 V	CHIP
H 1127	Mirror version of the H 1137				
H 1344	• 32 kHz quartz oscillator • Low current consumption: typ. 700 nA • Low output impedance for bipolar stepping motor • Programmable alarm functions	Analog clocks	$1.1 \leq V_{DD} \leq 1.8$ V	2 μA max. at 1.8 V	CHIP DIP8
H 5050	• 4,19 MHz quartz oscillator • LCD BIAS voltages: - adjustable via E^2PROM - with temperature compensation • 12 or 24 hour display mode • High electromagnetic immunity	Digital car clocks	$3 \leq V_{DD} \leq 6$ V	700 μA at $V_{DD} = 5$ V	SO28
1H	1 Hz auto-increment				
2H	2 Hz auto-increment				
4H	4 Hz auto-increment				

Watchdog

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
H 6006 **A2** **A3** **B1** **B2** **B3**	• Low voltage alarm prior to reset • Automatic reset initialized on power-up • Remains in reset after timeout - Fail safe • Outputs guaranteed down to V_{DD} = 1.5V • Standard timeout period (10 ms) or externally programmable Monitored Voltage Thresholds (V) • Open drain outputs 2.25, 2.00, 1.75 at V_{DD} = 5 V 2.00, 1.95, 1.90 independent from V_{DD} • Push-pull outputs 9.00, 8.00, 7.00 at V_{DD} = 5 V 2.25, 2.00, 1.75 at V_{DD} = 5 V 2.00, 1.95, 1.90 independent from V_{DD}	POS terminals Automotive electronics White goods	$1.5 \leq V_{DD} \leq 5.5$ V	50 μA at 5 V	DIP8 SO8
H 6060 **14** **16** **15**	• Low voltage alarm prior to reset • Automatic reset initialized on power-up • Self-recovering reset after timeout • Outputs guaranteed down to V_{DD} = 1.6V • Standard timeout period (100 ms) or externally programmable Monitored Voltage Thresholds (V) • Push-pull outputs 2.25, 2.00, 1.75 at V_{DD} = 5 V 2.00, 1.95, 1.90 independent from V_{DD} • Open drain outputs 2.00, 1.95, 1.90 independent from V_{DD}	POS terminals Automotive electronics White goods	$1.6 \leq V_{DD} \leq 5.5$ V	80 μA at 5 V	DIP8 SO8
H 6061 **25**	• Low voltage alarm prior to reset • Automatic reset initialized on power-up • Self-recovering reset after timeout • Outputs guaranteed down to V_{DD} = 1.6V • Standard timeout period (100 ms) or externally programmable Monitored Voltage Thresholds (V) • Open drain outputs 1.54, 1.50, 1.46 independent from V_{DD}	POS terminals Telephone handsets Modems	$2.7 \leq V_{DD} \leq 5.25$ V	80 μA at 5 V	DIP8 SO8
V 6130	• Voltage and software monitoring • Standby mode: typ. 22 μA at 5 V • Reset output guaranteed down to V_{DD} = 1.2 V • Programmable reset threshold • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatiblity	Industrial electronics Cellular telephones Security systems Battery powered products	$3 \leq V_{DD} \leq 5.5$ V	55 μA at 5.5 V with R_{EXT} = 100 kΩ	DIP8 SO8
V 6133	• Voltage and software monitoring • 3 chip select disable circuits • Standby mode: typ. 22 μA at 5 V • Reset output guaranteed down to V_{DD} = 1.2 V • Programmable reset threshold • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL/CMOS compatibility	Industrial electronics Cellular telephones Security systems Battery powered products	$3 \leq V_{DD} \leq 5.5$ V	55 μA at 5.5 V with R_{EXT} = 100 kΩ	DIP14 SO14

Watchdog

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
V 6150	• Voltage and software monitoring • Standby mode: typ. 23 μA at 5 V • Reset output guaranteed down to V_{DD} = 1.2 V • Programmable reset threshold • Voltage reference accuracy ± 3% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Automotive electronics Cellular telephones Security systems Battery powered products	$3 \leq V_{DD} \leq 5.5$ V	75 μA at 5.5 V with R_{EXT} = 100 kΩ	DIP8 SO8
01	$\overline{EN}$ = push-pull; RES = open drain				
V 6170	• Voltage and software monitoring • Standby mode: typ. 24 μA at 5 V • Reset output guaranteed down to V_{DD} = 1.2 V • Programmable reset low threshold • Voltage window, high threshold 5.9 V • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Industrial electronics Cellular telephones Security systems Battery powered products	$3 \leq V_{DD} \leq 5.5$ V	55 μA at 5.5 V with R_{EXT} = 100 kΩ	DIP8 SO8
V 6173	• Voltage and software monitoring • 3 chip select disable circuits • Standby mode: typ. 24 μA at 5 V • Reset output guaranteed down to V_{DD} = 1.2 V • Programmable reset low threshold • Voltage window, high threshold 5.9 V • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Industrial electronics Cellular telephones Security systems Battery powered products	$3 \leq V_{DD} \leq 5.5$ V	55 μA at 5.5 V with R_{EXT} = 100 kΩ	DIP14 SO14

Smart Reset

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
H 6052	• Clear microprocessor start on power-up • Reset output guaranteed down to $V_{DD} = 1.6$ V • On-chip oscillator • No external components required	Automotive electronics White/Brown goods Industrial systems	$1.6 \leq V_{DD} \leq 5.5$ V	80 μA at 5 V	TO-92 SOT-223
1	Reset output				
2	$\overline{\text{Reset}}$ output				
V 6300	• Clear microprocessor start on power-up • Reset output guaranteed down to $V_{DD} = 1.0$ V • On-chip oscillator, no external components required • Very low current consumption: 3.0 μA at 5 V • Pin-out compatible with DS 1233A	Automotive electronics Industrial electronics Telecom systems Hand-held systems	$1 \leq V_{DD} \leq 8$ V	1.5 μA at 2 V 3.0 μA at 5 V 5.2 μA at 8 V	TO-92 SOT-223
	Monitored Voltage Thresholds • Reset active low, push-pull				
A	2.0 V[1)]				
B	2.4 V[1)]				
C	2.8 V[1)]				
D	3.5 V[1)]				
E	4.0 V[1)]				
F	4.5 V[1)]				
	• Reset active high, push-pull				
G	2.0 V[1)]				
H	2.4 V[1)]				
I	**2.8 V**				
J	3.5 V[1)]				
K	4.0 V[1)]				
L	4.5 V[1)]				
	• Reset active low, open drain				
M	2.0 V[1)]				
N	2.4 V[1)]				
O	**2.8 V**				
P	**3.5 V**				
Q	4.0 V[1)]				
R	4.5 V[1)]				

[1)] Non-stock items, minimum order 30k pieces

Smart Reset

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
V 6310	• Clear microprocessor start on power-up • Reset output guaranteed down to V_{DD} = 1.0 V • On-chip oscillator, no external components required • Very low current consumption: 3.0 µA at 5 V • Pin-out compatible with DS 1233A Monitored Voltage Windows • Reset active low, push-pull **A** 2.0 to 6 V[1)] **B** 2.4 to 6 V[1)] **C** 2.8 to 6 V[1)] **D** 3.5 to 6 V[1)] **E** 4.0 to 6 V[1)] **F** 4.5 to 6 V[1)] • Reset active high, push-pull **G** 2.0 to 6 V[1)] **H** 2.4 to 6 V[1)] **I** 2.8 to 6 V[1)] **J** 3.5 to 6 V[1)] **K** 4.0 to 6 V[1)] **L** 4.5 to 6 V[1)] • Reset active low, open drain **M** 2.0 to 6 V[1)] **N** 2.4 to 6 V[1)] **O** **2.8 to 6 V** **P** 3.5 to 6 V[1)] **Q** 4.0 to 6 V[1)] **R** 4.5 to 6 V[1)]	Automotive electronics Industrial electronics Telecom systems Hand-held systems	$1 \leq V_{DD} \leq 8$ V	1.5 µA at 2 V 3.0 µA at 5 V 5.2 µA at 8 V	TO-92 SOT-223
V 6320	• Clear microprocessor start on power-up • Reset output guaranteed down to V_{DD} = 1.0 V • On-chip oscillator, no external components required • Very low current consumption: 3.0 µA at 5 V • Pin-out compatible with MC 33064 Monitored Voltage Thresholds • Reset active low, push-pull **A** 2.0 V[1)] **B** 2.4 V[1)] **C** 2.8 V[1)] **D** 3.5 V[1)] **E** 4.0 V[1)] **F** 4.5 V[1)] • Reset active high, push-pull **G** 2.0 V[1)] **H** 2.4 V[1)] **I** 2.8 V[1)] **J** 3.5 V[1)] **K** 4.0 V[1)] **L** 4.5 V[1)] • Reset active low, open drain **M** 2.0 V[1)] **N** 2.4 V[1)] **O** 2.8 V[1)] **P** **3.5 V** **Q** 4.0 V[1)] **R** **4.5 V**	Automotive electronics Industrial electronics Telecom systems Hand-held systems	$1 \leq V_{DD} \leq 8$ V	1.5 µA at 2 V 3.0 µA at 5 V 5.2 µA at 8 V	TO-92

[1)] Non-stock items, minimum order 30k pieces

Smart Reset

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
V 6330	• Clear microprocessor start on power-up • Reset output guaranteed down to V_{DD} = 1.0 V • On-chip oscillator, no external components required • Very low current consumption: 3.0 μA at 5 V • Pin-out compatible with MC 33064 Monitored Voltage Windows • Reset active low, push-pull **A** 2.0 to 6 V[1)] **B** 2.4 to 6 V[1)] **C** 2.8 to 6 V[1)] **D** 3.5 to 6 V[1)] **E** 4.0 to 6 V[1)] **F** 4.5 to 6 V[1)] • Reset active high, push-pull **G** 2.0 to 6 V[1)] **H** 2.4 to 6 V[1)] **I** 2.8 to 6 V[1)] **J** 3.5 to 6 V[1)] **K** 4.0 to 6 V[1)] **L** 4.5 to 6 V[1)] • Reset active low, open drain **M** 2.0 to 6 V[1)] **N** 2.4 to 6 V[1)] **O** 2.8 to 6 V[1)] **P** **3.5 to 6 V** **Q** 4.0 to 6 V[1)] **R** 4.5 to 6 V[1)]	Automotive electronics Industrial electronics Telecom systems Hand-held systems	$1 \leq V_{DD} \leq 8$ V	1.5 μA at 2 V 3.0 μA at 5 V 5.2 μA at 8 V	TO-92

[1)] Non-stock items, minimum order 30k pieces

Regulator and Surveillance Functions

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
A 6130	• Voltage and software monitoring • Standby mode: typ. 100 μA • Highly accurate 5 V / 100 mA guaranteed output • Low dropout voltage, typically 250 mV at 100 mA • Unregulated voltage input can withstand −20 V reverse battery and +60 V power transients • Regulated voltage accuracy ± 1% • Current limiting • Reset output guaranteed down to V_{OUTPUT} = 1.2 V • Programmable reset threshold • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Cellular telephones Security systems Battery powered products High efficiency linear power supply	$3.36 \leq V_{INPUT} \leq 26$ V	155 μA at V_{INPUT} = 6 V with R_{EXT} = 100 kΩ	DIP8 SO8
A 6133	• Voltage and software monitoring • 3 chip select disable circuits • Standby mode: typ. 100 μA • Highly accurate 5 V / 100 mA guaranteed output • Low dropout voltage, typically 250 mV at 100 mA • Unregulated voltage input can withstand −20 V reverse battery and +60 V power transients • Regulated voltage accuracy ± 1% • Current limiting • Reset output guaranteed down to V_{OUTPUT} = 1.2 V • Programmable reset threshold • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Cellular telephones Security systems Battery powered products High efficiency linear power supply	$3.36 \leq V_{INPUT} \leq 26$ V	155 μA at V_{INPUT} = 6 V with R_{EXT} = 100 kΩ	DIP14 SO14
V 6139	• Low power digitally programmable voltage regulator, 5 V, 3 V, or 2 V • Supply current 12 μA max. with: V_{IN} = 10 V, V_{OUT} = 5 V, I_L = 50 mA • Low dropout voltage, 4 mV at I_L = 100 μA • Short circuit and thermal protection • Battery fail warning, regulator input tested • $\overline{\text{Reset}}$ guaranteed down to V_{OUT} = 1.5 V • 32 kHz crystal oscillator, high stability • No external capacitor required with crystal	Pagers and cordless telephones Security systems Battery powered products	$2 \leq V_{IN} \leq 10$ V $1.5 \leq V_{OUT} \leq 6$ V	7 μA at 7 V	DIP16 SO16

Regulator and Surveillance Functions

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
A 6150	• Voltage and software monitoring • Standby mode: typ. 100 μA • Highly accurate 5 V / 100 mA guaranteed output • Low dropout voltage, typically 250 mV at 100 mA • Unregulated voltage input can withstand −20 V reverse battery and +60 V power transients • Regulated voltage accuracy ± 1% • Current limiting • Reset output guaranteed down to V_{OUTPUT} = 1.2 V • Programmable reset threshold • Voltage reference accuracy ± 3% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Automotive electronics Cellular telephones Security systems Battery powered products High efficiency linear power supply	$3.36 \leq V_{INPUT} \leq 26$ V	175 μA at V_{INPUT} = 6 V with R_{EXT} = 100 kΩ	DIP8 SO8
A1	$\overline{EN}$ = push-pull; $\overline{RES}$ = open drain				
A 6170	• Voltage and software monitoring • Standby mode: typ. 100 μA • Highly accurate 5 V / 100 mA guaranteed output • Low dropout voltage, typically 250 mV at 100 mA • Unregulated voltage input can withstand −20 V reverse battery and +60 V power transients • Regulated voltage accuracy ± 1% • Current limiting • Reset output guaranteed down to V_{OUTPUT} = 1.2 V • Programmable reset low threshold • Voltage window, high threshold 5.9 V • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Industrial electronics Security systems Telecom systems Hand-held systems High efficiency linear power supply	$3.36 \leq V_{INPUT} \leq 26$ V	155 μA at V_{INPUT} = 6 V with R_{EXT} = 100 kΩ	DIP8 SO8

Regulator and Surveillance Functions

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
A 6173	• Voltage and software monitoring • 3 chip select disable circuits • Standby mode: typ. 100 μA • Highly accurate 5 V / 100 mA guaranteed output • Low dropout voltage, typically 250 mV at 100 mA • Unregulated voltage input can withstand −20 V reverse battery and +60 V power transients • Regulated voltage accuracy ± 1% • Current limiting • Reset output guaranteed down to V_{OUTPUT} = 1.2 V • Programmable reset low threshold • Voltage window, high threshold 5.9 V • Voltage reference accuracy ± 1.5% • Programmable delays for P.O.R. and W.D. windows • Time base accuracy ± 10% (over the full temperature range) • ENABLE function • TTL / CMOS compatibility	Industrial electronics Security systems Telecom systems Hand-held systems High efficiency linear power supply	3.36 ≤ V_{INPUT} ≤ 26 V	155 μA at V_{INPUT} = 6 V with R_{EXT} = 100 kΩ	DIP14 SO14
A 6300	• Voltage monitoring • Low current consumption: typ. 100 μA • Highly accurate 5 V / 100 mA guaranteed output • Low dropout voltage, typically 250 mV at 100 mA • Unregulated voltage input can withstand −20 V reverse battery and +60 V power transients • Regulated voltage accuracy ± 1% • Current limiting • Reset output guaranteed down to V_{DD} = 1.0 V • Clear microprocessor start on power-up • On-chip oscillator, no external components required Monitored Voltage Thresholds • Reset active low, push-pull **AA** 2.0 V[1)] **AB** 2.4 V[1)] **AC** 2.8 V[1)] **AD** 3.5 V[1)] **AE** 4.0 V[1)] • Reset active high, push-pull **AG** 2.0 V[1)] **AH** 2.4 V[1)] **AI** 2.8 V[1)] **AJ** 3.5 V[1)] **AK** 4.0 V[1)] • Reset active low, open drain **AM** 2.0 V[1)] **AN** 2.4 V[1)] **AO** 2.8 V[1)] **AP** **3.5 V** **AQ** **4.0 V**	Automotive electronics Industrial electronics Security systems Telecom systems Hand-held systems High efficiency linear power supply	2.3 ≤ V_{INPUT} ≤ 26 V	100 μA at V_{INPUT} = 6 V	DIP8 SO8

[1)] Non-stock items, minimum order 20k pieces

Interface

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumption	Package
V 6910 [1]	• **DUAL Two Channel Level Shifter** • 4 separated input / output power supplies • 4 inputs (TTL compatible) • 2 Output Enable control • Standby current: typ. 100 nA at $V_{DD} = V_{CC}$ 10 V • Maximum frequency 8 MHz • TTL / CMOS compatibility	Industrial electronics Battery powered products	$1.5 \leq V_{DD} \leq 10$ V $1.5 \leq V_{CC} \leq 10$ V	I_{DD} (1.5 V) = 4 µA and I_{CC} (1.5 V) = 40 µA at 500 kHz on the inputs I_{DD} (10 V) = 40 µA and I_{CC} (10 V) = 1.2 mA at 500 kHz on the inputs	DIP16 SO16
10	Open drain output				
20	Push-pull output				
V 6912 [1]	• **Two Channel Level Shifter** • 2 separated input / output power supplies • 2 inputs (TTL compatible) • Output Enable control • Standby current: typ. 50 nA at $V_{DD} = V_{CC}$ 10 V • Maximum frequency 8 MHz • TTL / CMOS compatibility	Industrial electronics Battery powered products	$1.5 \leq V_{DD} \leq 10$ V $1.5 \leq V_{CC} \leq 10$ V	I_{DD} (1.5 V) = 2 µA and I_{CC} (1.5 V) = 20 µA at 500 kHz on the inputs I_{DD} (10 V) = 20 µA and I_{CC} (10 V) = 600 µA at 500 kHz on the inputs	DIP8 SO8
10	Open drain output				
20	Push-pull output				
V 6915 [1]	• **DUAL Two Channel Level Shifter** • 4 separated input / output power supplies • 4 inputs with Schmitt Trigger • 2 Output Enable control • High noise immunity • Standby current: typ. 100 nA at $V_{DD} = V_{CC}$ 10 V • Maximum frequency 5 MHz • Output CMOS compatiblity	Industrial electronics Battery powered products	$1.5 \leq V_{DD} \leq 10$ V $1.5 \leq V_{CC} \leq 10$ V	I_{DD} (1.5 V) = 4 µA and I_{CC} (1.5 V) = 40 µA at 500 kHz on the inputs I_{DD} (10 V) = 60 µA and I_{CC} (10 V) = 1.2 mA at 500 kHz on the inputs	DIP16 SO16
10	Open drain output				
20	Push-pull output				
V 6917 [1]	• **Two Channel Level Shifter** • 2 separated input / output power supplies • 2 inputs with Schmitt Trigger • Output Enable control • High noise immunity • Standby current: typ. 50 nA at $V_{DD} = V_{CC}$ 10 V • Maximum frequency 5 MHz • Output CMOS compatiblity	Industrial electronics Battery powered products	$1.5 \leq V_{DD} \leq 10$ V $1.5 \leq V_{CC} \leq 10$ V	I_{DD} (1.5 V) = 2 µA and I_{CC} (1.5 V) = 20 µA at 500 kHz on the inputs I_{DD} (10 V) = 30 µA and I_{CC} (10 V) = 600 µA at 500 kHz on the inputs	DIP8 SO8
10	Open drain output				
20	Push-pull output				

[1] Non-stock items, minimum order 50k pieces

Contactless Identification Devices (CID)

EM Type	Features	Applications	Supply Voltage	Typ. Current Consumpt.	Package
H 4001	• **Read-only contactless** identification IC • 64-bit memory array, laser programmable • Full wave rectifier • Voltage limiter • Data transmission by amplitude modulation • Manchester or PSK coding	Industrial transponder Car immobilizer Animal identification Access control	Supplied via electromagnetic field		
H 4003	• **Read-only contactless** identification IC • 64-bit memory array, laser programmable • Full wave rectifier • Voltage limiter • Data transmission by amplitude modulation • Manchester or PSK coding • 170 pF ± 2% resonant C on chip	ISO format contactless identification cards	Supplied via electromagnetic field		
Contactless Button 125 kHz	This contactless button is an application of the H 4001 • Material: mix PUR / mat PVC on both sides • Colour: white • Outside dimensions: 28 mm diam. x 1.5 mm thick • Temperature stability: −35 to +60°C • Electronic characteristics: - EM H 4001, 64 bit read-only integrated circuit - Manchester code - Coil, L = 2 mH ± 3% - Chip capacitor, C = 820 pF ± 5% • Resonance frequency: 125 kHz ±10% • Typical reading distance: 0 to 180 mm depending on reader performance and coil characteristics On request: • Resonant frequency tolerance ± 5% • PSK code	Access control Identification systems			
ISO-Contactless Chipcard 125 kHz	This contactless chip-card is an application of the H 400x • Material: mix PUR / bright PVC on both sides • Colour: white • Physical characteristics: - Dimensions, bending and torsion properties according to ISO norm 7816-1 - Temperature stability: −35 to +50°C • Electronic characteristics: - EM H 400x, 64 bit read-only integrated circuit - Manchester code • Resonant frequency: 125 kHz ±8% • Typical reading distance: 0 to 500 mm depending on reader performance and coil characteristics On request: • Both sides of the card can be printed according to customer requirements • Resonant frequency tolerance ± 3% • PSK code	Access control Identification systems			

EMS Mixed-Mode Arrays

EM Type	Description Features	Applications	Supply Voltage	Gate Complex.	Package
V 83nn [2]	**EMS V8300 Series** is a family of transistor arrays for analog/digital applications, with limited capability in the analog domain. Its internal organization is based on a "Sea-of-Gates" architecture offering a high degree of design flexibility and performance. This series is especially suitable for low-voltage, low-power digital applications. It is aimed to cost-effectively satisfy the digital and mixed-mode circuit requirements of up to 6,000 gate complexity. Mixed analog-digital family • 2μ Double-metal, low-voltage CMOS technology • Low power dissipation • Typical gate delay of 1.6 ns at C = 0.1 pF, 4.5 V, 85°C • Low power quartz oscillator • Fast turn-around time • Low development cost	Industrial control and automation Consumer Medical	$1 \leq V_{DD} \leq 6$ V		DIL8 to DIL64 SO8 to SO32 PLCC20 to PLCC84 QFP44 to QFP128 Chip form and other packages on request
nn [2]					Pads
06				300	24
09				700	36
12				1300	48
16				2600	64
20				4000	80
23				5200	92
26				6800	104
V 84nn [2]	**EMS V8400 Series** is a family of arrays designed to meet mixed analog-digital circuit requirements. In addition to their "Sea-of-Gates" core, a dedicated analog array field is added, consisting of passive elements such as resistors, capacitors, lateral pnp's and long-channel transistors. A fully integrated, low-power amplitude-regulated quartz oscillator and a temperature compensated bandgap voltage reference are available. Due to its specific architecture, the EMS V8400 Series offers an excellent performance in mixed mode applications. Mixed analog-digital family • 2μ Double-metal, low-voltage CMOS technology • Low power dissipation • Typical gate delay of 1.6 ns at C = 0.1 pF, 4.5 V, 85°C • Temperature compensated voltage reference • Low power quartz oscillator • Fast turn-around time • Low development cost	Industrial control and automation Consumer Medical	$1 \leq V_{DD} \leq 6$ V		DIL8 to DIL64 SO8 to SO32 PLCC20 to PLCC84 QFP44 to QFP128 Chip form and other packages on request
nn [2]					Pads
06				190	24
09				590	36
12				1000	48
16				2300	64
20				3400	80
23				4700	92
26				6300	104

[2] n or nn stands for the version

Quality Assurance and Reliability

EQNet

THE EUROPEAN NETWORK FOR QUALITY SYSTEM ASSESSMENT AND CERTIFICATION

This is to state that

EM Microelectronic-Marin SA
CH-2074 Marin-Epagnier
Toute l'entreprise

holds the Quality System Certificate

Reg. No 10388-01

for the standard from the
ISO 9000 / EN 29000
series, and the scope as specified therein

Signed for and on behalf of EQNet member

Swiss Association for
Quality Assurance Certificates (SQS)
The managing director:

DATE
Validity of the certificate:
16.03.1992 to
15.03.1995

EQNet members are:

AENOR *Spain* **AFAQ** *France* **AIB-Vincotte** *Belgium* **BSI QA** *United Kingdom*
CISQ *Italy* **DS** *Denmark* **DQS** *Germany* **ELOT** *Greece* **IPQ** *Portugal* **KEMA** *Netherlands*
NCS *Norway* **NSAI** *Ireland* **ÖQS** *Austria* **SFS** *Finland* **SIS** *Sweden* **SQS** *Switzerland*

The issuing member holds all other EQNet members harmless for any claims arising from the existence of this document

Schweizerische Vereinigung für Qualitätssicherungs-Zertifikate Swiss Association for Quality Assurance Certificates

The SQS hereby certifies that the firm named below is equipped with a Quality System which meets the international Standards of Quality Management and Quality Systems (series ISO 9000/EN 29000).

EM Microelectronic-Marin SA

Based upon the result of the certification audit, the SQS awards

the SQS Certificate, Category ISO 9001/EN 29 001

In the course of the certification audit by SQS, it was established that the firm's Quality System is complete and appropriate, maintained and applied, and also meets the requirements of the above mentioned international standards and model.
This SQS-Certificate is valid for three years.

Berne, 16 March 1992
This SQS Certificate is valid until and including 15 March 1995

For the Secretariat:

General Manager of the SQS

For the Board:

President of the SQS

Board Member of the SQS

Quality Assurance and Reliability

1. Management Responsibility

The Management of EM Microelectronic-Marin S.A. have engaged themselves to provide all services in a manner which not only conforms to contractual and regulatory requirements but also meets the total satisfaction of its customers' needs.
Employees are trained to know, understand and discharge their individual quality responsibilities in all areas of their work activity.
Management efficiency is evaluated once a year in accordance with a defined evaluation means and criteria.
Tasks and responsibilities are clearly defined indicating the sharing out of authority and responsibilities.

2. Quality System

The Quality System that has been established at EM Microelectronic-Marin S.A. is based on the International Standard ISO 9001 "Quality Systems - Model for Quality Assurance in Design, Production, Installation and Servicing".
The schematic representation of the quality system is shown in Fig. 1.

A. The QA manual consists of the quality policy, the objectives and principles which emanate from it to guarantee the required quality of products and services, the manufacturing organisation and the task and responsibility allocations with respect to quality assurance at all levels of the company.
B. Organisational procedures, containing the management and technical "know-how".
C. Detailed description of organisational rules and work practices.
D. Run cards, forms, auxiliary means.

3. Contract Review

Contracts are reviewed using the criteria
a) Work scope
b) Customer specifications
c) Relevant national, European, international and / or U.S. MIL standards and procedures
d) Technical feasibility
e) Delivery schedule

Order acceptance is the responsibility of the Order Acceptance Meeting where all assigned personnel confirm that all criteria for their department / discipline can be met.

4. Design Control

The design control is required to ensure the complete fulfilment of all technical, programme and contractual requirements during the design and development of new products or processes.

Process Development
The process development steps include acceptance of process specifications, pilot production and characterization.

Product Development
The Design Initiation stage assesses the total resources required to accomplish each design project prior to its acceptance.
The Design Rules ensure that in all respects, IC layout comply with the Design Rules appropriate to the design and technology.
The Design Reviews ensure that all necessary interfaces between design and other internal departments and customers are properly established and maintained by means of Design Reviews. All relevant technical details, quality requirements and programme constraints are reviewed.

QA System Representation

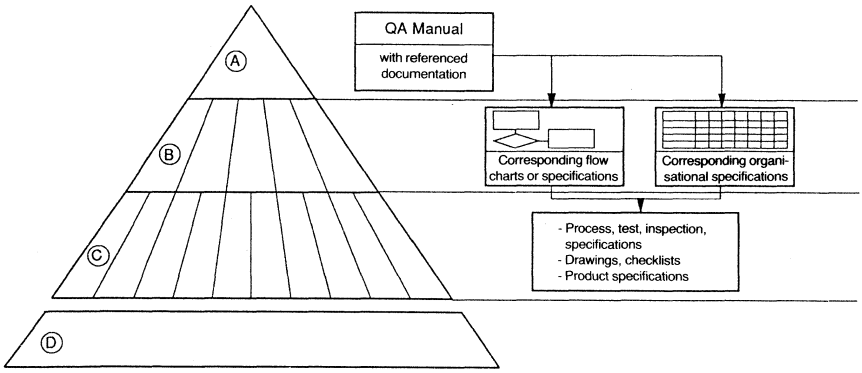


Fig. 1

Qualification Program
Device, process and package qualification programs are thoroughly documented and required failure rate criteria are established as part of the development cycle. Only engineering samples are allowed to be delivered without meeting the qualification criteria. The qualification programs have their basis and are in accordance with MIL-STD-883.
For example, the following is a list of tests necessary for product qualification.

1) Design Verification. It includes simulation, design and electrical rule checking, design acceptance (including viability in user applications).
2) Test Programm Verification to check the test coverage and guard bands.
3) Verification of Customer requirements, Device Specification and performance in the whole temperature range.

Sample of the first 3 lots must pass these tests:

4) 125°C operating life, 1000 hours.
5) 150°C data retention, 1000 hours, for memory circuits
6) Temperature cycling −40 / +85°C, 1000 cycles.
7) THB, 85°C / 85% RH with bias, 1000 hours.
8) Pressure pot, 168 hours.
9) E.S.D. (1.5 kΩ / 100 pF), 1000 V at all pins. Many devices have higher E.S.D. ratings, consult the product data sheet.
10) Static Latch-up sensitivity, ± 30 mA on all inputs / outputs.
11) Dynamic Latch-up sensitivity, ± 50 V on all inputs / outputs with 220 pF, 50 Ω.

5. Document Control

Document Control includes the control and distribution of all specifications, procedures, drawings and work instructions required for materials, subcontracted products or services, design, manufacture, inspection and testing of product. These documents provide the basis for the design and manufacture of a consistent and reliable product.
All changes to documents shall be implemented in writing, reviewed and approved by the manager of the responsible department and the Quality Management.
Distribution of documents is in accordance with two different types of marking on the specifications:

a) "Valid Copy" with uptdating service provided to the recipient, controlled copy.
b) "Valid Copy" and "Uncontrolled Copy" stamps indicates that no update service is provided when changes occur.

6. Purchasing

Vendor and subcontractor surveys are performed prior to their use to determine the potential vendor's quality capabilities and to ascertain the effectiveness and extent of their quality system. Vendors and subcontractors are then evaluated / audited on their ability to meet defined requirements including quality requirements.
Following satisfactory initial approval, suppliers and subcontractors are placed on the approved vendors list.
Suppliers and Subcontractors are quarterly evaluated on the basis of the incoming inspection results and delivery times.

7. Purchaser Supplied Product

All customer supplied materials are examined at entry for transit damage, completeness and correct type, proper identification, quantity and visual quality. In special cases, the initial control may include electrical testing.
Records are maintained of the receiving inspection results including arrangements made with the supplier for the return of any non-conforming, damaged or surplus to delivery material.

8. Product Identification and Traceability

Each product is identified through all stages of manufacture, repair or rework to final despatch.
The traceability is assured by the run card which is attached to the lot during manufacturing and by the information stored in a data base. The unique identification is recorded on all documents such as manufacturing run cards, process travellers, inspection and test records.

9. Process Control

Process quality control consists of routine monitoring of important process parameters such as resistivities, oxide thickness, mask alignment, dimensional checks, defect densities, bump parameters, bond strength and shear test measurements.
Statistical process charts are employed to record variability and highlight adverse trends. In addition, visual inspection of material is carried out at all stages of manufacture.
Regular reliability monitoring is implemented to assure continued uniformity of product reliability.
Periodic environmental and endurance testing are performed in accordance with US MIL STD or International (ISO) standard specifications.
Reliability assessment includes:

a) static life test
b) operating life test
c) high temperature bake
d) humidity bias test
e) autoclave
f) temperature cycle

10. Inspection and Testing

Receiving Inspection
All incoming materials used directly in the manufacture of EM products and those indirect materials that are specified as requiring incoming inspection are subject to

receiving inspection and approval in accordance with applicable specifications and / or drawings.

In-process Inspection and Testing
Quality control inspections are performed as either monitor or gate functions.
All in-process inspections, controls, measurements and tests are carried out in accordance with the requirements of the appropriate flow charts, quality plans and internal specifications.

Final Inspection and Testing
At the completion of all manufacturing operations each product lot is subjected to a final control. A random sample is selected from the lot to be released in accordance with the specified AQL or LTPD.
Any lot rejection will be cause for introducing corrective action and /or possible procedural changes, as appropriate.
All records are analysed and reported to the Direction on a weekly basis.

11. Inspection, Measuring and Test Equipment

In order to guarantee that the product resulting from different activities of EM Microelectronic-Marin S.A. meets the required specifications, all inspection, measuring and test equipment used in the manufacturing processes are verified and calibrated at regular intervals.

The calibration procedures are carried out on all inspection, measuring and test equipment, in particular:
a) registration and verification of new equipment
b) identification and logging all inspection, measuring and test euipment
c) calibrate, check and repair all equipment, at regular intervals according to the specified calibration procedures
d) control corrective / preventive actions on products in course or already manufactured when an equipment is identified as being out of specification
e) identify, declare obsolete, destroy equipment declared out of use
f) register and file the calibration results
g) check of sub-contracted calibration procedures.

12. Inspection and Test Status

A system of identifying the inspection status of product during all stages of manufacture is maintained by means of run cards, inspection sheets, adhesive and ink stamps, signatures and other control devices / forms.
Inspection stamps are used to verify inspection results on movement documentation (i.e. run cards). All stamps are issued by the Quality Department to a list of approved personnel. The QA&R Manager authorises the issuance and removal of all stamps.

13. Control of Non-Conforming Product

In the case of material found to be non-conforming during production inspection, non-conforming material and accompanying documentation are clearly identified and segregated from the production line to prevent unauthorised use.
The Material Review Board assesses the nature, severity, status and constraints relative to the non-conforming material decides its disposition:
Scrap, use as is, rework or rescreen, deviation permit, waiver / concession, return to supplier or subcontractor (for materials rejected by Incoming Inspection), or further evaluation.

The MRB can decide to ask the customer for:
a) an authorization to deviate process parameters from specified process (before production)
b) an authorization to release non-conforming material (after production).

14. Corrective Actions

An objective of EM is to be in the process of continuous improvements. The improvement of products, processes, services and documents is achieved on the basis of regular analysis or according to the needs. Any operation, procedure, document or service can be identified for corrective actions, within the company or to suppliers and subcontractors.
A management system ensures that corrective actions are taken, that they are effective and that the preventative actions are, where appropriate, implemented in established documented procedures.

15. Handling, Storage, Packaging and Delivery

A system is maintained for the preservation, segregation and handling of all material from initial storage through the entire manufacturing process. All precautions are taken to protect material from abuse, misuse, damage, deterioration and unauthorised use.
A comprehensive system of requirements and precautions has been established to eliminate, wherever possible, the generation and discharge of electrostatic charges which may damage or destroy static-sensitive products. All die from scribing onwards, including packaged product are considered static sensitive.
Devices for which compliance with the product or customer's specification has been demonstrated is accepted into the Finished Goods Store.

16. Quality Records

EM has established procedures for the identification, collection, filing, storage, maintenance and disposition of quality records. These records provide evidence of the product quality achieved and the effective operation of the Quality System.

Records are maintained:
a) device and material qualifications
b) audits (internal and external)
c) calibration
d) incoming Q.C. and production Q.C.
e) certicates of conformity
f) reliability data
g) customer returns
h) deviation or waivers requests
i) material review board
j) supplier corrective actions
k) supplier / subcontractor appraisal and qualification
l) despatch information
m) process control including SPC
n) run cards / routine sheets for all manufacturing areas
o) training reports

Where no contractual obligation exists, records are retained for a minimum period of five years.

17. Internal System Audit

Different types of audits are performed on a regular basis:
a) system audit
b) process compliance audit.

The system audits are performed according to the ISO 9001 standard requirements. System defficiencies are reported and appropriate corrective actions taken. The quality system and audit activities are audited once a year (chapters 2 and 17 of the ISO 9001 Standard) by a representative appointed by the Direction.
In order to verify the conformance of technical procedures to actual operations, random audits are performed according to internal procedures.

18. Training

All personnel performing tasks or activities affecting quality are adequately trained either by in-house schemes or by a recognised external organisation.

The training are planned to realise four precise aims:
1) to improve job knowledge
2) to prepare for promotion
3) to prepare for the professional environment and new production organisations and facilities
4) to improve individual and group capacities.

Regular assessment of personnel allows their training needs to be identification. The EM Training Centre maintains documented evidence of all personnel training.

19. Servicing after Sales

Every client has the ability to contact directly the relevant person in the Sales Department, in the appropriate BPU (Business Product Unit) or QA Department.
The servicing on a contractual basis is limited to the warranty (General Terms of Sale) of product to the specifications.
In case of customer return, the material with the attached documents will be entered in the QA Department. Following analysis, the Quality Management decides the corrective and / or preventative actions. The customer is then notified of the results.

20. Statistical Techniques

Inspections
QC sampling is on an AQL or LTPD basis, and is based upon the MIL-STD-105 (IEC 410) and MIL-M-38510.
Final inspection of packaged ICs is as follows:
Electrical: 0.1% AQL, I.L. II.
Visual: 0.4% AQL, I.L. II.

Reliability
New products and process changes are subjected to a qualification procedure using LTPD sampling techniques. Device life time (or MTBF) is extrapolated from a high temperature, accelerated life test sample.

SPC
Statistical Process Control (SPC) is an important interactive element of the complete quality system.

SPC Policy may be summarised as follows:
a) SPC provides verification that a process is under control, thereby avoiding unnecessary adjustments.
b) Prompt action shall be taken when adverse trends are indicated or warning limits are exceeded.
c) Causes of unnatural change are detected and eliminated, thereby removing unnatural variations.

Table of Contents

LCD-Driver

Features

- Drives up to 32 LCD segments in direct drive (versions 01/02) with an additional BP output
- Low power consumption
- Wide operating voltage range 3 to 15V
- Wide operating temperature range −40° to +85°C
- High noise immunity
- Few external components needed
- Serial data input/output
- 3 wire interface: CLOCK, DATA and STROBE
- N-way multiplex capability (versions 03/04)
- On-chip latches separate display and control sections
- Version 02/04 cross free cascadable
- Internal frequency control with on-chip oscillator
- Cascadable with on-chip wave shaping
- CMOS and NMOS compatible inputs
- Packages DIL40, PLCC44 and TAB

Description

The M 6003 is a CMOS integrated circuit that drives all LCD displays with either direct drive or multiplex voltage levels. The device accepts serial input data and requires only additional clock and strobe lines. Up to 32 segments may be driven by one device in direct drive. In the N-way multiplex version, 32N segments may be driven (N being limited by the display type in use). Versions 01 and 02 are for direct drive applications, versions 03 and 04 for multiplexed drive applications. Standard packaging for the M 6003 is 40 pin DIL plastic package, 44 pin PLCC and TAB on 35mm film.

Applications

- Instrumentation readouts
- Automotive dashboards
- Digital clocks, counters, etc.
- Large displays
- Telephones
- Balances and scales
- Portable battery operated products
- TAB for space limited, light weight products

Typical Operating Configuration

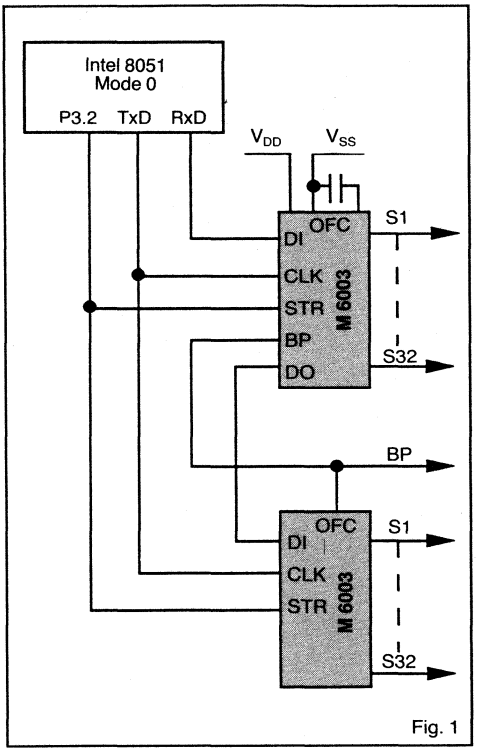


Fig. 1

Versions Available

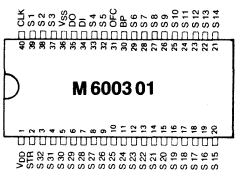
Version	Function	Packages
01	Direct drive	DIP40, PLCC44, TAB
02	Direct drive cascadable on single layer PCB	PLCC44, TAB
03	Multiplexed drive	DIP40, PLCC44, TAB
04	Multiplexed drive cascadable on single layer PCB	PLCC44, TAB

Table 1

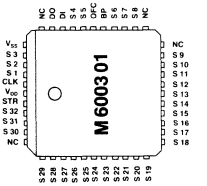
Pin Assignment

Version 01

a) DIP 40



b) PLCC 44



c) Film

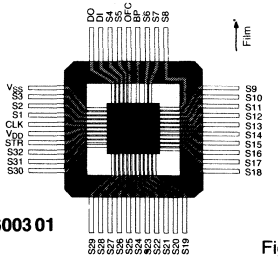
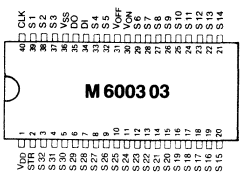


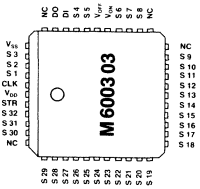
Fig. 2

Version 03

a) DIP 40



b) PLCC 44



c) Film

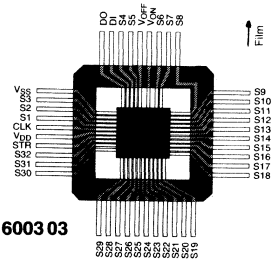
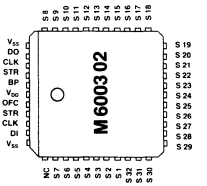


Fig. 3

Version 02

a) PLCC 44



b) Film

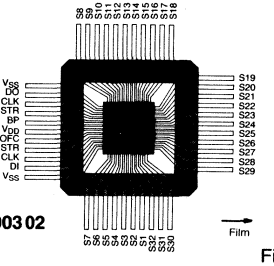
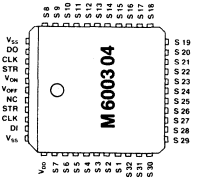


Fig. 4

Version 04

a) PLCC 44



b) Film

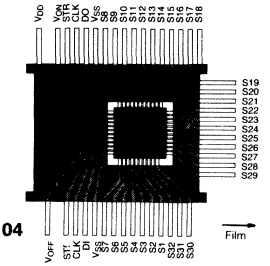


Fig. 5

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{MAX}	−0.3 to +17V
Voltage of any pin to V_{SS}	V_{MAX}	−0.3V
Voltage of any pin to V_{DD}	V_{MAX}	+0.3V
Storage temperature range	T_{STO}	−65 to +150°C

Table 2

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Handling Procedures

This device contains circuitry to protect the terminals against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit. For proper operation it is recommended that all terminal voltages are constrained to the range $V_{SS} < V_{TERMINAL} < V_{DD}$, unless specially permitted. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

3

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	3		15	V

Table 3

Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V$, $V_{SS} = 0$, unless otherwise stated

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Supply current	I_{DD}	OFC at V_{DD}		1.5	3	μA
		C = 100pF, see Fig. 8		30	40	μA
		f<100Hz, oscillator driven		4	7	μA
I/O Lines						
Input high voltage	V_{IH}	$V_{DD} = 3V$	0.7 V_{DD}		V_{DD}	V
		$V_{DD} \geq 5V$	0.5 V_{DD}		V_{DD}	V
Input low voltage	V_{IL}	$V_{DD} \leq 5V$	0		0.2 V_{DD}	V
		$V_{DD} = 15V$	0		0.1 V_{DD}	V
Input voltages for OFC	V_{IH}		0.9 V_{DD}		V_{DD}	V
	V_{IL}		V_{SS}		0.1 V_{DD}	V
Input current	I_L	$V_{SS} < V_{IN} < V_{DD}$			10	μA
Input current for OFC	I_L	$V_{SS} < V_{IN} < V_{DD}$	1	3	10	μA
Input capacitance	C_{IN}			5		pF
Data output impedance	R_{ON}	$I_L = 1mA$		0.6	1	kΩ
Segment output impedance	R_{ON}	$I_L = 10\mu A$		15	40	kΩ
Backplane output impedance	R_{ON}	$I_L = 150\mu A$		1	2	kΩ

* Typical values are at 25°C and nominal voltages.

Table 4

Timing Characteristics at $V_{DD} = 5V$, $V_{SS} = 0$ and $T_A = 25°C$, unless otherwise stated

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock pulse width	t_{CL}, t_{CH}		250		∞	ns
Strobe pulse width	t_{PS}		200		t_{CL}	ns
Data set-up time	t_{DS}		250			ns
Data hold time	t_{DH}		100			ns
DO rise and fall time	t_R, t_F	$C_L = 50pF$, 10% to 90%			150	ns
DO propagation delay	t_{PD}	$C_L = 15pF$			500	ns
Strobe delay	t_{SD}		150			ns
Clock rise and fall time	t_{CR}, t_{CF}	10% to 90%			200	ns
Backplane frequency	f_{BP}	C = 33pF	40		90	Hz

Table 5

Timing Waveform

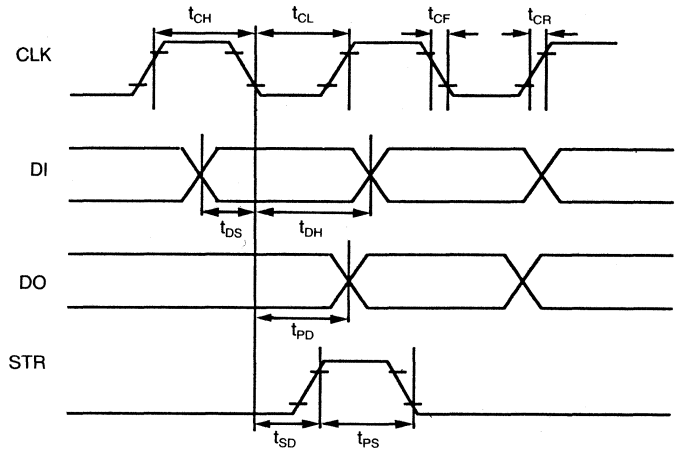


Fig. 6

Block Diagram

Direct drive versions shown:
Links I: direct drive
Links II: N-way mux

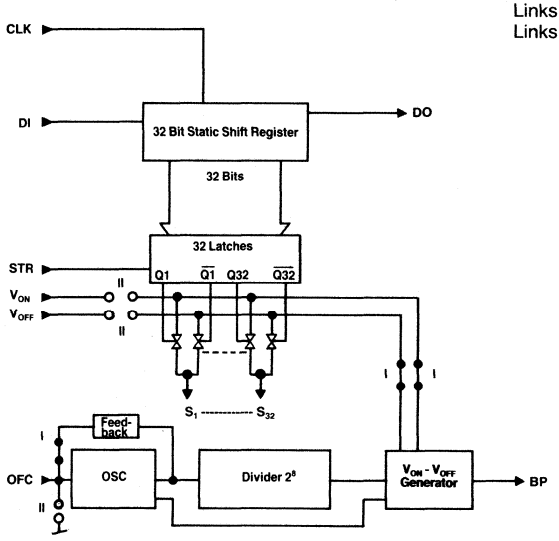


Fig. 7

Pin Description

Name	Function
V_{DD}	Positive supply terminal
V_{SS}	Ground terminal
V_{ON}	On-voltage waveform input (03/04)
V_{OFF}	Off-voltage waveform input (03/04)
OFC	Oscillator frequency control terminal (01/02)
DI	Serial data input
DO	Serial data output
CLK	Clock input
STR	Strobe input
S xx	Segment drive outputs
BP	Backplane drive output (01/02)

Table 6

Functional Description

General

Referring to the block diagram (Fig. 7), the M 6003 may be divided into two parts: the segment drivers and the waveform generator. The segment driver part consists of a 32 bit static shift register paralleled by 32 latches, which drive 64 analog switches. The waveform generator contains an RC oscillator, divider chain and the generator for the backplane and segment drive signals. The waveform generator is disconnected in the versions 03/04 for multiplexed drive, the corresponding waveforms being fed directly to the analog switches by the V_{ON}/V_{OFF} inputs.

V_{DD}, V_{SS}, V_{ON}, V_{OFF}

These pins constitute the supply lines. Only V_{DD} and V_{SS} are used in the direct drive mode (versions 01/02), but for multiplexing (versions 03/04) the extra voltages V_{ON} and V_{OFF} are needed. These two voltages depend upon the LCD and the multiplex scheme used. V_{DD} - V_{SS} being the supply voltage for the logic part, care should be taken that the swing of the input signals does not go outside this range.

OFC Input

This input, present in the direct drive versions (versions 01/02) only, controls the frequency of the waveforms of the segment and backplane drivers. Two different modes are possible: free running or externally driven. In the free running mode, the frequency of the RC oscillator is inversely proportional to the capacitance connected between OFC and either V_{SS} or V_{DD}. With 33pF connected, the internal divider chain provides a basic LCD drive frequency. The temperature variation is approximately 0,6Hz/°C. When the OFC input is driven by a logic signal, an internal sense circuit switches off the oscillator and bypasses the divider chain thus generating a drive frequency in phase with the input signal.

BP Output

The backplane drive output, available only in the direct drive versions (versions 01/02), delivers a square wave signal with amplitude V_{DD} - V_{SS} of a frequency determined by the OFC input (see "OFC Input").

Segment Outputs

The 32 segment-drive outputs S_1 to S_{32} have their display drive waveforms fed from the on-chip oscillator (versions 01/02) or from the V_{ON}/V_{OFF} inputs (versions 03/04). Each of the 32 corresponding data bits output by the latches selects for its segment the ON or the OFF waveform. The latches are loaded from the data input shift register by a positive pulse on the STR input, and the segment number of a data bit is the number of clock pulses used to shift it in from the data input pin DI.

Direct Drive Versions (versions 01/02)

The 32 segment-drive outputs deliver each a square wave of the amplitude V_{DD} - V_{SS} at the frequency of the backplane output (see "BP Output"). This square wave is either in phase with the backplane signal (data 0) or in antiphase (data 1), resulting in a differential voltage across the corresponding LCD segment of either 0 or [V_{DD} - V_{SS}].

Multiplexed versions (versions 03/04)

Depending on the data latched for the corresponding segment, the 32 segment drive outputs are either connected to the V_{ON} input (data 1) or the V_{OFF} input (data 0). The resulting voltage across the LCD segment is the difference between the V_{ON}/V_{OFF} output waveform and the segment's counter-electrode waveform from another driver. Details of different multiplex schemes are available on request.

DI Input

Data present on the DI pin is clocked in at the falling edge of the clock signal (see "CLK Input") and shifted through the 32 stages of the M 6003. A logic high level on the DI input causes a segment to be visible (direct drive) or connected to V_{ON} (multiplex drive). The timing and waveforms are shown in Fig. 6. The segment number corresponds to the number of clock pulses applied to shift in the data bit concerned.

DO Output

The data presented at the DI input will be shifted out at the DO output 32 clock periods later at the falling edge of the clock signal (see "CLK Input"). Exact timing and waveforms are shown in Fig. 6.

CLK Input

This input is used to clock the data present at the DI input through the shift register. Loading, shift and output of the data occur with the falling edge of the clock signal (Fig. 6). In order to avoid race conditions, data and strobe should be changed with the rising edge of the clock signal.

STR Input

The strobe signal is used to latch the data held in the shift register. A logic high level on the STR input causes a parallel loading of the shift register data into the output latches. If the STR input is held high, the latches are transparent. Timing and waveforms are shown in Fig. 6.

Cascading

Due to the on-chip wave shaper, the M 6003 is specially

suited for cascading. Just connect the DO pin of the previous device to the DI pin of the following and tie all CLK, STR and supply lines together. A few precautions should be taken with the OFC and BP pins (versions 01/02 only) in order to achieve best performances. When the waveforms are generated with the internal oscillator, connect the OFC input of the following device to the BP output of the previous one. Only one capacitor is then needed to provide frequency control. The same procedure may be used for driving OFC, or all OFC inputs may be connected to a common driving signal. The backplane of the LCD display should be connected to the free BP output thus minimizing the DC components of the driving signals.

Versions 02 and 04

Due to internal links, these two versions in either PLCC44 or TAB package allows the cascading of several M 6003 on a single layer PCB (Fig. 9 and 10). Version 02 is for direct driven LCD displays, version 04 for multiplexed displays.

Typical Applications

M 6003 01/02 Circuits Driving a 64 Segment Display in Direct Drive

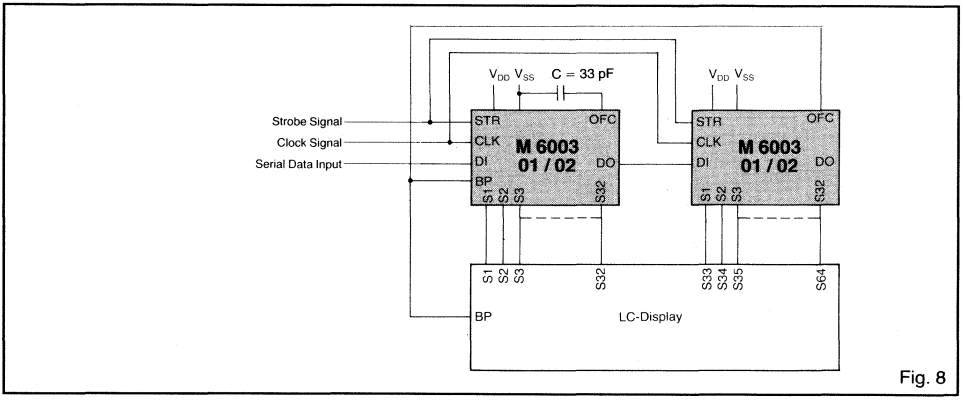


Fig. 8

M 6003 03/04 Circuits Driving an LCD at Low Mux Rate

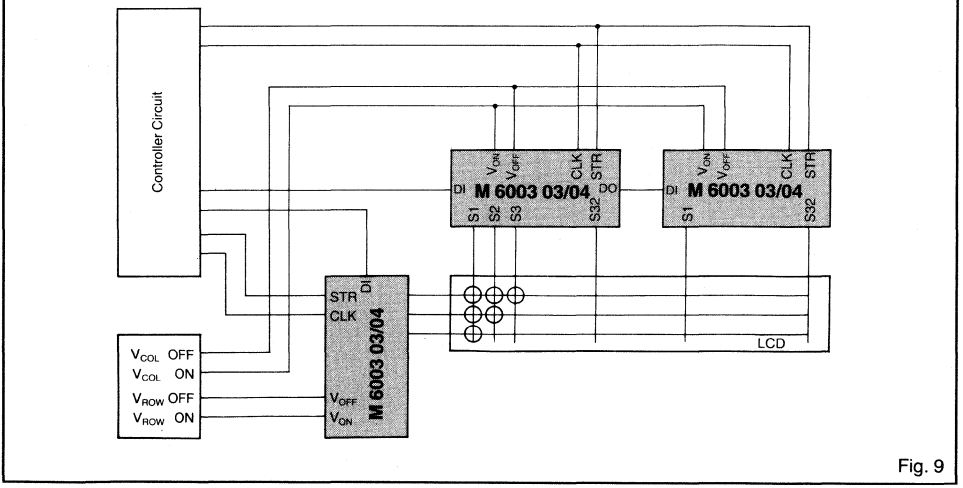


Fig. 9

Cascaded Version 02 for Direct Drive Application

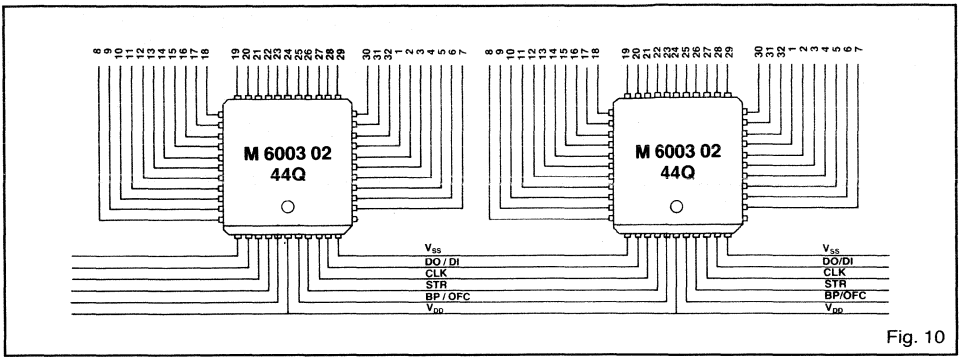


Fig. 10

Cascaded Version 04 on Film

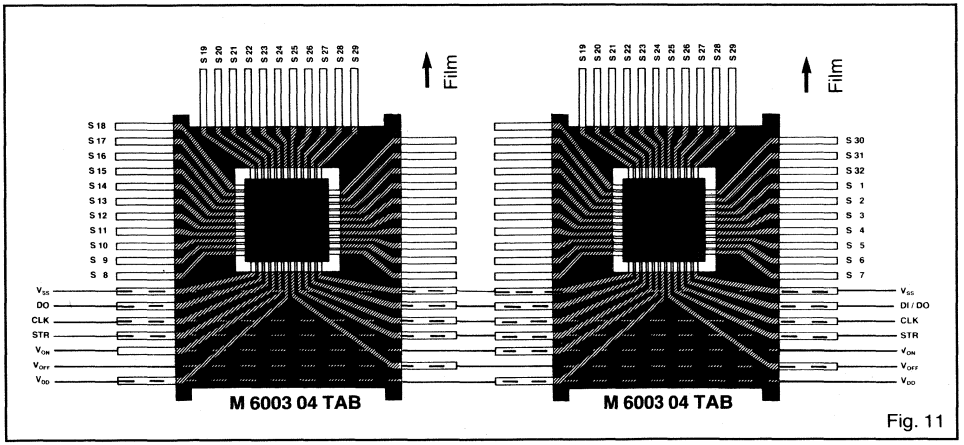
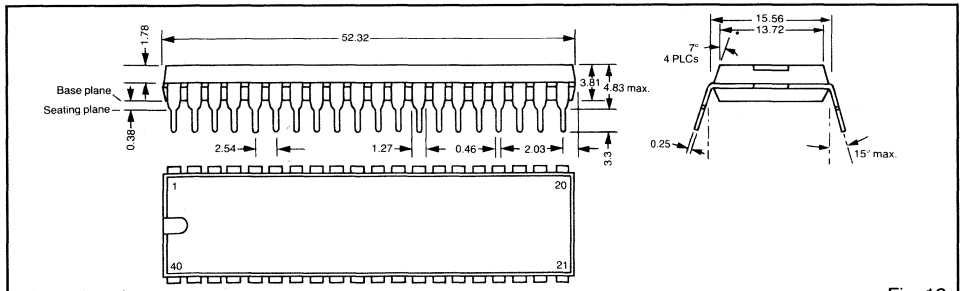


Fig. 11

Package and Ordering Information

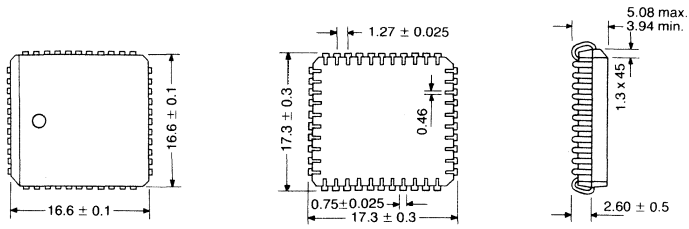
Dimensions of DIP40 Package



Dimensions in mm

Fig. 12

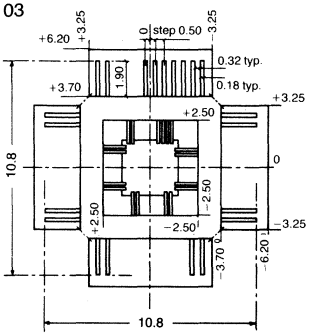
Dimensions of PLCC44 Package



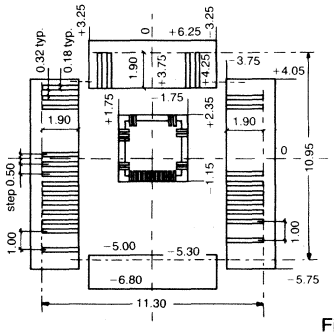
Dimensions in mm Top Bottom Side Fig. 13

Dimensions of TAB Packages

Versions 01 - 03



Version 04



Dimensions in mm Fig. 14

Recommended Solder Area (Top View)

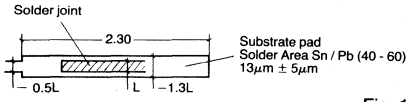


Fig. 15

Soldered Lead (Side View)

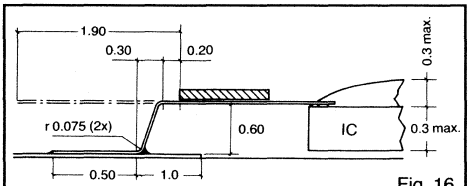


Fig. 16

Ordering Information

The M 6003 is available in the following versions and packages:

Version 01	DIP 40	M6003 01 40P
	PLCC 44 pin	M6003 01 44Q
	Film*	M6003 01 TAB
Version 02	PLCC 44 pin*	M6003 02 44Q
	Film*	M6003 02 TAB
Version 03	DIP 40*	M6003 03 40P
	PLCC 44 pin*	M6003 03 44Q
	Film*	M6003 03 TAB
Version 04	PLCC 44 pin*	M6003 04 44Q
	Film*	M6003 04 TAB

* and chip form, on request

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LCD-Driver

(Not recommended for new designs. Contact EM-Microelectronic regarding replacement product.)

Features

- Drives up to 40 LCD segments in direct drive
- Serial data input
- Separate input-logic and display voltages
- Positive logic voltage, negative display voltage
- On-chip latches separate control and display sections
- Crossfree cascadable
- CMOS and NMOS input compatible
- High noise immunity
- Low power consumption, 10 μA max.
- Outputs short circuit protected
- Packages: TAB and PLCC52

Description

The M 6004 series of monolithic CMOS integrated circuits drive LCD displays with either direct or N-way multiplex level drives. The circuit drives up to 40 LCD segments from a serial clocked input. It has a serial output for cascading to further drivers. The serially clocked data is parallel loaded into 40 latches under control of the strobe pin. Two segment outputs are driven with extra power for driving the backplane in direct drive. The multiplex drive version can be used either as a row driver or as a column driver.

Applications

- Public information panel
- Instrumentation readouts
- Voltmeter, counter, digital clocks
- Automotive dashboards
- 40 bit serial in / parallel out shift register

Typical Operating Configuration

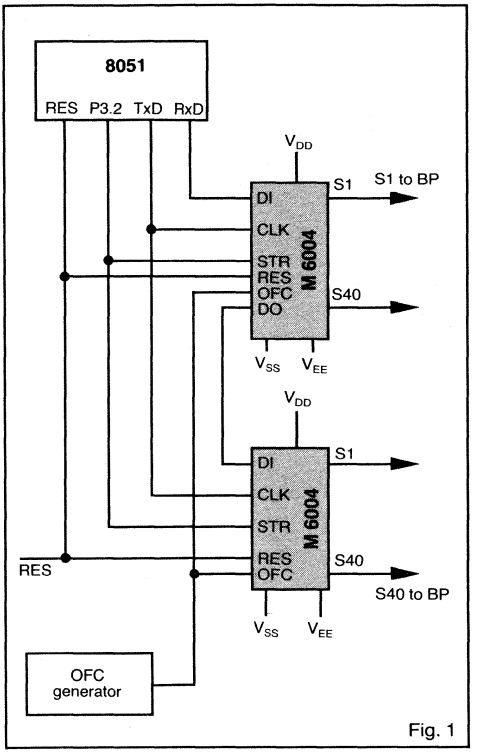


Fig. 1

Versions Available

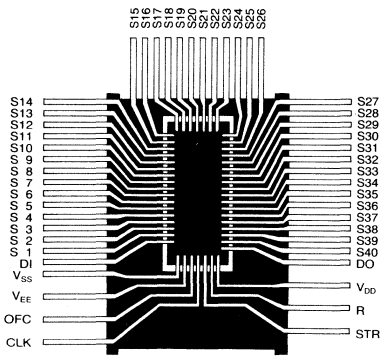
Version	Function	Packages
02	Direct drive	TAB, PLCC52
04	Multiplexed drive	TAB, PLCC52

Table 1

Pin Assignment

M 6004 02

a) Film



b) PLCC52

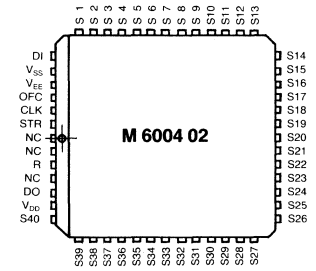
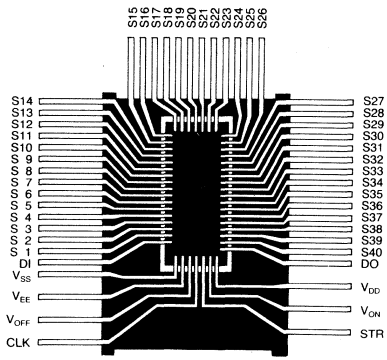


Fig. 2

M 6004 04

a) Film



b) PLCC52

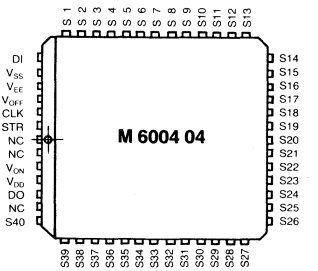


Fig. 3

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Logic Supply Voltage	V_{DD}	−0.3 to +6V
Display Supply Voltage	V_{DD}-V_{EE}*	V_{DD}-V_{SS} to +17V
Voltage of DI, CLK, STR, OFC	V_{MAX}	−0.3 to V_{DD} +0.3V
Storage Temperature Range	T_{STO}	−65 to +150°C
Power Dissipation	P_{MAX}	100mW

* $V_{EE} < V_{SS}$; $V_{EE} \leq V_{ON} \leq V_{DD}$; $V_{EE} \leq V_{OFF} \leq V_{DD}$

Table 2

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	4.5		5.5	V

Table 3

Electrical Characteristics

T = 25°C, V_{SS} = 0V, V_{DD} = 5V, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Temperature	T		−40		+85	°C
Logic Supply Voltage	V_{DD}		+4.5	+5	+5.5	V
Display Supply Voltage	$V_{DD}-V_{EE}$		$V_{DD}-V_{SS}$		+12*	V
Supply Current (static)	I_{DD}				10	μA
Supply Current (static)	I_{SS}				10	μA
Supply Current (dynamic)	I_{SS}				10	mA
Control Signals DI, CL, LD, FL						
Input Voltage (high)	V_{IH}		+4.2			V
Input Voltage (low)	V_{IL}				+0.8	V
Static Input Current	I_{IN}	$V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$			1	μA
Output Signal DO						
Output Voltage (high)	V_{OH}	$I_H = < 2\mu A$	$V_{DD}-50mV$			V
Output Voltage (low)	V_{OL}	$I_L = < 2\mu A$			$V_{SS}+50mV$	V
Segment Output (version 02)						
1 and 40		$V_{DD} - V_{EE} = 8V$				
Output Voltage (high)	V_{SH}	$I_H = 20\mu A$	$V_{DD}-50mV$			V
Output Voltage (low)	V_{SL}	$I_L = 20\mu A$			$V_{EE}+50mV$	V
Segment Outputs (versions 04)						
1 to 40		$V_{DD} - V_{EE} = 8V$				
Output Voltage (high)	V_{SH}	$I_H = 10\mu A$	$V_{DD}-50mV$			V
Output Voltage (low)	V_{SL}	$I_L = 10\mu A$			$V_{EE}+50mV$	V
Segment Outputs (versions 02)						
2 to 39		$V_{DD} - V_{EE} = 8V$				
Output Voltage (high)	V_{SH}	$I_H = 10\mu A$	$V_{DD}-50mV$			V
Output Voltage (low)	V_{SL}	$I_L = 10\mu A$			$V_{EE}+50mV$	V

* $V_{EE} < V_{SS}$; $V_{EE} \leq V_{ON} \leq V_{DD}$; $V_{EE} \leq V_{OFF} \leq V_{DD}$

Table 4

Timing Characteristics

T = 25°C, V_{SS} = 0 V, V_{DD} = 5 V, unless otherwise specified

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Clock High Pulse Width	t_{CL}	V_{DD} = 4.5V	$V_{DD} - V_{EE} = 4.5V$	900			ns
	t_{CL}		$V_{DD} - V_{EE} = 5V$	600			ns
	t_{CL}		$V_{DD} - V_{EE} = 12V$	300			ns
Clock Low Pulse Width	t_{CL}	V_{DD} = 4.5V	$V_{DD} - V_{EE} = 4.5V$	900			ns
	t_{CL}		$V_{DD} - V_{EE} = 5V$	600			ns
	t_{CL}		$V_{DD} - V_{EE} = 12V$	300			ns
CL, LD Rise and Fall Time	t_{CR}, t_{CF}					100	ns
Data Input Setup Time	t_{DS}		$V_{DD} - V_{EE} = 5V$	490			ns
	t_{DS}		$V_{DD} - V_{EE} = 12V$	200			ns
Data Input Hold Time	t_{DH}	Full range		0	−20		ns
Data Output Propagation	t_{PD}		$V_{DD} - V_{EE} = 5V$	20	500	900	ns
	t_{PD}		$V_{DD} - V_{EE} = 12V$	20	250	400	ns
STR Pulse Width	t_{PS}	V_{DD} = 4.5V	$V_{DD} - V_{EE} = 4.5V$	900		$2t_{CL}-t_{SD}$*	ns
	t_{PS}		$V_{DD} - V_{EE} = 5V$	600		$2t_{CL}-t_{SD}$*	ns
	t_{PS}		$V_{DD} - V_{EE} = 12V$	200		$2t_{CL}-t_{SD}$*	ns
STR Pulse Delay	t_{SD}			150		$2t_{CL}-t_{PS}$*	ns

* Only limited when cascading devices.

Table 5

Timing Waveforms

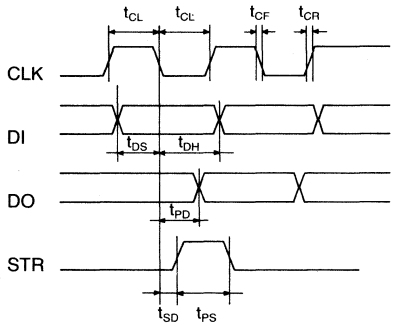


Fig. 4

Block Diagram

Direct Drive Version (M 6004 02)

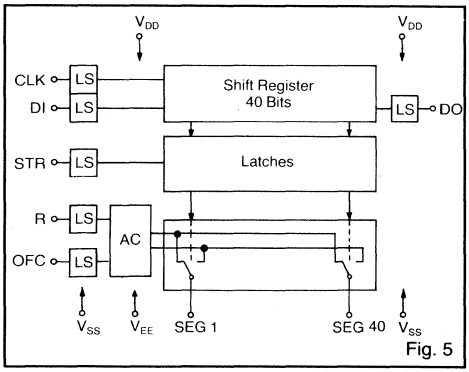


Fig. 5

Multiplex Version (M 6004 04)

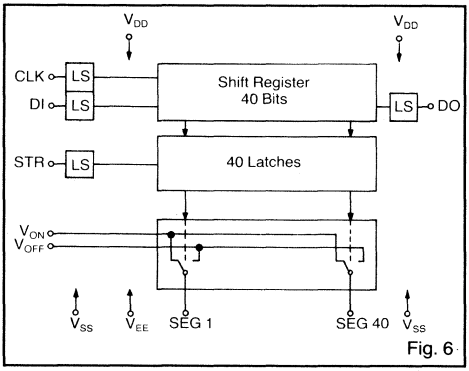


Fig. 6

Pin Description

M 6004 02 (direct drive)

Name	Function
S_{XX}	Segment drive outputs
DO	Serial data output
V_{DD}	Positive supply voltage
R	Display blank control input
STR	Strobes the input data into the output latches
CLK	Clock input
OFC	Input for segment frequency control
V_{EE}	Display GND voltage
V_{SS}	GND voltage for logic inputs
DI	Serial data inputs

Table 6

M 6004 04 (multiplex drive)

Name	Function
S_{XX}	Segment drive outputs
DO	Serial data output
V_{DD}	Positive supply voltage
V_{ON}	Power supply I/P depending upon LCD (row-on or column-on voltage)
STR	Strobes the input data into the output latches
CLK	Clock input
V_{OFF}	Power supply I/P depending upon LCD (row-off or column-off voltage)
V_{EE}	Display GND voltage
V_{SS}	GND voltage for logic inputs
DI	Serial data inputs

Table 7

See Fig. 2 and 3 for circuit pinning on the TAB film.

Functional Description

Chip Versions

The M 6004 exists in two versions which differ only in the generation of the segment voltages.
Versions 02: for direct drive displays. The segment voltages are generated on chip. This version can blank the display and also drive the backplane (see Fig. 8).
Versions 04: for multiplexed displays. The segment voltages V_{ON} and V_{OFF} are supplied from external circuitry so that driving waveforms corresponding to any multiplex scheme may be used. Each chip can be either a column- or a row-driver (see Fig. 9).

Powering and Driving Voltages

The V_{DD}, V_{SS} and V_{EE} pins constitute the supply lines (see Fig. 7). V_{DD} and V_{EE} are used in direct drive mode to generate the driving voltage signals, but for the N-way multiplexing external voltages V_{ON} and V_{OFF} supply the drive. In the N-way multiplex version, V_{ON} and V_{OFF} are fed directly to the O/P drivers as their amplitudes and frequency are determined externally. If the swing of the controlling logic signals is larger than the swing of V_{ON} and V_{OFF} then the negative supply of the control logic V_{SS} should be connected in common with the negative supply V_{EE} of the M 6004.

Supply Lines

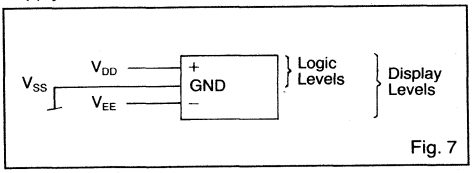


Fig. 7

Data Input/Output (DI/DO)

The data input DI pin accepts serial data from the data source. The data is clocked in at a rate determined by the clock input frequency. A logic "1" on DI causes a segment to be visible if the backplane is driven by a signal corresponding to logic "0" (or the opposing display element in a MUX display by logic "1"). The data output pin DO transfers the data to the next cascaded chip. The data at DO is equal to the data at DI delayed by 40 clock periods. In order to cascade devices the DO of one chip must be connected to DI of the following chip (see Fig. 8).

CLK Input

This input is used to clock the serial input data into the 40-bit shift register. Loading, shifting and outputting of the data occurs at the falling edge of this clock. When cascading devices, all clock lines should be tied together.

STR Input

The STR input is used to latch the input data shifted into the 40-bit shift register. The latched data is held for display. A logic "1" on the STR input transfers the data contained in the shift register cells to the corresponding latches. The latches remain open during the whole time STR remains at logic "1". When cascading devices the STR lines should all be connected.

OFC Input (version 02 only)

This input controls the segment voltage output frequency generation according to table 8. It must be connected to an external clock signal. When cascading devices, their OFC inputs may all be connected to a common signal.

Segment Switching Table

Latched Signal (DI) $0 = V_{IL}$ $1 = V_{IH}$	Signal OFC	Segment Voltage $0 = V_{EE}$ $1 = V_{DD}$
0	0	0
0	1	1
1	0	1
1	1	0

Table 8

R Input (version 02 only)

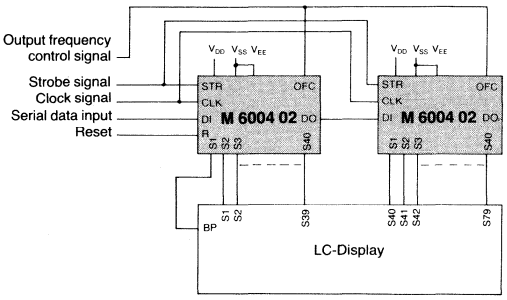
When R is active (high), the display is blanked: all segment outputs are tied to V_{EE}. R does not clear the information in the latches. If several driver outputs are connected together to drive the backplane, R should be active during turning the power on to avoid a short circuit caused of the random contents of the shift register, and should stay active until the first data are latched.

Line Driver

The number of O/P line drivers available on the chip is 40. Segment outputs 1 and 40 provide higher currents than the other segment outputs for direct drive backplane applications. If any drivers are paralleled together, care must be taken to ensure the drivers do not cause circuit malfunction by driving one against the other.

Typical Applications

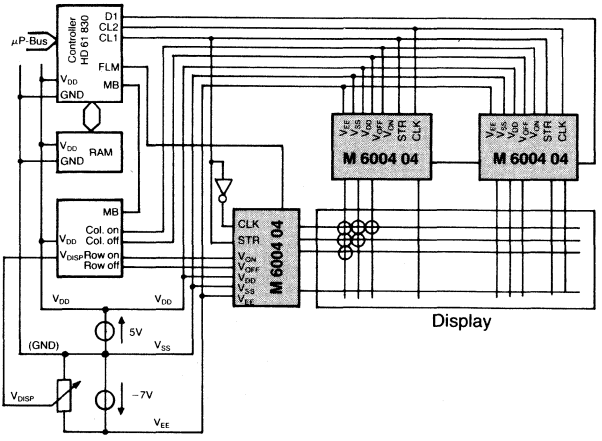
Type M 6004 02 Circuits Driving a 79 Segment Display in Direct Drive



As the backplane signal is identical to the external generated OFC signal it could be driven by this signal which would liberate one more segment driver. In this case you must switch backplane low (V_{EE}) when reset signal is activated.

Fig. 8

Type M 6004 04 Circuits Driving an 80 Columns by 40 Rows Multiplexed Dot Matrix Display



Please note: the M 6004 is a common V_{DD} device.

Fig. 9

Serial to Parallel Converter with Latching Inversable Outputs (or 40-output 2-way signal switcher)

OFC	Outputs
0	Normal
1	Inverted

Use version M 6004 04 in a similar way to make a signal switcher. Each output can be programmed via DI, CLK and STR to output one of two waveforms V_{ON} or V_{OFF}.

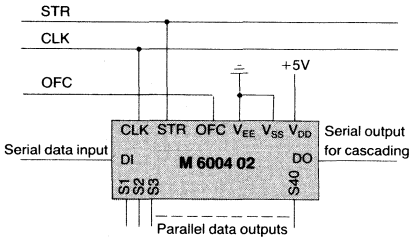


Fig. 10

Cascaded M 6004 02 TAB for Direct Drive Application

(The M 6004 04 TAB can be cascaded in the same way on a single layer PCB.)

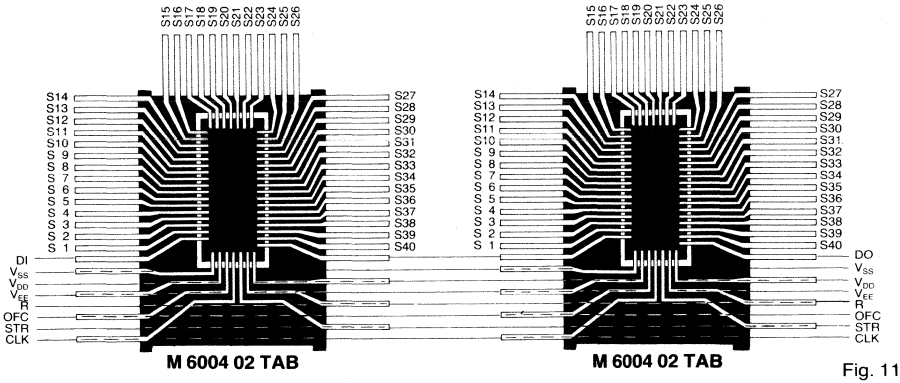


Fig. 11

Cascaded M 6004 02 PLCC52 for Direct Drive Application on a Single Layer PCB

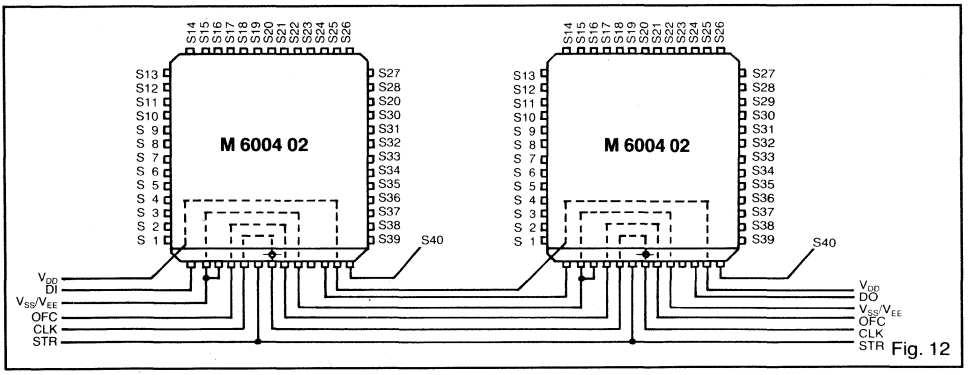
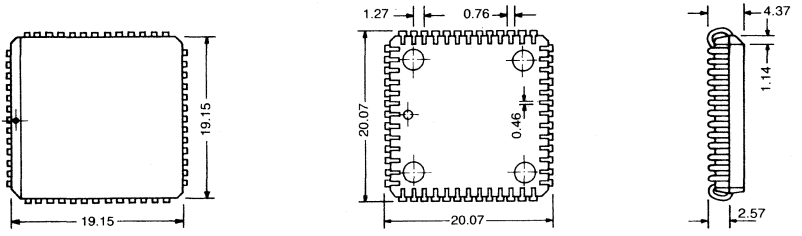


Fig. 12

Packages and Ordering Information

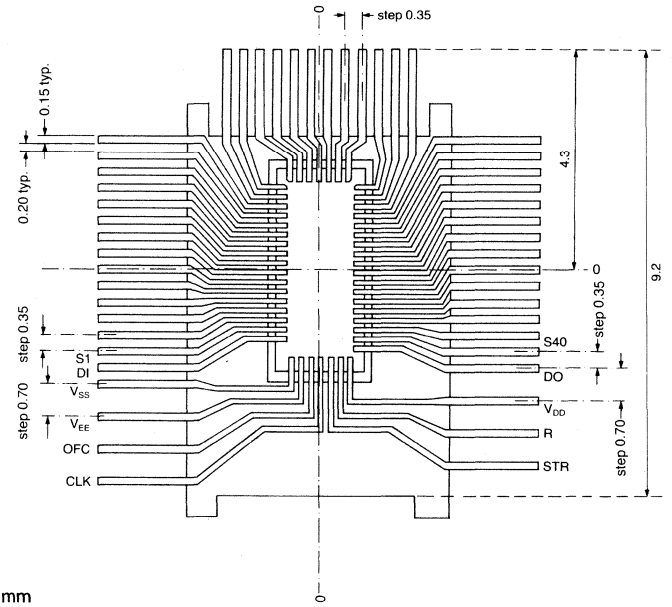
Dimensions of PLCC52 Package



Dimensions in mm

Fig. 13

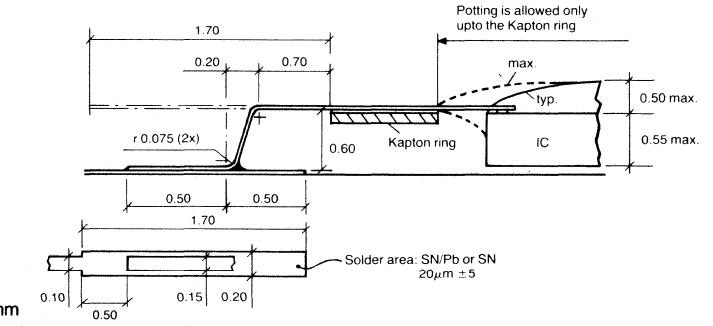
Dimensions of TAB Package



Dimensions in mm

Fig. 14

Side View and Recommended Solder Area



Dimensions in mm

Fig. 15

Package and Ordering Information

The M 6004 is available in the following packages:

TAB package: M 6004 02 TAB*
M 6004 04 TAB*

PLCC52 package: M 6004 02 52Q
M 6004 04 52Q*

* and chip form, on request

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Low Mux LCD Driver

Features

- V 6118 2 is 2 way multiplex with 2 rows and 38 columns
- V 6118 4 is 4 way multiplex with 4 rows and 36 columns
- V 6118 8 is 8 way multiplex with 8 rows and 32 columns
- Low dynamic current, 150 μA max.
- Low standby current, 1 μA max. at 25°C
- Voltage bias and mux signal generation on chip
- Display refresh on chip, 40 x 8 RAM for display storage
- Display RAM addressable as 8, 40 bit words
- Column driver only mode to have 40 column outputs
- Crossfree cascadable for large LCD applications
- Separate logic and LCD supply voltage pins
- Wide power supply range, V_{DD}: 2 to 6 V, V_{LCD}: 2 to 7 V
- BLANK function for LCD blanking on power up etc.
- Voltage bias inputs for applications with large pixel sizes
- Bit mapped
- Serial input / output
- Very low external component count
- −40°C to +85°C temperature range
- No busy states
- LCD updating synchronized to the LCD refresh signal
- QFP52 and TAB packages

Description

The V 6118 is a universal low multiplex LCD driver. The version V 6118 2 drives two way multiplex (two backplanes) LCD, the version V 6118 4, four way multiplex LCD, and the V 6118 8, eight way multiplex LCD. The display refresh is handled on chip via a 40 x 8 bit RAM which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 40 x 8 bit RAM (a set bit corresponds to an activated LCD pixel). The V 6118 has very low dynamic current consumption, 150 μA max., making it particularly attractive for portable and battery powered applications. The wide operating range on both the logic (V_{DD}) and the LCD (V_{LCD}) supply voltages offers much application flexibility. The LCD bias generation is internal. The voltage bias levels can also be provided externally for applications having large pixel sizes. The V 6118 can be used as a column only driver for cascading in large display applications. In the column only mode, 40 column outputs are available to address the display. A BLANK function is provided to blank the LCD, useful at power up to hold the display blank until the microprocessor has updated the display RAM.

Applications

- Balances and scales
- Automotive displays
- Utility meters
- Large displays (public information panels etc.)
- Pagers
- Portable, battery operated products
- Telephones

Typical Operating Configuration

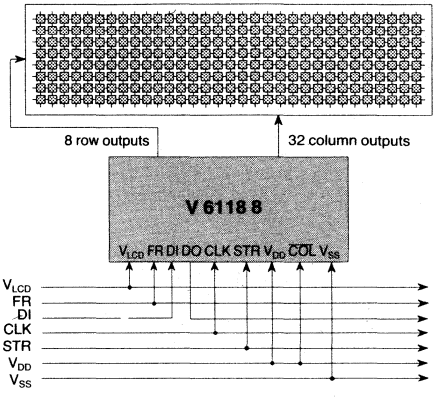
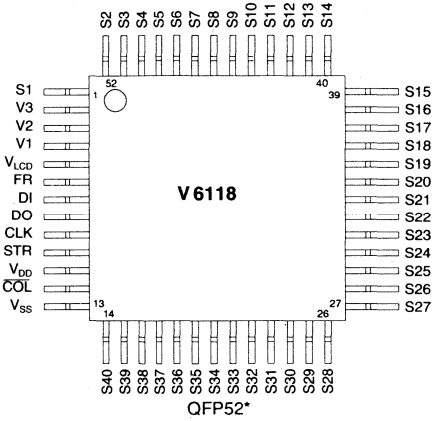


Fig. 1

Pin Assignment



QFP52*

See Fig. 15 for the TAB pinout

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	V_{DD}	−0.3V to 8 V
LCD supply voltage range	V_{LCD}	−0.3V to 8 V
Voltage at DI, DO, CLK, STR, FR, $\overline{COL}$	V_{LOGIC}	−0.3V to V_{DD}+0.3V
Voltage at V1 to V3, S1 to S40	V_{DISP}	−0.3V to V_{LCD}+0.3V
Storage temperature range	T_{STO}	−65 to +150°C
Power dissipation	P_{MAX}	100 mW
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{SMAX}	1000 V
Max. soldering conditions	T_S	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	2	5	6.0	V
LCD supply voltage	V_{LCD}	2	5	7.0	V

Table 2

Electrical Characteristics

V_{DD} = 5.0 V ± 10%, V_{LCD} = 2 to 7 V and T_A = −40°C to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Dynamic supply current	I_{LCD}	See note [1]		100	150	µA
Dynamic supply current	I_{DD}	See note [1] at T_A = 25°C		0.1	1	µA
Dynamic supply current	I_{DD}	See note [1]		3	12	µA
Dynamic supply current	I_{DD}	See note [2]		200	250	µA
Standby supply current	I_{SS}	See note [3] at T_A = 25°C		0.1	1	µA
Control Signals DI, CLK, STR, FR and $\overline{COL}$						
Input leakage	I_{IN}	$0 < V_{IN} < V_{DD}$		1	100	nA
Input capacitance	C_{IN}	at T_A = 25°C		8		pF
Low level input voltage	V_{IL}		0		0.8	V
High level input voltage for DI, STR, FR and $\overline{COL}$	V_{IH}		2.0		V_{DD}	V
High level input voltage for CLK	V_{IH}		3.0		V_{DD}	V
Data Output DO						
High level output voltage	V_{OH}	I_H = 4 mA	2.4			V
Low level output voltage	V_{OL}	I_L = 4 mA			0.4	V
Driver outputs S1 ... S40						
Driver impendance[4]	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 7 V		500	1.5	kΩ
Driver impendance[4]	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 3 V		1.2	2.5	kΩ
Driver impendance[4]	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 2 V		9		kΩ
Bias impedance V1, V2, V3[5]	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 7 V		16	20	kΩ
Bias impedance V1, V2, V3[5]	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 3 V		18	25	kΩ
Bias impedance V1, V2, V3[5]	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 2 V		30		kΩ
DC output component	$\pm V_{DC}$	See tables 4a and 4b, V_{LCD} = 5 V		30	50	mV

Table 3

[1] All outputs open, STR at V_{SS}, FR = 400 Hz, all other inputs at V_{DD}.

[2] All outputs open, STR at V_{SS}, FR = 400 Hz, f_{CLK} = 1 MHz, all other inputs at V_{DD}.

[3] All outputs open, all inputs at V_{DD}.

[4] This is the impendance between of the voltage bias level pins (V1, V2 or V3) and the output pins S1 to S40 when a given voltage bias level is driving the outputs (S1 to S40).

[5] This is the impedance seen at the segment pin. Outputs measured one at a time.

Column Drivers

Outputs	FR polarity	$\overline{COL}$	Column data	Measured	Guaranteed
S1 to S40	logic 1	logic 0	logic 1	$\lvert Sx^* - V_{SS} \rvert$	
S1 to S40	logic 0	logic 0	logic 1	$\lvert V_{LCD} - Sx^* \rvert$	$\lvert V_{LCD} - Sx^* \rvert = \lvert Sx^* - V_{SS} \rvert \pm 25\,mV$
S1 to S40	logic 1	logic 0	logic 0	$\lvert V_{LCD} - Sx^* \rvert$	
S1 to S40	logic 0	logic 0	logic 0	$\lvert Sx^* - V_{SS} \rvert$	$\lvert V_{LCD} - Sx^* \rvert = \lvert Sx^* - V_{SS} \rvert \pm 25\,mV$

* Sx = the output no. (i.e. S1 to S40)

Table 4a

Row Drivers

Outputs	FR polarity	$\overline{COL}$	Row data	Measured	Guaranteed
S1 to Sn*	logic 1	logic 1	logic 1	$\lvert V_{LCD} - Sx \rvert$	
S1 to Sn*	logic 0	logic 1	logic 1	$\lvert Sx - V_{SS} \rvert$	$\lvert V_{LCD} - Sx \rvert = \lvert Sx - V_{SS} \rvert \pm 25\,mV$
S1 to Sn*	logic 1	logic 1	logic 0	$\lvert Sx - V_{SS} \rvert$	
S1 to Sn*	logic 0	logic 1	logic 0	$\lvert V_{LCD} - Sx \rvert$	$\lvert V_{LCD} - Sx \rvert = \lvert Sx - V_{SS} \rvert \pm 25\,mV$

* n = the V 6118 version no. (i.e. 2, 4 or 8)

Table 4b

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{LCD} = 2 to 7 V, and T_A = −40°C to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		120			ns
Clock low pulse width	t_{CL}		120			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20[1]			ns
Data input hold time	t_{DH}		30[1]			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF			100	ns
STR pulse width	t_{STR}		100			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		200			ns
FR frequency (Vers. 2/4/8)	F_{FR}[2]			128/256/512		Hz

[1] $t_{DS} + t_{DH}$ minimum must be ≥ 100 ns. If t_{DS} = 20 ns then $t_{DH} \geq 80$ ns.

[2] V 6118 n, FR = n times the desired LCD refresh rate where n is the V 6118 version number.

Table 5a

V_{DD} = 2 to 6 V, V_{LCD} = 2 to 7V and T_A = −40°C to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		500			ns
Clock low pulse width	t_{CL}		500			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		100[1]			ns
Data input hold time	t_{DH}		150[1]			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF			400	ns
STR pulse width	t_{STR}		500			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		1			µs
FR frequency (Vers. 2/4/8)	F_{FR}			128/256/512		Hz

[1] $t_{DS} + t_{DH}$ minimum must be ≥ 500 ns. If t_{DS} = 100 ns then $t_{DH} \geq 400$ ns.

[2] V 6118 n, FR = n times the desired LCD refresh rate where n is the V 6118 version number.

Table 5b

Timing Wafeforms

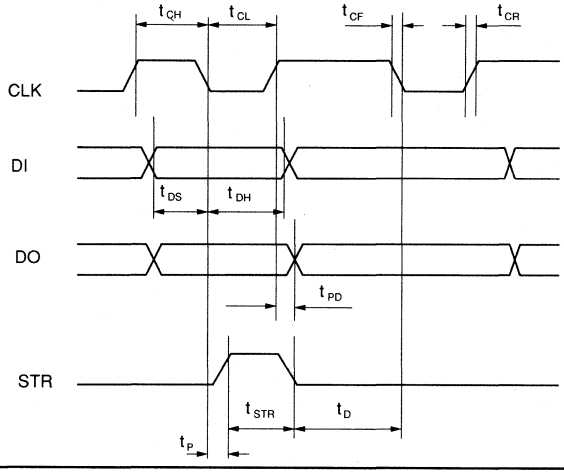
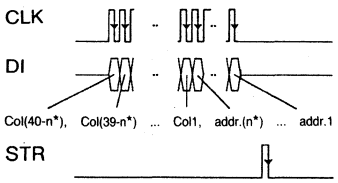


Fig. 3

V 6118 Data Transfer Cycle, $\overline{COL}$ Inactive

V 6118 as a row and column driver ($\overline{COL}$ inactive)
40 bit load cycle, RAM address provided by address bits 1 to (n*)



* n = the V 6118 version no. (i.e. 2, 4 or 8)

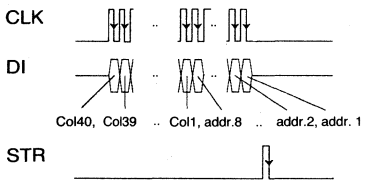
Address Bits			Display RAM	
V 61182	V 61184	V 61188	Addr.	LCD row[1)]
Addr. 1 to Addr. n*				
10	1000	10000000	10000000	Row 1
01	0100	01000000	01000000	Row 2
	0010	00100000	00100000	Row 3
	0001	00010000	00010000	Row 4
		00001000	00001000	Row 5
		00000100	00000100	Row 6
		00000010	00000010	Row 7
		00000001	00000001	Row 8

[1)] A set address bit corresponds to a write enabled RAM address, the same data can be written to more than one RAM address by setting the required address bits.

Fig. 4

V 6118 Data Transfer Cycle, $\overline{COL}$ Active

V 6118 as a column driver only ($\overline{COL}$ active)
48 bit load cycle, RAM address provided by address bits 1 to 8

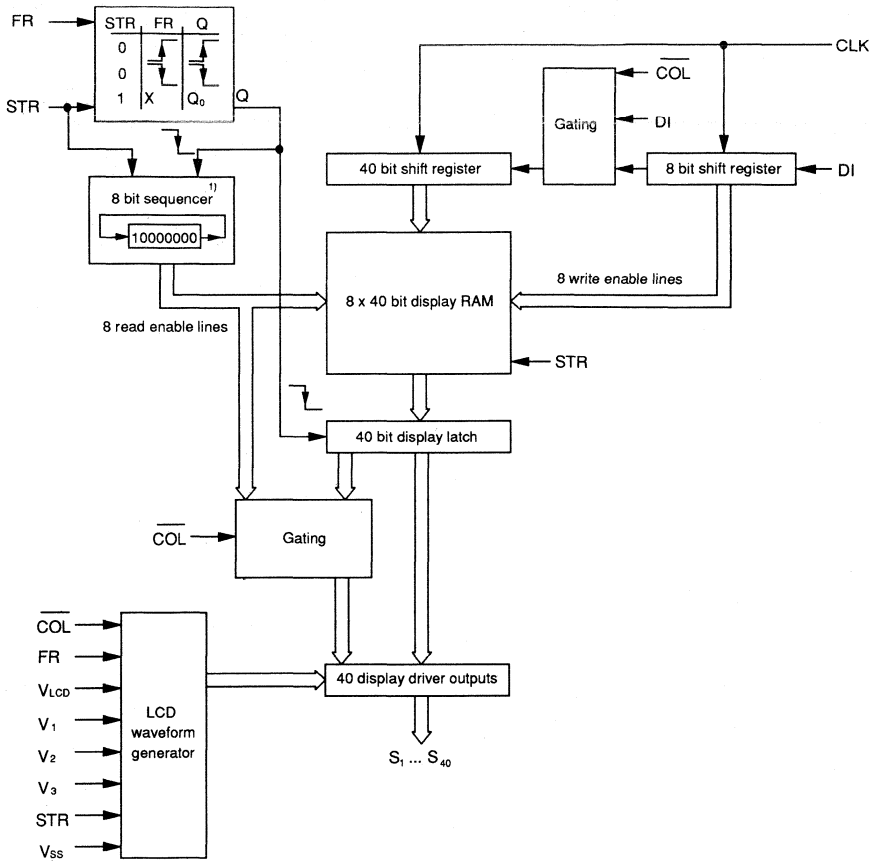


Address Bits			Display RAM	
V 61182	V 61184	V 61188	Addr.	LCD row[1)]
Addr. 1 to Addr. 8				
10000000	10000000	10000000	10000000	Row 1
01000000	01000000	01000000	01000000	Row 2
	00100000	00100000	00100000	Row 3
	00010000	00010000	00010000	Row 4
		00001000	00001000	Row 5
		00000100	00000100	Row 6
		00000010	00000010	Row 7
		00000001	00000001	Row 8

[1)] A set address bit corresponds to a write enabled RAM address, the same data can be written to more than one RAM address by setting the required address bits.

Fig. 5

Block Diagram



1) When logic "1" the STR input forces the display RAM addr. 10000000 (which corresponds to row 1) to be selected by the 8 bit sequences. Cascaded V 6118s are synchronized in this way. The LCD picture is rebuilt starting from row 1 each time data is written to the display RAM.

Fig. 6

Pin Description

Name	Function
S1...S40	LCD outputs, see table 7
V3	LCD voltage bias level 3[1)2)]
V2	LCD voltage bias level 2[1)]
V1	LCD voltage bias level 1[1)]
V_{LCD}	Power supply for the LCD
FR	AC input signal for LCD driver outputs
DI	Serial data input
DO	Serial data output
CLK	Data clock input
STR	Data strobe, blank, synchronize input
V_{DD}	Power supply for logic
$\overline{COL}$	Column only driver mode
V_{SS}	Supply GND

Table 6

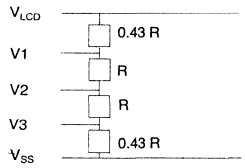
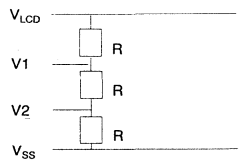
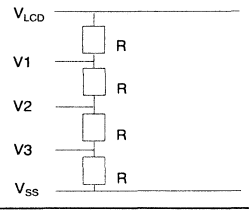
[1)] The V 6118 has internal voltage bias level generation. When driving large pixels, an external resistor divider chain can be connected to the voltage bias level inputs to obtain enhanced display contrast (see Fig. 12, 13 and 14). The external resistor divider ratio should be in accordance with the internal resistor ratio (see table 8).

[2)] V3 is not connected internally on the V 6118 4.

Name	$\overline{COL}$ Inactive			$\overline{COL}$ Active
	V 6118 2	V 6118 4	V 6118 8	
S1	Row1	Row1	Row1	Col1
S2	Row2	Row2	Row2	Col2
S3	Col1	Row3	Row3	Col3
S4	Col2	Row4	Row4	Col4
S5	Col3	Col1	Row5	Col5
S6	Col4	Col2	Row6	Col6
S7	Col5	Col3	Row7	Col7
S8	Col6	Col4	Row8	Col8
S9...S40	Col7...38	Col5...36	Col1...32	Col9...40

Table 7

LCD Voltage Bias Levels

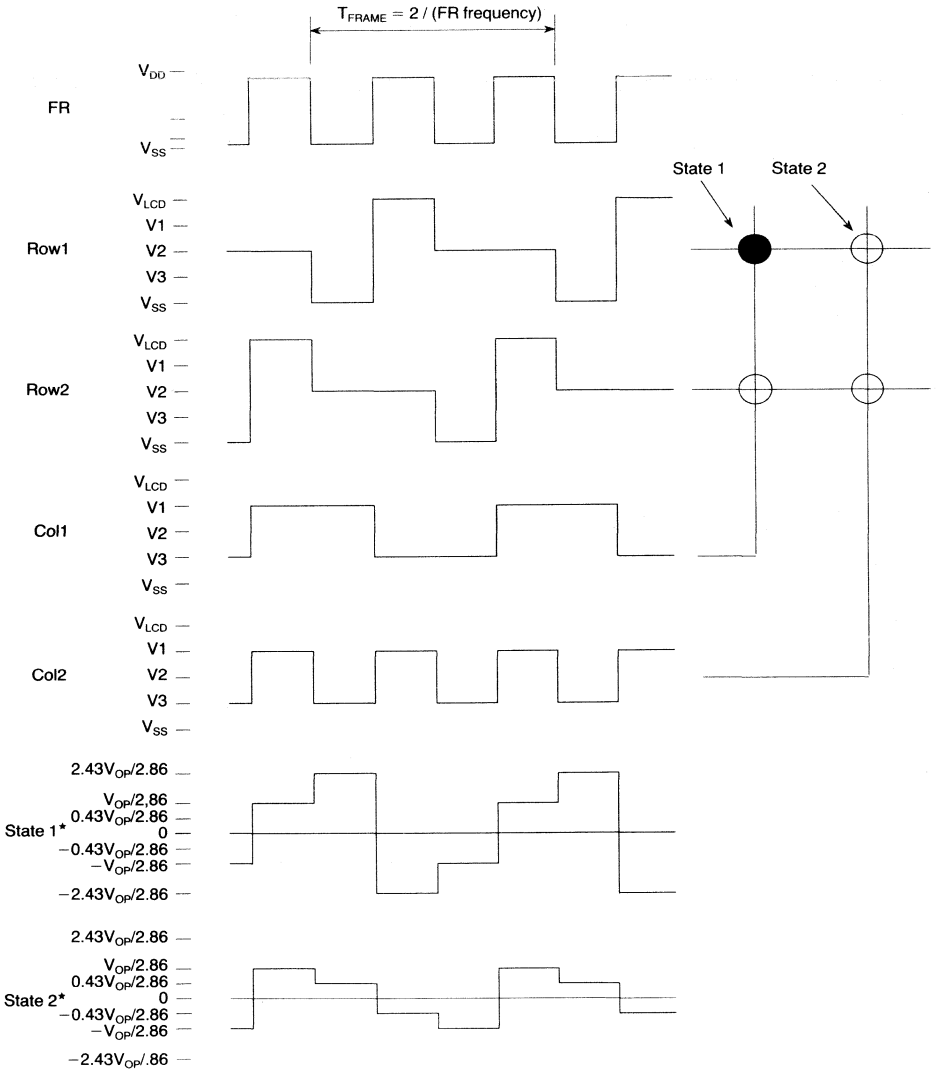
	LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}(*)}{V_{OFF}(rms)}$	$\frac{V_{ON}(rms)}{V_{OFF}(rms)}$
	V 6118 2 n = 2 1 : 2 MUX	Alt + Pleshko 5 levels	$\sqrt{\frac{2n}{1-\sqrt{\frac{1}{n}}}} = 3.69$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 2.41$
	V 6118 4 n = 4 1 : 4 MUX	1/3 Bias 4 levels	3	$\sqrt{1+\frac{8}{n}} = 1.73$
	V 6118 8 n = 8 1 : 8 MUX	1/4 Bias 5 levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n+15}{n+3}} = 1.446$

(*) $V_{OP} = V_{LCD} - V_{SS}$

Table 8

Row and Column Multiplexing Waveform V 6118 2

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

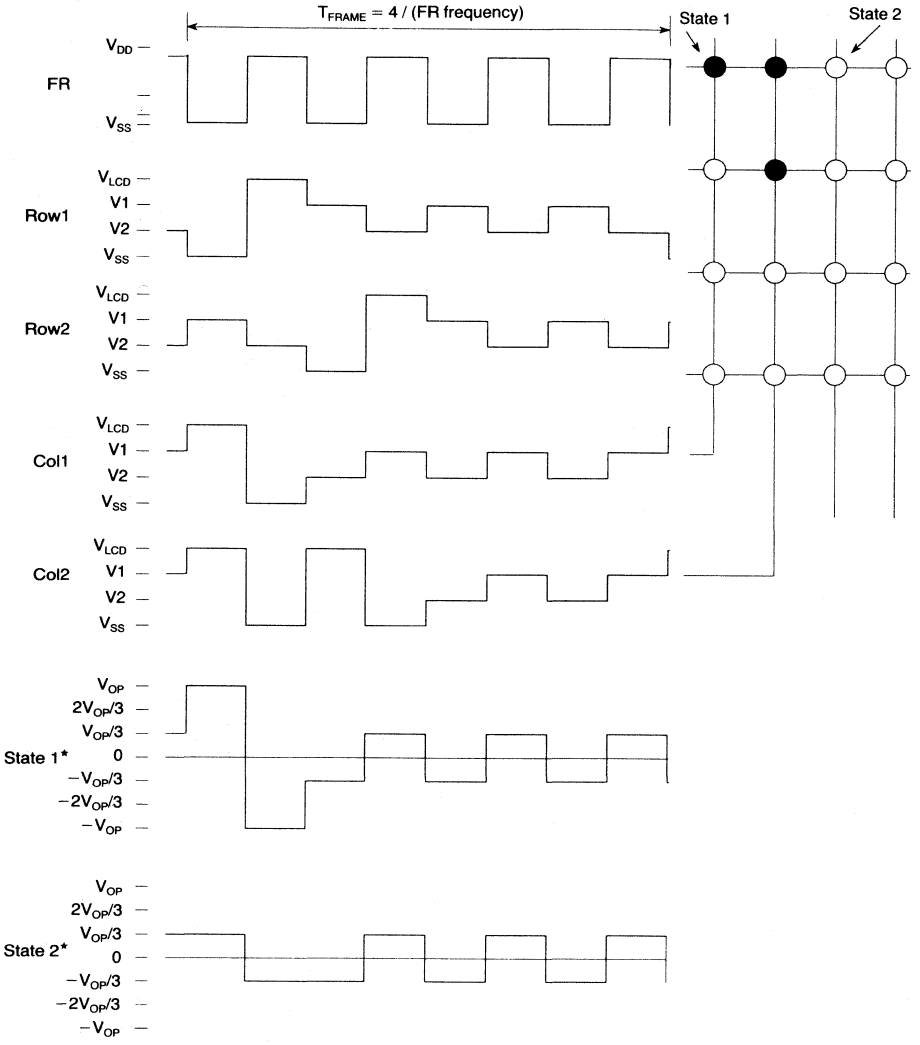


* See table 8

Fig. 7

Row and Column Multiplexing Waveform V 6118 4

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

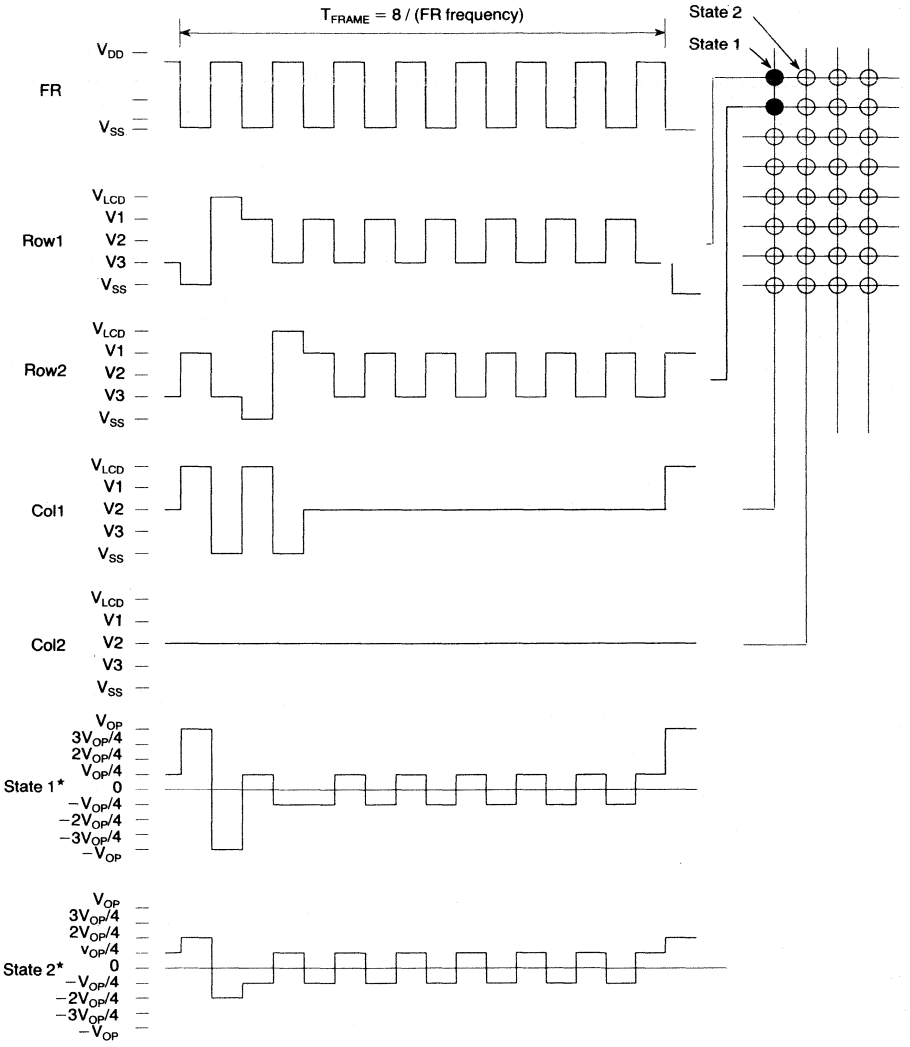


* See table 8

Fig. 8

Row and Column Multiplexing Waveform V 6118 8

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$



* See table 8

Fig. 9

Functional Description

Supply Voltages V_{LCD}, V_{DD}, V_{SS}

The voltage between V_{DD} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{LCD} and V_{SS} is the supply voltage for the LCD and is used for the generation of the internal LCD bias levels. The internal LCD bias levels have a maximum impedance of 25 kΩ for a V_{LCD} voltage from 3 to 7 V. Without external connections to the V1, V2, and V3 bias level inputs, the V 6118 can drive most medium sized LCD.

For displays with a wide variation in pixel sizes the configuration shown in Fig. 13 can give enhanced contrast by giving faster pixel switching times. On changing the row polarity (see Fig. 7, 8 and 9) the parallel capacitors lower the impedance of the bias level generation to the peak current, giving faster pixel charge times and thus a higher RMS "on" value. A higher RMS "on" value can give better contrast. If for a given LCD size and operating voltage, the "off" pixels appear "on", or there is poor contrast, then an external bias level generation circuit can be used with the V 6118. An external bias level generation circuit can lower the bias level impedance and hence improve the LCD contrast (see Fig. 12). The optimum values of R, Rx, and C, vary according to the LCD size used and V_{LCD}. They are best determined through actual experimentation with the LCD.

For LCD with very large average pixel size (eg. 25 mm^2) the bias level configuration shown in Fig. 14 should be used.

When V 6118s are cascaded connect the V1, V2, and V3 bias inputs as shown in Fig. 10. The pixel load is averaged across all the cascaded drivers. This will give enhanced display contrast as the effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V 6118 are cascaded as shown in Fig. 10, then the maximum bias level impedance becomes 12.5 kΩ for a V_{LCD} voltage from 3 to 7 V.

Table 8 shows the relationship between V1, V2, and V3 for the multiplex rates 2, 4 and 8. Note that $V_{LCD} > V1 > V2 > V3$ for the V 6118 2 and V 6118 8, and for the V 6118 4, $V_{LCD} > V1 > V2$.

Data Input / Output

The data input pin, DI, is used to load serial data into the V 6118. The serial data word length is 40 bits when $\overline{COL}$ is inactive, and 48 bits when it is active. Data is loaded in inverse numerical order, the data for bit 40 (bit 48 when $\overline{COL}$ is active) is loaded first with the data for bit 1 last. The column data bits are loaded first and then the address bits (see Fig. 4 and 5).

The data output pin, DO, is used in cascaded applications (see Fig. 10). DO transfers the data to the next cascaded chip. The data at DO is equal to the data at DI delayed by 40 clock periods, when $\overline{COL}$ is inactive, and 48 clock periods when $\overline{COL}$ is active. In order to cascade V 6118s, the DO of one chip must be connected to DI of the following chip (see Fig. 10). In cascaded applications the data for the last V 6118 (the one that does not have DO connected) must be loaded first and the data for the first V 6118 (its DI is connected to the processor) loaded last (see Fig. 10).

The display RAM word length is 40 bits (see Fig. 6). Each LCD row has a corresponding display RAM address which provides the column data (on or off) when the row is selected (on). When down loading data to the V 6118 any display RAM address can be chosen, there is no display RAM addressing sequence (see Fig. 4 and 5).

The same data can be written to more than one display RAM address. If more than one address bit is set, then more than one display RAM address is write enabled, and so the same data is written to more than one address. This feature can be useful to flash the LCD on and off under software control. If the address bits are all zero then no display RAM address is write enabled and no data is written to the display RAM on the falling edge of STR. Use address 0 to synchronize cascaded V 6118s without updating the display RAM.

CLK Input

The CLK input is used to clock the DI serial data into the shift register and to clock the DO serial data out. Loading, shifting and outputting of the data occurs at the falling edge of this clock (see Fig. 3). When cascading devices, all CLK lines should be tied together (see Fig. 10).

STR Input

The STR input is used to write to the display RAM, blank the LCD, and synchronize cascaded V 6118s. The STR input writes the data loaded into the shift register, on the DI input, to the display RAM on the falling edge of the STR signal. The display RAM address is given by the address bits (see Fig. 4 and 5).

The STR input when high blanks the LCD by disconnecting the internal voltage bias generation from the V_{SS} potential. Segment outputs S1 to S40 (rows and columns) are pulled up to V_{LCD}. The delay to driving the LCD with V_{LCD} on S1 to S40, is dependent on the capacitive load of the LCD and is typically 1 μs. An LCD pixel responds to RMS voltage and takes approximately 100 ms to turn on or off. The delay from putting STR high to the LCD being blank is dependent on the LCD off time and is typically 100 ms. In applications which have a long STR pulse width (10 μs) the LCD is driven by V_{LCD} on both the rows and columns during this time. As the time is short (1 μA), it will have zero measurable effect on the RMS "on" value (over 100 ms) of an LCD pixel and also zero measurable effect on the pixel DC component. Such STR pulses will not be visible to the human eye on an LCD.

Note if an external voltage bias generation circuit is used as shown in Fig. 12 and 14, the LCD blank function (STR high) will not blank the LCD. When STR is high the LCD will be driven by the parallel combination of the external voltage bias generation circuit and part of the internal voltage bias generation circuit.

The STR input, when high, synchronizes cascaded V 6118s by forcing a new time frame to begin at the next falling edge of the FR input signal (see Fig. 6). A time frame begins with row 1 and so the LCD picture is rebuilt from row 1 each time cascaded V 6118s are synchroniz-

ed. When cascading devices, all STR lines must be tied together (see Fig. 10).

FR Input

The FR signal controls the segment output frequency generation (see Fig. 7, 8 and 9). To avoid having DC on the display, the FR signal must have a 50% duty cycle. The frequency of the FR signal must be n times the desired display refresh rate, where n is the V 6118 version no. (2, 4 or 8). For example, if the desired refresh rate is 40 Hz, the FR signal frequency must be 320 Hz for the V 6118 8. A selected row (on) is in phase with the FR signal (see Fig. 7, 8, and 9).

It is recommended that data transfer to the V 6118 should be synchronized to the FR signal to avoid a falling or rising edge on the FR signal while writing data to the V 6118. The LCD pixels change polarity with the FR signal. On the edges of the FR signal current spikes will appear on the V_{SS} and V_{LCD} supply lines. If the supply lines have high impedance then voltage spikes will appear. These voltage spikes could interfere with data loading on the DI and CLK pins.

Driver Outputs S1 to S40

There are 40 LCD driver outputs on the V 6118. When $\overline{COL}$ is inactive the outputs S1 to Sn function as row drivers and the outputs S(n + 1) to S40 function as column drivers, where n is the V 6118 version no. (2, 4 or 8). When $\overline{COL}$ is active all 40 outputs function as column drivers (see table 6). There is a one to one relationship between the display RAM and the LCD driver outputs. Each pixel (segment) driven by the V 6118 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the segment "on" and clearing it turns it "off".

$\overline{COL}$ Input

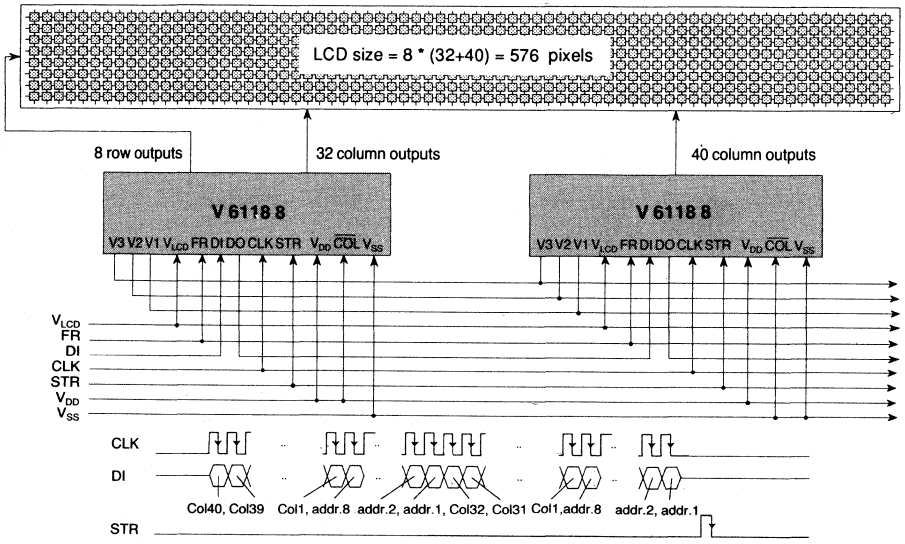
The V 6118 functions as a row and column driver while the $\overline{COL}$ input is inactive. When active the $\overline{COL}$ input configures the V 6118 to function as a column driver only. The former row outputs function as column outputs. In cascaded applications one V 6118 should be used in the row and column configuration ($\overline{COL}$ inactive) and the rest as pure column drivers ($\overline{COL}$ active) (see Fig. 10). Note when cascading V 6118s never cascade one version with another. If a V 6118 8 is used to drive the rows then only V 6118 8s can be cascaded with it. When $\overline{COL}$ is active the V 6118 needs 48 bits of data in a load cycle. 40 bits are used for the column data and 8 bits to address the display RAM regardless of V 6118 version (2, 4 or 8) (see Fig. 4, 5 and 10).

Power Up

On power up the data in the shift registers, the display RAM and the 40 bit display latch are undefined. The STR input should be taken high on power up to blank the display, and then the display data written to the display RAM (see Fig. 11). When finished the initial write to the display RAM, take the STR input low to display the display RAM contents (see also section "STR Input").

Applications

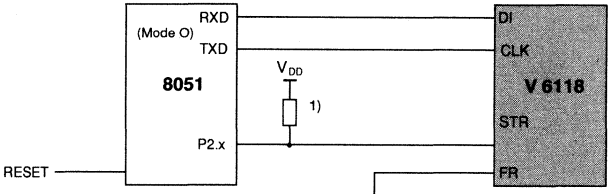
Two V 6118 8s Cascaded



By connecting the V1, V2 and V3 bias inputs as shown, the pixel load is averaged across all the drivers. The effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V 6118 are cascaded as above, then the maximum bias level impedance becomes 12.5 kΩ.

Fig. 10

Microprocessor Interface and LCD Blanking



[1] When the microprocessor is reset, the port pin will be configured as an input and so the STR line would float. The pullup resistor will ensure that the LCD is blank while the system reset line is active and after until the port pin is setup by software.

Writing Data to the Display RAM while Keeping the LCD Blank

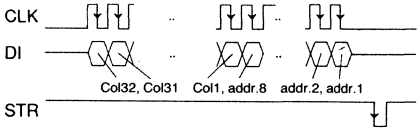
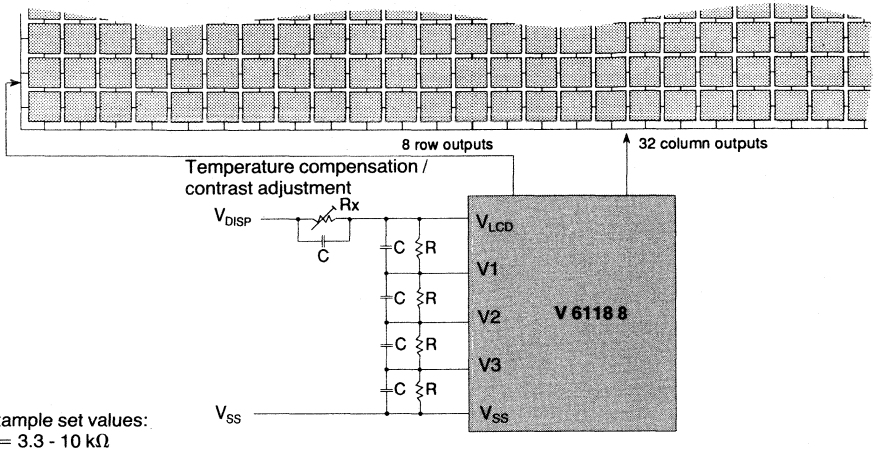


Fig. 11

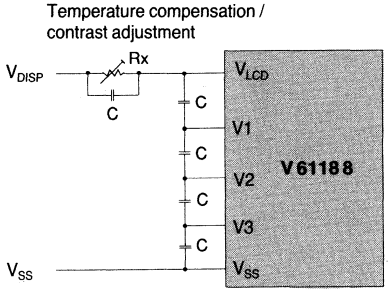
V 6118 with External Resistor Divider Bias Generation



Example set values:
R = 3.3 - 10 kΩ
C = 2.2 - 47 nF
Rx is given by the formula:
$Rx = 4R\ ((V_{DISP}/V_{LCD}) - 1) = 10 - 30\ k\Omega$

Fig. 12

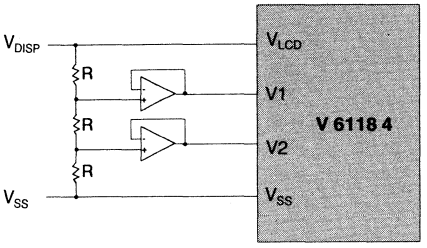
Enhanced Switching from the V 6118



C = 1 μF
Rx is given by the formula:
$Rx = 4\ (20\ k\Omega)\ ((V_{DISP}/V_{LCD}) - 1)$

Fig. 13

Bias Configuration for a Large LCD

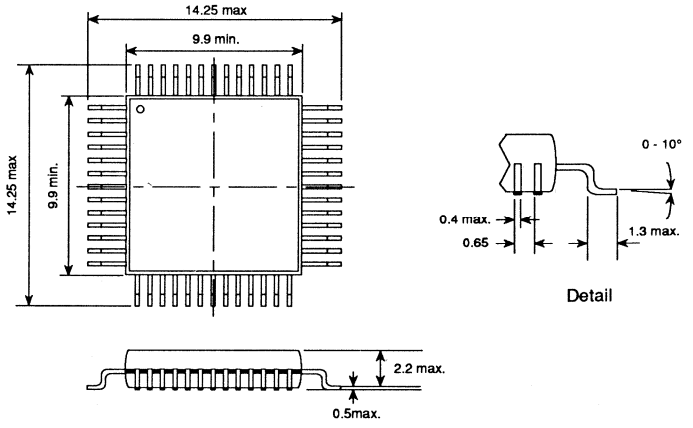


Large LCD example:
V_{OP} = 5V, average pixel active area = 25 mm^2,
display refresh rate = 30 Hz

For a single V 6118 4 driving such an LCD the voltage follower buffer (opamp) requirement is:
peak current 1.8 mA,
steady state current typically 100 μA

Fig. 14

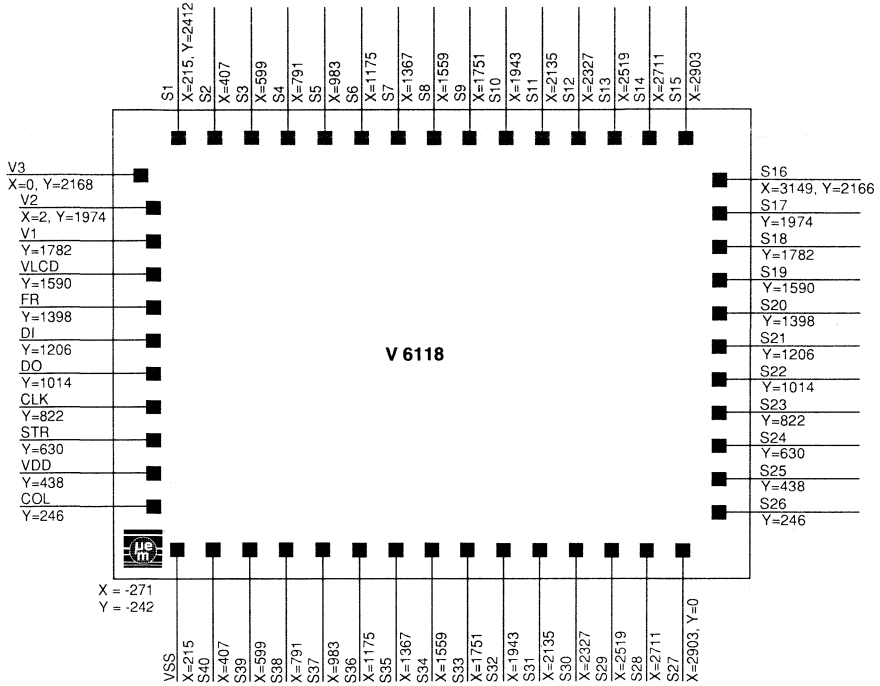
Dimensions of QFP Package



Dimensions in mm

Fig. 16

Dimensions of Chip Form



Thickness (typ.) = 11 mils
Chip size is X = 3657 by Y = 2895 microns or X = 144 by Y = 114 mils
Note: The origin (0,0) is the lower left coordinate of center pads.
The lower left corner of the chip shows distances to origin.

Dimensions in microns

Fig. 17

Ordering Information

The V 6118 is available in the following packages:

QFP52, pin plastic package	V 6118 2 52F
	V 6118 4 52F
	V 6118 8 52F
TAB, tape automated bonding	V 6118 2 TAB
	V 6118 4 TAB
	V 6118 8 TAB

Chip form	V 6118 2 Chip*
	V 6118 4 Chip*
	V 6118 8 Chip*

* on request

When ordering, please specify the complete part number and package.

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Table of Contents

Real Time Clock Circuit

Features

- Battery pin, bus disabled on power down
- Easy to use like a RAM with fast access time
- Interface compatible with both Intel and Motorola microprocessors
- TTL/CMOS compatible
- Standby on power down typically 5 μA
- Chrono and alarm time interrupt
- Can be synchronized to a master clock pulse
- Pulse output once per second, minute or hour
- $\overline{\text{BUSY}}$ pin can be used as a 1 Hz strobe for display control
- BCD data format
- Leap-year and auto roll-over of week number
- Packages DIP 16 and SO 16
- $\overline{\text{SYNC}}$ pin to tune the device to an external time reference
- Frequency tuning and test modes

Description

The M 3002 is a monolithic low power CMOS device which functions as a 4 bit real time clock. The device is accessed by chip select ($\overline{\text{CS}}$) with read and write function timing provided by $\overline{\text{OE}}$ and R/$\overline{\text{W}}$. The M 3002 is driven by an external 32.768 kHz crystal, and uses the 24 hour system. An alarm can be preprogrammed up to one month in advance. The timer can measure elapsed time up to 24 hours. Time data is stored in a 15 by 8 bit RAM in BCD format. An 8 bit status word in the RAM controls the mode of operation.

Applications

- Single board computers
- Industrial controllers
- PABX and telephone systems
- Taximeters, lorry tachos
- Data loggers

Typical Operating Configuration

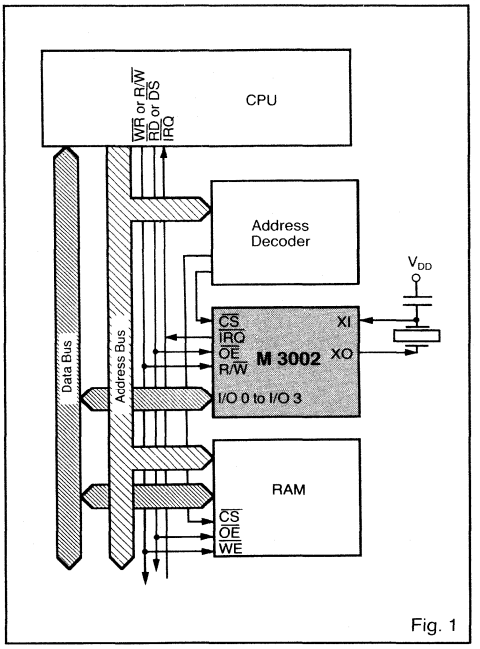


Fig. 1

Pin Assignment

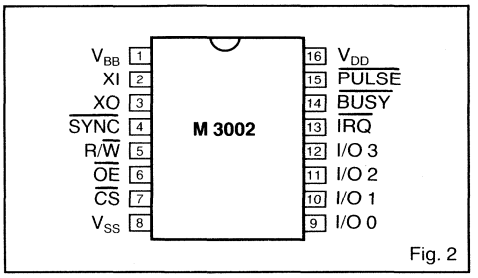


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	$V_{DD\,max}$	V_{SS} + 8.0 V
Minimum voltage at V_{DD}	$V_{DD\,min}$	V_{SS} − 0.3 V
Maximum voltage at XI and XO	V_{max}	V_{DD} + 0.3 V
Minimum voltage at XI and XO	V_{min}	V_{BB} − 0.3 V
Max. voltage at any signal pin	V_{max}	V_{DD} + 0.3 V
Min. voltage at any signal pin	V_{min}	V_{SS} − 0.3 V
Maximum storage temperature	T_{STOmax}	+ 150°C
Minimum storage temperature	T_{STOmin}	−65°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	+2.4	+5.0	+5.5	V
Battery voltage[1]	$V_{DD}-V_{BB}$	+2.4		+5.0	V
Crystal Characteristics					
Frequency[2]	f		32.768		kHz
Load capacitance	C_L	8	10	13	pF
Series resistance	R_S		20	50	kΩ
Trimmer capacitance	C_T	5	15	40	pF

[1] See Fig. 10 and Fig. 11
[2] Parallel resonant crystal

Table 2

Electrical Characteristics

V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = 3.0 V, and T_A = 0°C to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Total static supply	I_{DD}	all outputs open, all inputs at V_{DD}			10	µA
Standby current	I_{BB}	V_{DD} = 0 V		5	8	µA
Inputs and Outputs						
Input logic low	V_{IL}		0.0		0.8	V
Input logic high	V_{IH}		2.4		5.0	V
Pullup on $\overline{OE}$ and $\overline{SYNC}$ pins	I_L	V_{IL} = 0.8 V	30			µA
Output logic low on I/O pins	V_{OL}	I_{OL} = 3.2 mA			0.4	V
Output logic low	V_{OL}				0.4	V
Output logic high on I/O pins	V_{OH}	I_{OH} = 2 mA	2.4			V
Output logic high on $\overline{IRQ}$	V_{OH}	100k pullup to V_{DD}	2.4			V
Output logic high	V_{OH}		2.4			V
Input leakage	I_{IN}	0.0 < V_{IN} < 5.0			1	µA
Oscillator						
Starting voltage	V_{STA}	C_T = 18pF	1.8			V
Input capacitance on XI	C_{IN}			3.7		pF
Output capacitance on XO	C_{OUT}			25		pF
Start-up time	T_{STA}	C_T = 18pF		0.6	5	s
Frequency stability	△f/f	2.0 ≤ V_{BB} ≤ 5.0 V C_T = 5 pF		5	10	ppm/V

Table 3

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = 3.0 V, and T_A = 0°C to +70°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Chip select duration	t_{CS}		280			ns
RAM access time[1]	t_{ACC}			150	270	ns
Time between two transfers	t_W		1000			ns
Data valid to Hi-impedance[2]	t_{DF}			180	300	ns
Write data settle time[3]	t_{DW}		200			ns
Data hold time[4]	t_{DH}		0			ns

Table 4

[1] t_{ACC} starts from $\overline{OE}$ or $\overline{CS}$, whichever activates last.
[2] t_{DF} starts from $\overline{OE}$ or $\overline{CS}$, whichever deactivates first.
[3] t_{DW} ends at R/$\overline{W}$ or $\overline{CS}$, whichever deactivates first.
[4] t_{DH} starts from R/$\overline{W}$ or $\overline{CS}$, whichever deactivates first.

4

Timing Waveforms

Read Timing for Both Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola (Advanced R/$\overline{W}$ with $\overline{OE}$ Tied to $\overline{CS}$)

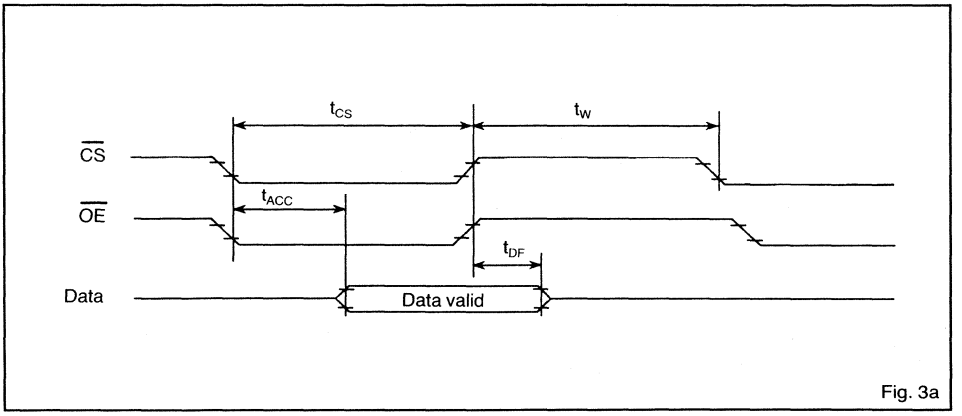


Fig. 3a

Write Timing for Both Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola (Advanced R/$\overline{W}$ with $\overline{OE}$ Tied to $\overline{CS}$)

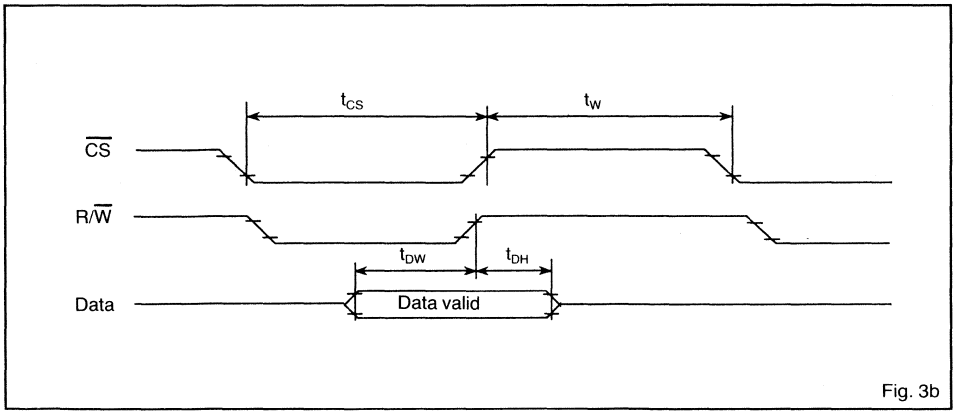


Fig. 3b

Block Diagram

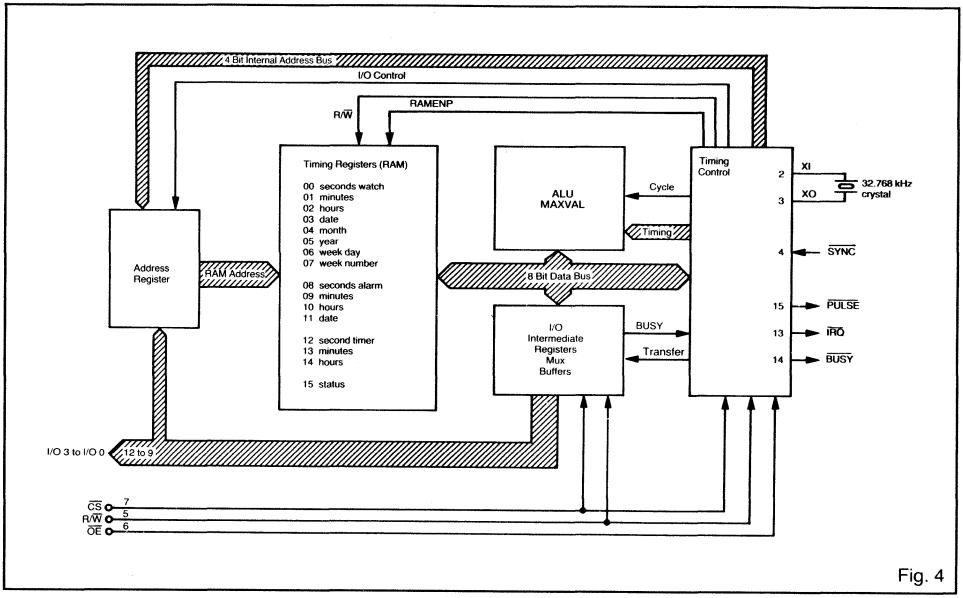


Fig. 4

Pin Description

Pin	Name	Function
1	V_{BB}	Negative battery terminal
2	XI	32.768 kHz quartz input
3	XO	32.768 kHz quartz output
4	$\overline{SYNC}$	Time synchronization input (internal pullup)
5	R/$\overline{W}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola), see Fig. 10 and 11
6	$\overline{OE}$	$\overline{RD}$ (Intel), see Fig. 10 and 11 (internal pullup)
7	$\overline{CS}$	Chip select input
8	V_{SS}	Ground terminal
9	I/O 0	Data bus input/output lines Address bus input lines
10	I/O 1	
11	I/O 2	
12	I/O 3	
13	$\overline{IRQ}$	Interrupt request output (open drain with internal pullup)
14	$\overline{BUSY}$	Internal update cycle status output
15	$\overline{PULSE}$	Programmable timing pulse output
16	V_{DD}	Positive supply terminal (substrate)

Table 5

Functional Description

Power Supply and Data Retention

The M 3002 can be powered with a supply voltage between 2.4 and 5.5 V, and backed up with a battery or supercap (2.4 to 5.0 V), as indicated in Fig. 10 and 11, to ensure operation and data retention during power-down. Because of the low power consumption of the device, lithium cells or standard rechargeable cells give many years of effective life. If the battery is not required then connect V_{BB} to V_{SS}. When the voltage at the V_{BB} pin drops below the voltage at the V_{SS} pin, access to the device is disabled. The I/O lines and the outputs $\overline{BUSY}$ and $\overline{PULSE}$ are set to a high impedance state. The open-drain output $\overline{IRQ}$ will be inactive until V_{DD} is restored. Care should be taken to avoid the occurance of improper states on interfacing signal lines.

RAM

The 16 x 8 RAM is used to store all clock, alarm, timer and status data. The allocation of RAM addresses is shown in Table 6. All time data are stored in Binary Coded Decimal (BCD) format. The transfer of this data between the internal 8-bit bus and the I/O lines is performed by the bidirectional I/O buffer (see Block Diagram Fig. 4). If the alarm and timer functions are not needed, then the RAM section from these functions, addresses 8 to E hex, may be used as non-volatile system storage by software. It should be noted however that, if the unused function is inadvertently activated by altering the status word, the

stored data may be modified.

I/O Address Locations

Address Hex	Address Dec	Data	Group	Max. Value	Operations
0	0	Seconds	Watch	59	Time data
1	1	Minutes		59	incremented
2	2	Hours		23	under control of
3	3	Date		28, 29, 30, 31	status bit 0
4	4	Month		12	
5	5	Year		99	
6	6	Week day		07	
7	7	Week no.		53	
8	8	Seconds	Alarm	59	Alarm data,
9	9	Minutes		59	providing an IRQ
A	10	Hours		23	under control of
B	11	Date		28, 29, 30, 31	status bit 1
C	12	Seconds	Timer	59	Timer data
D	13	Minutes		59	incremented
E	14	Hours		23	under control of status bit 4
F	15	Status	Status		Control

Table 6

Status and Control

The function of the individual bits of the status word are shown in Table 7. The status word, address F hex, controls the timekeeping functions performed in the ALU section of the M 3002 (see Block Diagram Fig. 4). The status word must be written on recovery from a total power loss, V_{DD} and the battery voltage < 2.4 V.

Status Word

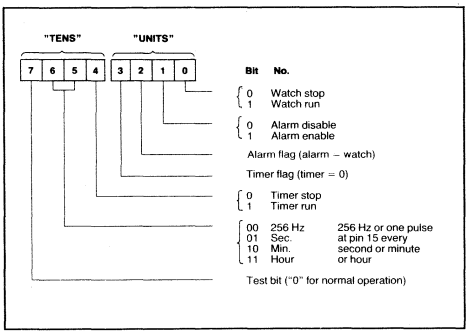


Table 7

RAM Access

The interface between the M 3002 and the host microprocessor consists of four bidirectional multiplexed data/address lines (I/O lines), three control lines ($\overline{CS}$, $\overline{OE}$, R/$\overline{W}$), and an interrupt request line ($\overline{IRQ}$). Three steps are required to access a RAM address. The first access transfers the 4-bit address of the data location, the second reads or writes data bits 7 to 4 (tens) to or from the address written in step one, and the third reads or writes data bits 3 to 0 (units). Fig. 5 shows the 3 step access sequence.

3 Step Access Sequence

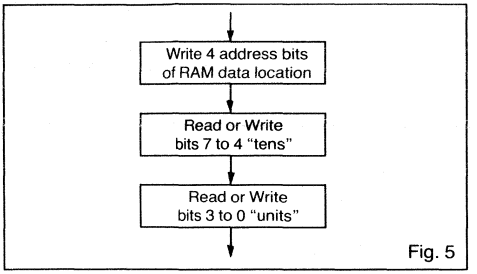


Fig. 5

An internal multiplexer defines the 3 step access sequence position. A 3 step access sequence is began by writing the RAM 4-bit address and then the M 3002 treats the next two accesses as the 4-bit data transfers, tens first, units second. A read access, while the multiplexer is expecting an address write, will not begin a 3 step access sequence. The multiplexer can be initialized (expecting an address write) by two read accesses. Read accesses will complete a 3 step access sequence, but will not begin one. The multiplexer must be initialized by software on every power up of the system including power up of the M 3002 from a power loss (V_{DD} and the battery voltage < 2.4 V) condition.

RAM Access and Internal Update Cycles

Every second an internal update occurs and lasts between 0.73 ms and 6 ms. During this update cycle, the multiplexer is initialized, the $\overline{BUSY}$ output is active, and a read will give F hex on the I/O pins. The RAM is allocated to the ALU (see Block Diagram Fig. 4). If an external data transfer is in progress (see RAM Access section), the internal update cycle is delayed for a maximum of one second. After a delay of one second the external data transfer will be aborted and the RAM assigned to the internal update cycle. With the multiplexer in its initial state, reading the M 3002 will give 0 hex if an internal update cycle is not in progress and F hex if in progress. Thus prior to beginning a 3 step access sequence, software must read the I/O pins to determine if the RAM is available. Additionally the $\overline{BUSY}$ pin goes active while an internal update cycle is in progress. To prevent an update during a sequence of transfers, for example hours, minutes and seconds, there must be less than 2 ms between each transfer (i.e. 3 step access sequence). If software continuously polls the M 3002 to seek an event or refresh a display then the delay between two poll sequences (e.g. read hours, minutes, seconds) should be greater than 6 ms to allow an update cycle to occur.

RAM Access and Interrupts

Any false or aborted access will make the M 3002 jump incorrectly to the next step in the 3 step access sequence. Access to the M 3002 is not re-entrant and so

the software routine accessing the M 3002 must complete the 3 step access sequence before another software routine can access the device. Interrupt software routines must not access the M 3002 unless it can be guaranteed that the M 3002 is not in a 3 step access sequence. Additionally interrupt software routines must not delay the 3 step access sequence in the background routine longer than one second or an internal update cycle will occur within the M 3002. It is recommended that all software routines reading or writing to the M 3002 call one of the software routine structures, shown in Fig. 6, for each device access.

M 3002 Software Access Routines

```
M 3002 __ WRITE:
    Disable maskable interrupts
        Wait for Bus = 0 hex
        Write address to M 3002
        Write data bits 7 to 4 to M 3002
        Write data bits 3 to 0 to M 3002
    Enable maskable interrupts

M 3002 __ READ:
    Disable maskable interrupts
        Wait for Bus = 0 hex
        Write address to M 3002
        Read data bits 7 to 4 from M 3002
        Read data bits 3 to 0 from M 3002
    Enable maskable interrupts
```

Fig. 6

Non maskable interrupt routines must not access the M 3002 as it cannot be guaranteed that the M 3002 is not in the middle of a 3 step access sequence. In a multitasking software environment the task accessing the M 3002 must not be interrupted during a 3 step access sequence.

Alarm and $\overline{IRQ}$

An alarm date and time may be preset in RAM addresses 8 to B hex. During every update cycle, the ALU (see Block Diagram Fig. 4) compares the contents of the watch addresses, 0 to 3 hex, with the preset alarm time data. If the alarm is enabled (status word bit 1) and the alarm time data matches the watch addresses 0 to 3 hex, the $\overline{IRQ}$ pin goes active and the alarm flag (status word bit 2) is set to indicate to the software the source of the interrupt. $\overline{IRQ}$ will remain active until the software acknowledges the interrupt by clearing the alarm flag (status word bit 2). If the alarm is enabled (status word bit 1), and an alarm RAM location set to FF hex, this location is not compared with the associated watch location. Thus it is possible to achieve a repeat feature where an alarm occurs every programmed number of, seconds, or seconds and minutes, or seconds, minutes and hours. The M 3002 does not generate interrupts until the 3 step access sequence is complete.

Timer and $\overline{IRQ}$

By setting the status word bit 4 (timer enable bit), the preset time data in RAM addresses C hex to E hex, increments every second with the update cycle. When passing from 23:59:59 to 00:00:00, the timer flag (status word bit 3) is set and the $\overline{IRQ}$ output goes active. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the timer flag (status word bit 3). The M 3002 does not generate interrupts until the 3 step access sequence is complete.

$\overline{PULSE}$ Output

The $\overline{PULSE}$ output can be programmed with bits 5 and 6 of the status word, as shown in Table 7, to produce a negative pulse of 64 μs duration, every second, minute, or hour, while the watch is running. Clearing bits 5 and 6 of the status word will produce a 256 Hz square wave on the $\overline{PULSE}$ pin. The latter feature is intended for frequency tuning, see section Frequency Tuning.

$\overline{SYNC}$ Input

If the $\overline{SYNC}$ input is set low for longer than 200 μs, the watch will synchronize to the falling edge of this $\overline{SYNC}$ signal with a precision of $\pm$ 2 ms. The seconds RAM location (address 0 hex) will be cleared and if the contents were $\geq$ 30, the minutes location (address 1 hex) will be incremented.

Frequency Tuning

The $\overline{PULSE}$ pin will output a 256 Hz square wave signal if the bits 5 and 6 of the status word are cleared. The period of the signal on the $\overline{PULSE}$ pin can be adjusted by the crystal trimmer. The nominal period for 256 Hz is 3.90625 ms (see Fig. 7)

Calibration Circuit

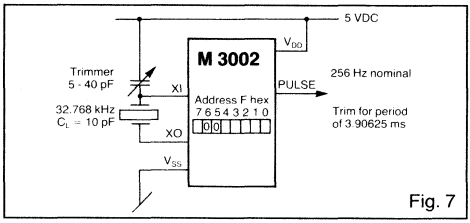


Fig. 7

Crystal Layout

In order to ensure proper oscillator operation we recommend the following standard practices.

- Keep traces as short as possible
- Use a guard ring around the crystal and capacitor or trimmer.

Fig. 8 shows the recommended layout.

P.C.B. Layout

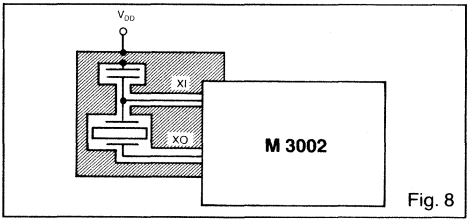


Fig. 8

Test

Some of the various test features added to the M 3002, some can be activated by software. Table 8 shows the available test modes and how they may be activated.

Test Modes

Status bit 7	Status bit 5	$\overline{\text{SYNC}}$ input	Function
0	0	V_{SS}	Normal operation
1	0	V_{SS}	First 5 stages of divider chain bypassed: acceleration by a factor of 32[1]
1	1	V_{SS}	Parallel increment of all time and timer data at 1 Hz depending on the status of bit 0 and bit 4[2]
1	1	V_{DD}	Parallel increment of all time and timer data at 32 Hz depending on the status of bit 0 and bit 4 First 5 stages of divider chain bypassed: thus acceleration by a factor of 32[1]

[1] External signal generator to be used
[2] Crystal or extended signal generator

Table 8

An external signal generator can be used to drive the M 3002. Fig. 9 shows how to connect the signal generator. The speed can be increased by increasing the signal generator frequency to a maximum of 128 kHz. Test modes can be activated while using an external signal generator if required. To leave test, the test bit (status word bit 7) must be cleared by software. Test corrupts the watch and timer data and so all parameters should be reloaded after a test session.

Signal Generator Connection

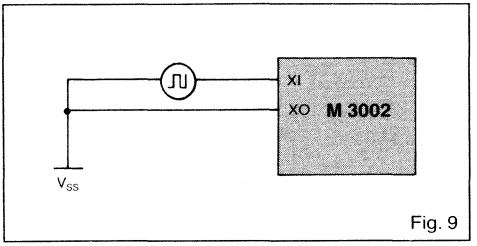


Fig. 9

Typical Application

Intel Microprocessor Interfaced with the M 3002 in a Typical Configuration

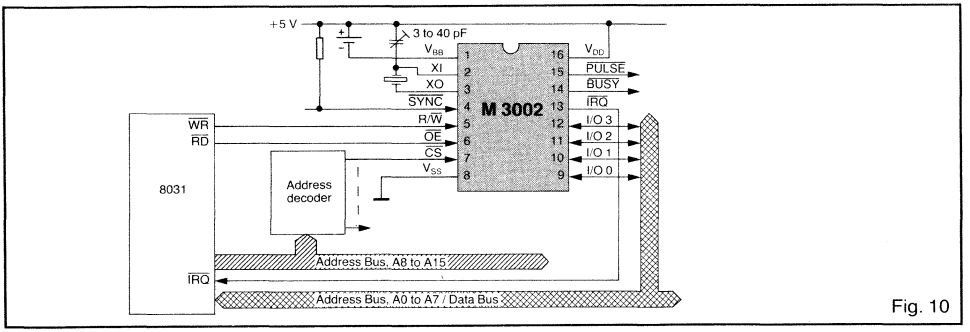
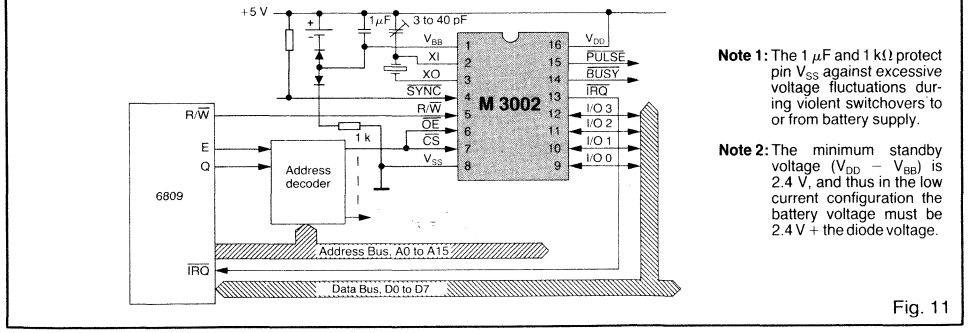


Fig. 10

Motorola Microprocessor Interfaced with the M 3002 in a Low Battery Current Configuration



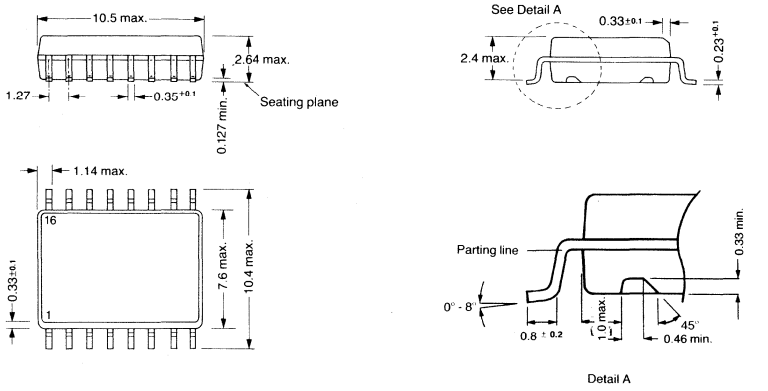
Note 1: The 1 µF and 1 kΩ protect pin V_{SS} against excessive voltage fluctuations during violent switchovers to or from battery supply.

Note 2: The minimum standby voltage (V_{DD} – V_{BB}) is 2.4 V, and thus in the low current configuration the battery voltage must be 2.4 V + the diode voltage.

Fig. 11

Package and Ordering Information

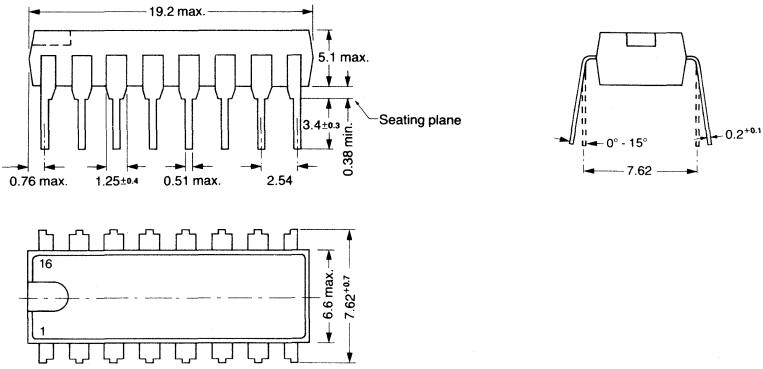
Dimensions of SO Package



Dimensions in mm

Fig. 12

Dimensions of DIP Package



Dimensions in mm

Fig. 13

Ordering Information

The M 3002 is available in the following packages:

DIP 16-pin plastic package	M 3002 16P
SO 16-pin wide plastic package	M 3002 16S

Chip form on request.

When ordering, please specify the complete part number and package.

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Real Time Clock Circuit

Features

- Easy to use like a RAM with fast access time
- Interface compatible with both Intel and Motorola microprocessors
- TTL/CMOS compatible
- Standby on power down typically 5 μA
- Chrono and alarm time interrupt
- Sleep mode capability
- Can be synchronized to a master clock pulse
- Pulse output once per second, minute or hour
- $\overline{\text{BUSY}}$ pin can be used as a 1 Hz strobe for display control
- BCD data format
- Leap-year and auto roll-over of week number
- Packages DIP 16 and SO 16
- $\overline{\text{SYNC}}$ pin to tune the device to an external time reference
- Frequency tuning and test modes

Description

The M 3003 is a monolithic low power CMOS device which functions as a 4 bit real time clock. The device is accessed by chip select ($\overline{\text{CS}}$) with read and write function timing provided by $\overline{\text{OE}}$ and R/$\overline{\text{W}}$. The M 3003 is driven by an external 32.768 kHz crystal, and uses the 24 hour system. An alarm can be preprogrammed up to one month in advance, and, even in standby, the M 3003 pulls the IRQ pin active low on an internal alarm interrupt. The timer can measure elapsed time up to 24 hours. Time data is stored in a 15 by 8 bit RAM in BCD format. An 8 bit status word in the RAM controls the mode of operation.

Applications

- Single board computers
- Industrial controllers
- PABX and telephone systems
- Taximeters, lorry tachos
- Data loggers

Typical Operating Configuration

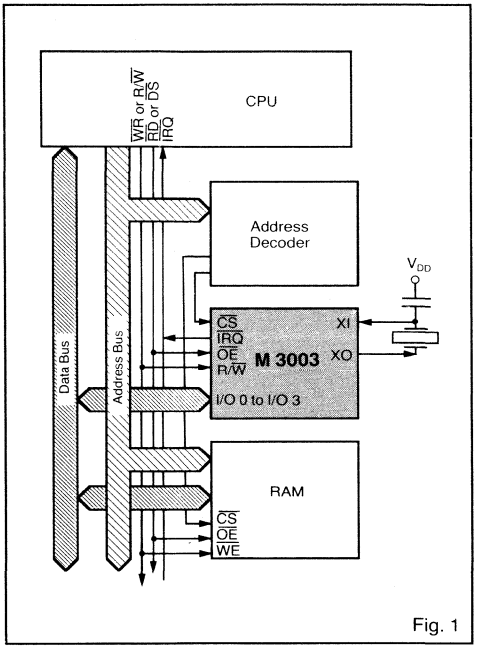


Fig. 1

Pin Assignment

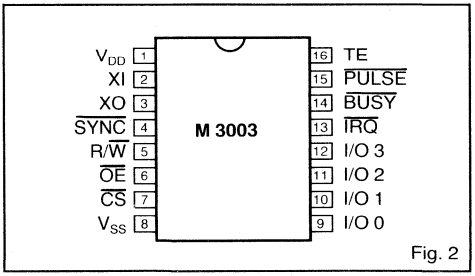


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Max. voltage at V_{DD} and IRQ	$V_{DD\,max}$	V_{SS} + 8.0 V
Min. voltage at V_{DD} and IRQ	$V_{DD\,min}$	V_{SS} − 0.3 V
Max. voltage at remaining pins	V_{max}	V_{DD} + 0.3 V
Min. voltage at any signal pins	V_{min}	V_{SS} − 0.3 V
Maximum storage temperature	T_{STOmax}	+150°C
Minimum storage temperature	T_{STOmin}	−65°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	+2.0	+5.0	+5.5	V
Crystal Characteristics					
Frequency[1]	f		32.768		kHz
Load capacitance	C_L	8	10	13	pF
Series resistance	R_S		20	50	kΩ
Trimmer capacitance	C_T	5	15	40	pF

[1] Parallel resonant crystal

Table 2

Electrical Characteristics

V_{DD} = 5.0 V, V_{SS} = 0 V, and T_A = 0°C to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Total static supply	I_{SS}	[1]		12	20	µA
Standby current	I_{SS}	V_{DD} = 3 V[1]		5	8	µA
Inputs and Outputs						
Input logic low	V_{IL}		0.0		0.8	V
Input logic high	V_{IH}		2.4		5.0	V
Pullup on $\overline{OE}$ and $\overline{SYNC}$ pins	I_L	V_{IL} = 0.8 V	30			µA
Output logic low on I/O pins	V_{OL}	I_{OL} = 3.2 mA			0.4	V
Output logic high on I/O pins	V_{OH}	I_{OH} = 2 mA	2.4			V
Input leakage	I_{IN}	$0.0 < V_{IN} < 5.0$			1	µA
Oscillator						
Starting voltage	V_{STA}	C_T = 18pF	1.8			V
Input capacitance on XI	C_{IN}			3.7		pF
Output capacitance on XO	C_{OUT}			25		pF
Start-up time	T_{STA}	C_T = 18pF		0.6	5	s
Frequency stability	$\triangle f/f$	$2.0 \leq V_{DD} \leq 5.0$ V, C_T = 5 pF		5	10	ppm/V

[1] All outputs open, TE at V_{SS}, all other inputs at V_{DD}.

Table 3

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, and T_A = 0°C to +70°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Chip select duration	t_{CS}		280			ns
RAM access time[1]	t_{ACC}			150	270	ns
Time between two transfers	t_W		1000			ns
Data valid to Hi-impedance[2]	t_{DF}			180	300	ns
Write data settle time[3]	t_{DW}		200			ns
Data hold time[4]	t_{DH}		10			ns

Table 4

[1] t_{ACC} starts from $\overline{OE}$ or $\overline{CS}$, whichever activates last.
[2] t_{DF} starts from $\overline{OE}$ or $\overline{CS}$, whichever deactivates first.
[3] t_{DW} ends at R/$\overline{W}$ or $\overline{CS}$, whichever deactivates first.
[4] t_{DH} starts from R/$\overline{W}$ or $\overline{CS}$, whichever deactivates first.

4

Timing Waveforms

Read Timing for Both Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola (Advanced R/$\overline{W}$ with $\overline{OE}$ Tied to $\overline{CS}$)

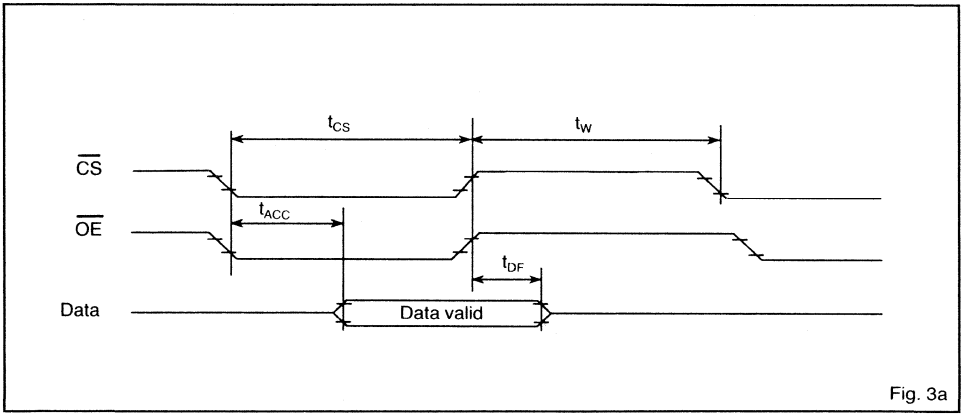


Fig. 3a

Write Timing for Both Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola (Advanced R/$\overline{W}$ with $\overline{OE}$ Tied to $\overline{CS}$)

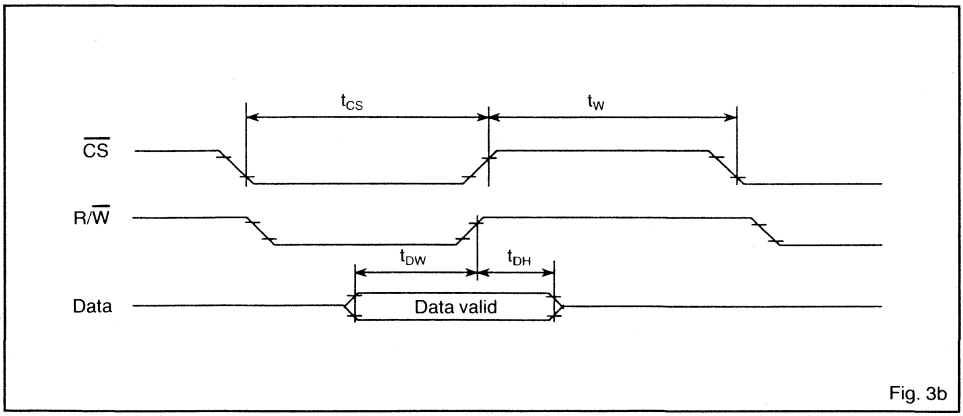


Fig. 3b

Block Diagram

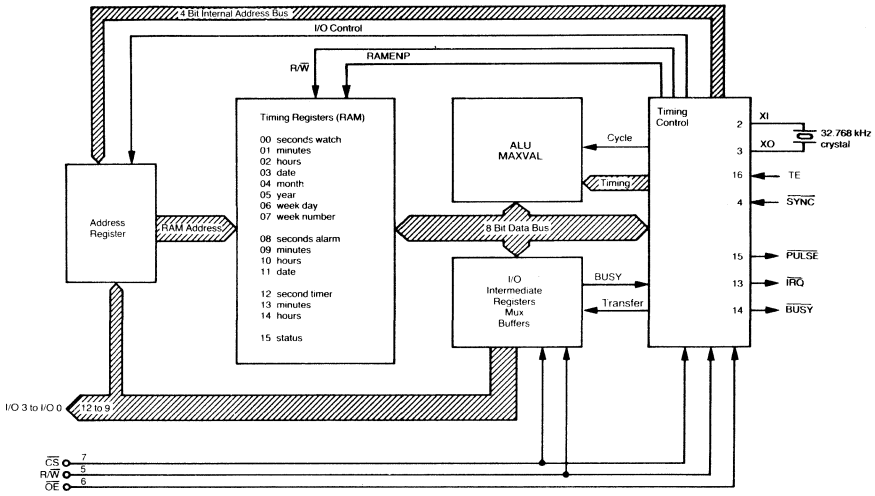


Fig. 4

Pin Description

Pin	Name	Function
1	V_{DD}	Positive supply terminal
2	XI	32.768 kHz quartz input
3	XO	32.768 kHz quartz output
4	$\overline{SYNC}$	Time synchronization input (internal pullup)
5	R/$\overline{W}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola), see Fig. 10
6	$\overline{OE}$	$\overline{RD}$ (Intel), see Fig. 10 (internal pullup)
7	$\overline{CS}$	Chip select input
8	V_{SS}	Ground terminal
9	I/O 0	Data bus input/output lines / Address bus input lines
10	I/O 1	
11	I/O 2	
12	I/O 3	
13	$\overline{IRQ}$	Interrupt request output (open drain with internal pullup)
14	$\overline{BUSY}$	Internal update cycle status output
15	$\overline{PULSE}$	Programmable timing pulse output
16	TE	Transfer enable input

Table 5

Functional Description

Power Supply and Data Retention

The M 3003 can be powered with a supply voltage between 2.0 and 5.5 V, and backed up with a battery or supercap (2.0 to 5.0 V), as indicated in Fig. 10. To ensure correct operation and data retention during power-down an active low power fail signal must be connected to the TE pin. Because of the low power consumption of the device, lithium cells or standard rechargeable cells give many years of effective life. When the transfer enable input TE goes to a low state, all inputs are disable, and the I/O lines and the outputs $\overline{BUSY}$ and $\overline{PULSE}$ are set to a high impedance state. The open-drain output $\overline{IRQ}$ will still go to GND if an internal alarm interrupt condition occurs. Thus it is possible to use the M 3003 in a "sleep and awake" condition to switch on the power system. Care should be taken that no parasitic current flows due to improper states of interfacing signal lines.

RAM

The 16 x 8 RAM is used to store all clock, alarm, timer and status data. The allocation of RAM addresses is shown in Table 6. All time data are stored in Binary Coded Decimal (BCD) format. The transfer of this data between the internal 8-bit bus and the I/O lines is performed by the bidirectional I/O buffer (see Block Diagram Fig. 4). If the alarm and timer functions are not needed, then the RAM section from these functions, addresses 8 to E hex, may be used as non-volatile system storage by software.

It should be noted however that, if the unused function is inadvertently activated by altering the status word, the stored data may be modified.

I/O Address Locations

Address Hex	Address Dec	Data	Group	Max. Value	Operations
0	0	Seconds	Watch	59	Time data
1	1	Minutes		59	incremented
2	2	Hours		23	under control of
3	3	Date		28, 29, 30, 31	status bit 0
4	4	Month		12	
5	5	Year		99	
6	6	Week day		07	
7	7	Week no.		53	
8	8	Seconds	Alarm	59	Alarm data,
9	9	Minutes		59	providing an $\overline{IRQ}$
A	10	Hours		23	under control of
B	11	Date		28, 29, 30, 31	status bit 1
C	12	Seconds	Timer	59	Timer data
D	13	Minutes		59	incremented
E	14	Hours		23	under control of status bit 4
F	15	Status	Status		Control

Table 6

Status and Control

The function of the individual bits of the status word are shown in Table 7. The status word, address F hex, controls the timekeeping functions performed in the ALU section of the M 3003 (see Block Diagram Fig. 4). The status word must be written on recovery from a total power loss, $V_{DD} < 2.0$ V.

Status Word

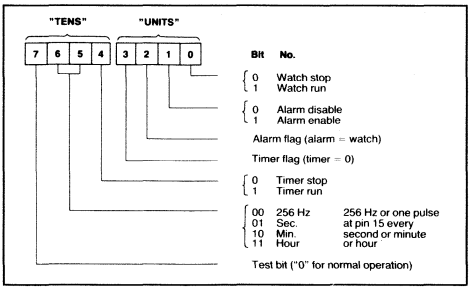


Table 7

RAM Access

The interface between the M 3003 and the host microprocessor consists of four bidirectional multiplexed data/address lines (I/O lines), three control lines ($\overline{CS}$, $\overline{OE}$, R/$\overline{W}$), and an interrupt request line ($\overline{IRQ}$). Three steps are required to access a RAM address. The first access transfers the 4-bit address of the data location, the second reads or writes data bits 7 to 4 (tens) to or from the address written in step one, and the third reads or writes data bits 3 to 0 (units). Fig. 5 shows the 3 step access sequence.

3 Step Access Sequence

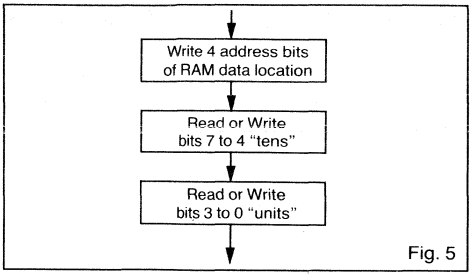


Fig. 5

An internal multiplexer defines the 3 step access sequence position. A 3 step access sequence is began by writing the RAM 4-bit address and then the M 3003 treats the next two accesses as the 4-bit data transfers, tens first, units second. A read access, while the multiplexer is expecting an address write, will not begin a 3 step access sequence.

The multiplexer can be initialized (expecting an address write) by two read accesses. Read accesses will complete a 3 step access sequence, but will not begin one. The multiplexer must be initialized by software on every power up of the system including power up of the M 3003 from a power loss ($V_{DD} < 2.0$ V) condition.

RAM Access and Internal Update Cycles

Every second an internal update occurs and lasts between 0.73 ms and 6 ms. During this update cycle, the multiplexer is initialized, the $\overline{BUSY}$ output is active, and a read will give F hex on the I/O pins. The RAM is allocated to the ALU (see Block Diagram Fig. 4). If an external data transfer is in progress (see RAM Access section), the internal update cycle is delayed for a maximum of one second. After a delay of one second the external data transfer will be aborted and the RAM assigned to the internal update cycle. With the multiplexer in its initial state, reading the M 3003 will give 0 hex if an internal update cycle is not in progress and F hex if in progress. Thus prior to beginning a 3 step access sequence, software must read the I/O pins to determine if the RAM is available. Additionally the $\overline{BUSY}$ pin goes active while an internal update cycle is in progress. To prevent an update during a sequence of transfers, for example hours, minutes and seconds, there must be less than 2 ms between each transfer (i.e. 3 step access sequence). If software continuously polls the M 3003 to seek an event or refresh a display then the delay between two poll sequences (e.g. read hours, minutes, seconds) should be greater than 6 ms to allow an update cycle to occur.

RAM Access and Interrupts

Any false or aborted access will make the M 3003 jump incorrectly to the next step in the 3 step access sequence. Access to the M 3003 is not re-entrant and so

the software routine accessing the M 3003 must complete the 3 step access sequence before another software routine can access the device. Interrupt software routines must not access the M 3003 unless it can be guaranteed that the M 3003 is not in a 3 step access sequence. Additionally interrupt software routines must not delay the 3 step access sequence in the background routine longer than one second or an internal update cycle will occur within the M 3003. It is recommended that all software routines reading or writing to the M 3003 call one of the software routine structures, shown in Fig. 6, for each device access.

M 3003 Software Access Routines

```
M 3003 __ WRITE:
    Disable maskable interrupts
        Wait for Bus = 0 hex
        Write address to M 3003
        Write data bits 7 to 4 to M 3003
        Write data bits 3 to 0 to M 3003
    Enable maskable interrupts

M 3003 __ READ:
    Disable maskable interrupts
        Wait for Bus = 0 hex
        Write address to M 3003
        Read data bits 7 to 4 from M 3003
        Read data bits 3 to 0 from M 3003
    Enable maskable interrupts
```

Fig. 6

Non maskable interrupt routines must not access the M 3003 as it cannot be guaranteed that the M 3003 is not in the middle of a 3 step access sequence. In a multitasking software environment the task accessing the M 3003 must not be interrupted during a 3 step access sequence.

Alarm and $\overline{IRQ}$

An alarm date and time may be preset in RAM addresses 8 to B hex. During every update cycle, the ALU (see Block Diagram Fig. 4) compares the contents of the watch addresses, 0 to 3 hex, with the preset alarm time data, and the alarm is enabled (status word bit 1), the $\overline{IRQ}$ pin goes active and the alarm flag (status word bit 2) is set to indicate to the software the source of the interrupt. $\overline{IRQ}$ will remain active until the software acknowledges the interrupt by clearing the alarm flag (status word bit 2). If the alarm is enabled (status word bit 1), and an alarm RAM location set to FF hex, this location is not compared with the associated watch location. Thus it is possible to achieve a repeat feature where an alarm occurs every programmed number of, seconds or seconds and minutes or seconds, minutes and hours. The M 3003 does not generate interrupts until the 3 step access sequence is complete. The M 3003 will pull the $\overline{IRQ}$ pin active low, while TE is also active low, if an alarm interrupt occurs. This feature can be used to switch on the microprocessor power.

Timer and $\overline{IRQ}$

By setting the status word bit 4 (timer enable bit), the preset time data in RAM addresses C hex to E hex, increments every second with the update cycle. When passing from 23:59:59 to 00:00:00, the timer flag (status word bit 3) is set and the $\overline{IRQ}$ output goes active. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the timer flag (status word bit 3). The M 3003 does not generate interrupts until the 3 step access sequence is complete. The timer is incremented while TE is active low, however it will not cause $\overline{IRQ}$ to become active until TE goes inactive high.

$\overline{PULSE}$ Output

The $\overline{PULSE}$ output can be programmed with bits 5 and 6 of the status word, as shown in Table 7, to produce a negative pulse of 64 μs duration, every second, minute, or hour, while the watch is running. Clearing bits 5 and 6 of the status word will produce a 256 Hz square wave on the $\overline{PULSE}$ pin. The latter feature is intended for frequency tuning, see section Frequency Tuning.

$\overline{SYNC}$ Input

If the $\overline{SYNC}$ input is set high for longer than 200 μs, the watch will synchronize to the falling edge of this $\overline{SYNC}$ signal with a precision of $\pm$ 2 ms. The seconds RAM location (address 0 hex) will be cleared and if the contents were $\geq$ 30, the minutes location (address 1 hex) will be incremented.

Frequency Tuning

The $\overline{PULSE}$ pin will output a 256 Hz square wave signal if the bits 5 and 6 of the status word are cleared. The period of the signal on the $\overline{PULSE}$ pin can be adjusted by the crystal trimmer. The nominal period for 256 Hz is 3.90625 ms (see Fig. 7)

Calibration Circuit

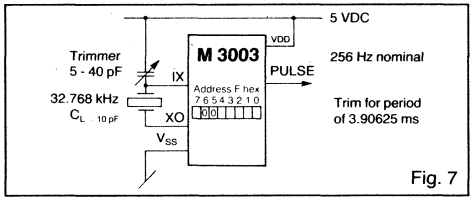


Fig. 7

Crystal Layout

In order to ensure proper oscillator operation we recommend the following standard practices.

- Keep traces as short as possible
- Use a guard ring around the crystal and capacitor or trimmer.

Fig. 8 shows the recommended layout.

P.C.B. Layout

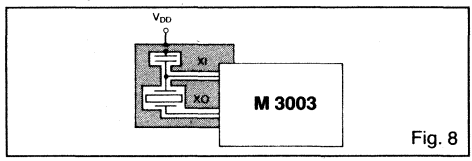


Fig. 8

Test

Some of the various test features added to the M 3003, can be activated by software. Table 8 shows the available test modes and how they may be activated.

Test Modes

Status bit 7	Status bit 5	$\overline{SYNC}$ input	Function
0	0	V_{SS}	Normal operation
1	0	V_{DD}	First 5 stages of divider chain bypassed: acceleration by a factor of 32
1	1	V_{SS}	Parallel increment of all time and timer data at 1Hz depending on the status of bit 0 and bit 4.
1	1	V_{DD}	Parallel increment of all time and timer data at 32Hz depending on the status of bit 0 and bit 4. First 5 stages of divider chain bypassed: thus acceleration by a factor of 32

Table 8

An external signal generator can be used to drive the M 3003. Fig. 9 shows how to connect the signal generator. The speed can be increased by increasing the signal generator frequency to a maximum of 128 kHz. Test modes can be activated while using an external signal generator if required. To leave test, the test bit (status word bit 7) must be cleared by software. Test corrupts the watch and timer data and so all parameters should be reloaded after a test session.

Signal Generator Connection

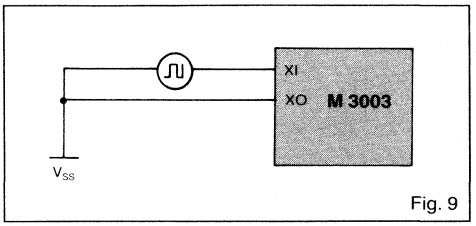


Fig. 9

4

Typical Application

Intel Microprocessor Interfaced with the M 3003

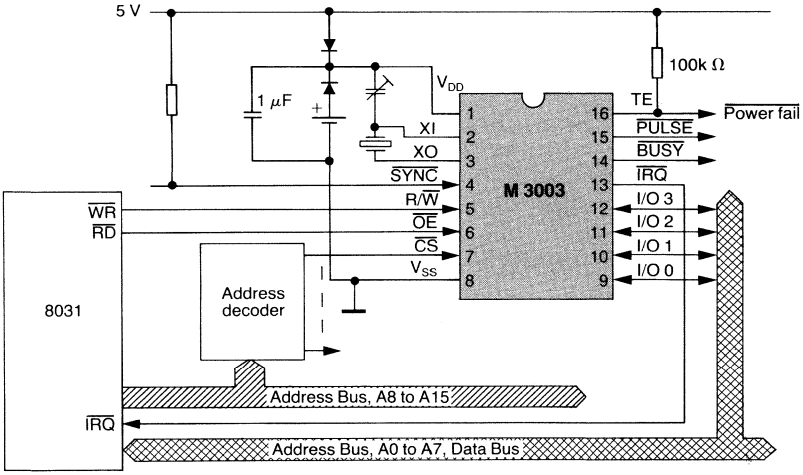
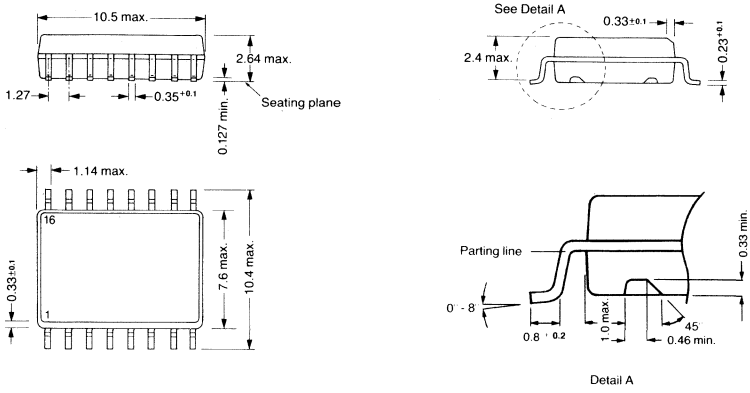


Fig. 10

Package and Ordering Information

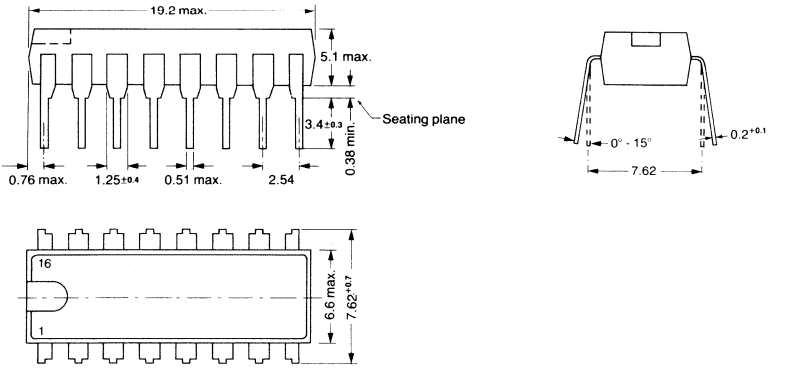
Dimensions of SO Package



Dimensions in mm

Fig. 11

Dimensions of DIP Package



Dimensions in mm

Fig. 12

Ordering Information

The M 3002 is available in the following packages:

DIP 16-pin plastic package	M 3003 16 P
SO 16-pin wide plastic package	M 3003 16 S

Chip form on request.

When ordering, please specify the complete part number and package.

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1 Bit Real Time Clock

Features

- Supply current typically 800 nA at 3 V
- 60 ns access time
- Fully operational from 2.0 V to 5.5 V
- No busy states or danger of a clock update while accessing
- Serial communication on one line of a standard parallel data bus or over a conventional 3 wire serial interface
- Interface compatible with both Intel and Motorola
- Seconds, minutes, hours, day of month, month, year, week day and week number in BCD format
- Leap year and week number correction
- Time set lock mode to prevent unauthorized setting of the current time or date
- Oscillator stability 0.3 ppm / volt
- No external capacitor needed
- Frequency measurement and test modes
- Packages DIP8 and SO8

Description

The V 3021 is a low power CMOS real time clock. Data is transmitted serially as 4 address bits and 8 data bits, over one line of a standard parallel data bus. The device is accessed by chip select ($\overline{CS}$) with read and write control timing provided by either $\overline{RD}$ and $\overline{WR}$ pulse (Intel CPU) or $\overline{DS}$ with advanced R/$\overline{W}$ (Motorola CPU). Data can also be transmitted over a conventional 3 wire serial interface having CLK, data I/O and strobe. The V 3021 has no busy states and there is no danger of a clock update while accessing. Supply current is typically 800 nA at V_{DD} = 3.0 V. Battery operation is supported by complete functionality down to 2.0 V. The oscillator stability is typically 0.3 ppm/V. If the V 3021 is used with a ± 10 ppm crystal having a load capacitance of 8.2 pF, then the accuracy will be typically 1 s/day at 25°C.

Applications

- Utility meters
- Battery operated and portable equipment
- Consumer electronics
- White/brown goods
- Pay phones
- Cash registers
- Personal computers
- Programmable controller systems
- Data loggers

Typical Operating Configuration

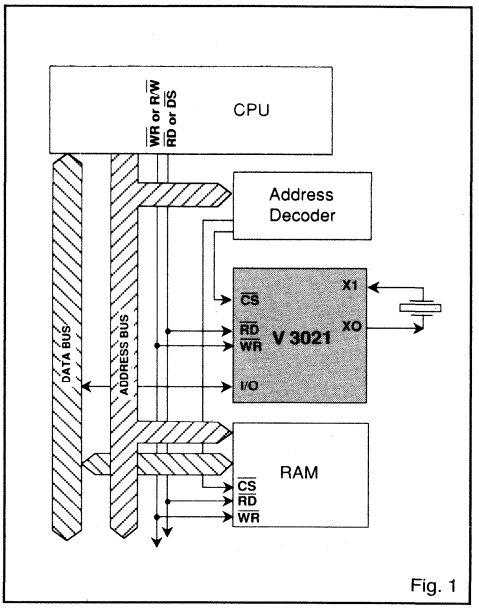


Fig. 1

Pin Assignment

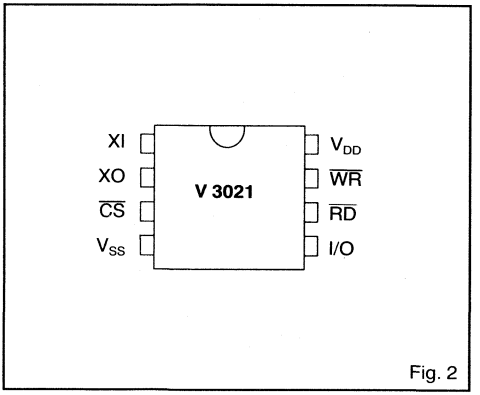


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS} + 7.0V
Minimum voltage at V_{DD}	V_{DDmin}	V_{SS} − 0.3V
Maximum voltage at any signal pin	V_{max}	V_{DD} + 0.3V
Minimum voltage at any signal pin	V_{min}	V_{SS} − 0.3V
Maximum storage temperature	T_{STOmax}	+150°C
Minimum storage temperature	T_{STOmin}	−65°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{Smax}	1000V
Maximum soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, it is advised that normal precautions be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	+2.0	+5.0	+5.5	V
Supply voltage dv/dt (power-up & power-down)				6	V/µs
Decoupling capacitor			100		nF
Crystal Characteristics					
Frequency[1]	f		32.768		kHz
Load capacitance	C_L	7	8.2	30	pF
Series resistance	R_S		35	50	kΩ

[1] Parallel resonant crystal, use a ±10ppm crystal with a load capacitance of 8.2pF to achieve an accuracy of typically ± 1s/day at 25°C. ±11.57ppm = ±1s/day.

Table 2

Electrical Characteristics

V_{DD} = 5.0V ± 10%, V_{SS} = 0V and T_A = −40°C to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Total static supply	I_{SS}	all outputs open, all inputs at V_{DD} V_{DD} = 3.0V, address 0 = 0		0.8	1.8	µA
Total static supply	I_{SS}	all outputs open, all inputs at V_{DD} address 0 = 0		1.3	10	µA
		T_A = 25°C			3	µA
Dynamic current	I_{SS}	I/O to V_{SS} through 1MΩ $\overline{RD}$ = V_{SS}, $\overline{WR}$ = V_{DD}, $\overline{CS}$ = 4MHz address 0 = 0, read all 0			300	µA
Input / Output						
Input logic low	V_{IL}				1.0	V
Input logic high	V_{IH}		3.5			V
Output logic low	V_{OL}	I_{OL} = 4mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 4mA	2.4			V
Input leakage	I_{IN}	0.0 < V_{IN} < 5.0 V		0.1	1	µA
Output tri-state leakage on I/O pin	I_{TS}	$\overline{CS}$ high, and address 0, bit 0, low		0.1	1	µA
Oscillator						
Starting voltage	V_{STA}		1.8			V
Input capacitance on XI	C_{IN}	T_A = 25°C		13		pF
Output capacitance on XO	C_{OUT}	T_A = 25°C		9		pF
Start-up time	T_{STA}			1		s
Frequency stability	△f/f	2.0 ≤ V_{DD} ≤ 5.5V, T_A = 25°C		0.3	0.5	ppm/V
Frequency Measurement Mode						
Current source on I/O pin pulsed on/off @ 256Hz	I_{ONF}	$\overline{CS}$ high, addr. 0, bit 0, high $V_{I/O}$ = 1 V	10	25	60	µA

Table 3

Timing Characteristics

V_{SS} = 0V, and T_A = −40°C to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Max.	Min.	Typ.	Max.	Units
			$V_{DD} \geq 2V$		$V_{DD} = 5.0V \pm 10\%$			
Chip select duration	t_{CS}	Write cycle	500		50			ns
RAM access time[1]	t_{ACC}	C_{LOAD} = 50pF		300		50	60	ns
Time between two transfers	t_W		500		100			ns
Rise time[2]	t_R		10	200	10		200	ns
Fall time[2]	t_F		10	200	10		200	ns
Data valid to Hi-impedance[3]	t_{DF}		15	200	15	30	40	ns
Write data settle time[4]	t_{DW}		80		50			ns
Data hold time[5]	t_{DH}		120		25			ns
Advance write time	t_{ADW}		20		10			ns
Write pulse time[6]	t_{WC}		500		50			ns

Table 4

[1] t_{ACC} starts from $\overline{RD}$ or $\overline{CS}$, whichever activates last
[2] $\overline{CS}$, $\overline{RD}$, $\overline{DS}$, $\overline{WR}$ and R/$\overline{W}$ rise and fall times are specified by t_R and t_F
[3] t_{DF} starts from $\overline{RD}$ or $\overline{CS}$, whichever deactivates first
[4] t_{DW} ends at $\overline{WR}$ or $\overline{CS}$, whichever deactivates first
[5] t_{DH} starts from $\overline{WR}$ or $\overline{CS}$, whichever deactivates first
[6] t_{WC} starts from $\overline{WR}$ or $\overline{CS}$, whichever activates last and ends at $\overline{WR}$ or $\overline{CS}$, whichever deactivates first

Timing Waveforms

Read Timing for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola ($\overline{DS}$ (or $\overline{RD}$ pin tied to $\overline{CS}$) and R/$\overline{W}$)

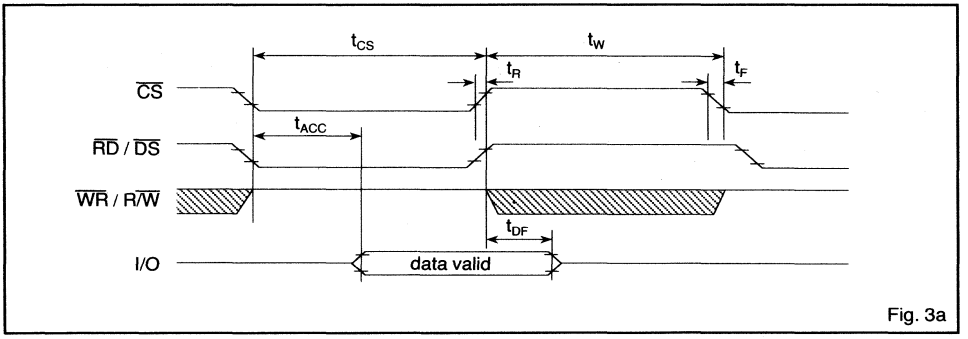


Fig. 3a

Write Timing for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)

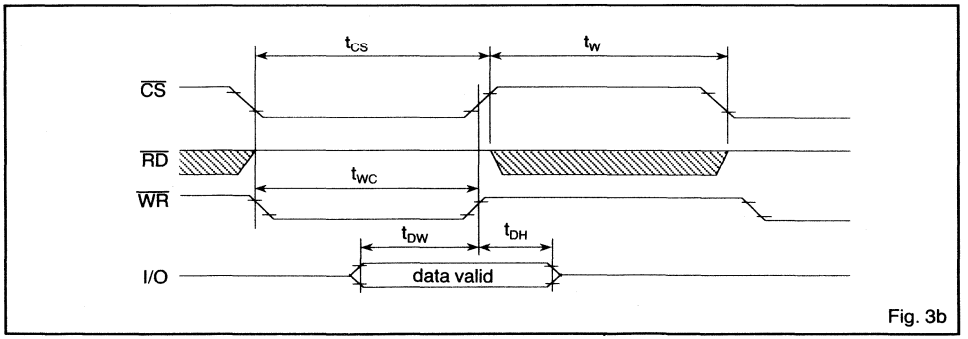


Fig. 3b

Write Timing for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)

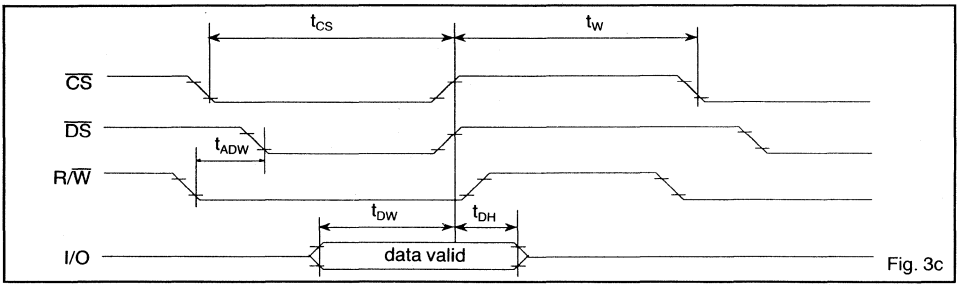


Fig. 3c

Communication Cycles

Read Data Cycle for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)

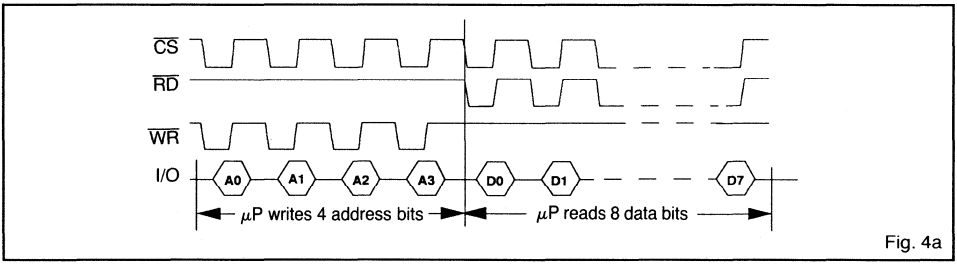


Fig. 4a

Read Data Cycle for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)

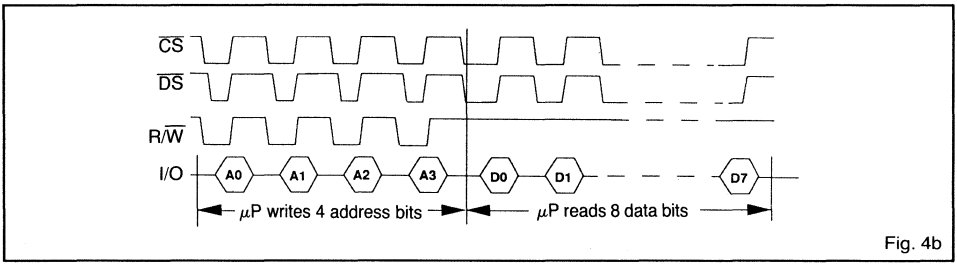


Fig. 4b

Write Data Cycle for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)

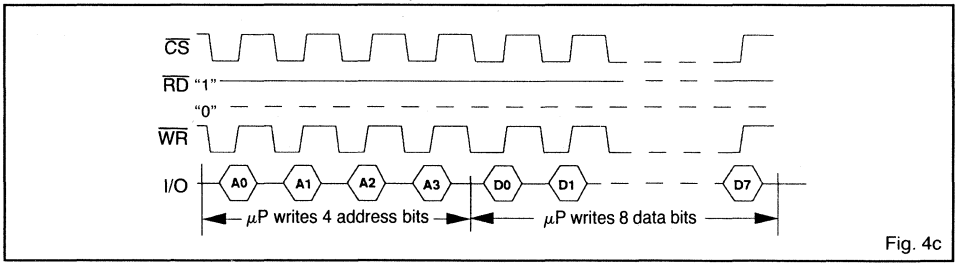


Fig. 4c

Write Data Cycle for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)

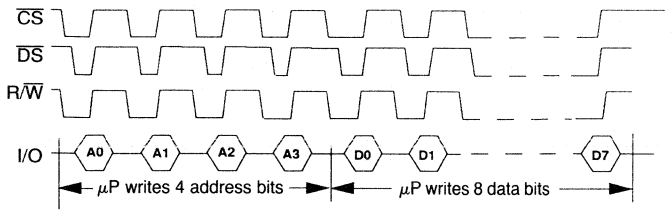


Fig. 4d

Address Command Cycle for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)

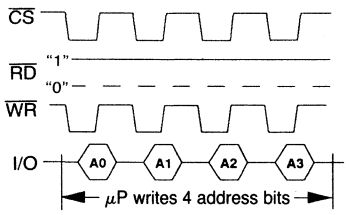


Fig. 4e

Address Command Cycle for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)

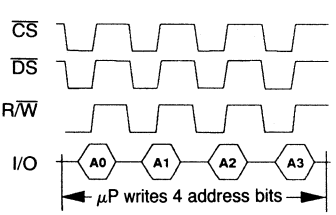


Fig. 4f

Block Diagram

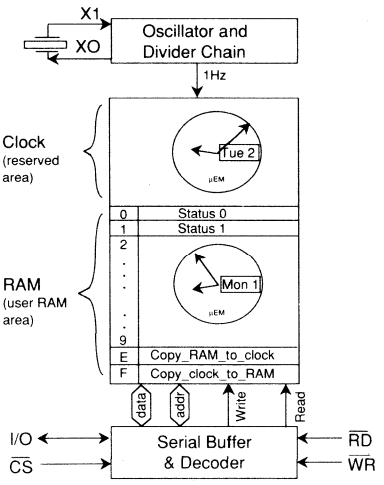


Fig. 5

Pin Description

Pin	Name	Function
1	XI	32 kHz crystal input
2	XO	32 kHz crystal output
3	$\overline{CS}$	Chip select input
4	V_{SS}	Ground supply
5	I/O	Data input and output
6	$\overline{RD}$	Intel $\overline{RD}$ Motorola $\overline{DS}$ (or tie to $\overline{CS}$)
7	$\overline{WR}$	Intel $\overline{WR}$, Motorola R/$\overline{W}$
8	V_{DD}	Positive supply

Table 5

Functional Description

Serial Communication

The V 3021 resides on the parallel data and address buses as a standard peripheral (see Fig. 11 and 12). Address decoding provides an active low chip select ($\overline{CS}$) to the device. For Intel compatible bus timing the control signals $\overline{RD}$ and $\overline{WR}$ pulse and $\overline{CS}$ are used for a single bit read or write (see Fig. 3a and 3b). Two options exist for Motorola compatible bus timing. The first is to use the control signals $\overline{DS}$ with R/$\overline{W}$ and $\overline{CS}$, the second is to tie the $\overline{RD}$ input to CS and use the control signals R/$\overline{W}$ and $\overline{CS}$ (see Fig. 3a and 3c). Data transfer is accomplished through a single input/output line (I/O). Any data bus line can be chosen. A conventional 3 wire serial interface can also be used to communicate with the V 3021 (see Fig. 13).

Communication Cycles

The V 3021 has 3 serial communication cycles. These are:

1) Read data cycle
2) Write data cycle
3) Address command cycle

A communication cycle always begins by writing the 4 address bits, A0 to A3. A microprocessor read from the V 3021 cannot begin a communication cycle. Read and write data cycles are similar and consist of 4 address bits and 8 data bits. The 4 address bits, A0 to A3, define the RAM location and the 8 data bits, D0 to D7, provide the relevant information. An address command cycle consists of only 4 address bits.

Read Data Cycle

A read data cycle commences by writing the 4 RAM address bits (A3, A2, A1 and A0) to the V 3021. The LSB, A0, is transmitted first (see Fig. 4a and 4b). Eight microprocessor reads from the V 3021 will read the RAM data at this address, beginning with the LSB, D0. The read data cycle finishes on reading the 8th data bit, D7.

Write Data Cycle

A write data cycle commences by writing the 4 RAM address bits (A3, A2, A1 and A0) to the V 3021. The LSB, A0, is transmitted first (see Fig. 4c and 4d). Eight microprocessor writes to the V 3021 will write the new RAM data. The LSB, D0, is loaded first. The write data cycle finishes on writing the 8th data bit, D7.

Address Command Cycle

An address command cycle consists of just 4 address bits. The LSB, A0, is transmitted first (see Fig. 4e and 4f). On writing the fourth address bit, A3, the address will be decoded. If the address bits are recognized as one of the command codes E hex, or F hex (see Table 6), then the communication cycle is terminated and the corresponding command is executed. Subsequent microprocessor writes to the V 3021 begin another communication cycle with the first bit being interpreted as the address LSB, A0.

Clock Configuration

The V 3021 has a reserved clock area and a user RAM area (see Fig. 5). The clock is not directly accessible, it is used for internal time keeping and contains the current time and date. The contents of the RAM is shown in Table 6, it contains a data space and an address command space. The data space is directly accessible. Addresses 0 and 1 contain status informaton (see Tables 7a and 7b), addresses 2 to 5, time data, and addresses 6 to 9, date data. The address command space is used to issue commands to the V 3021.

RAM Map

Address Dec	Address Hex	Parameter	BCD range
Data Space			
0	0	Status 0	
1	1	Status 1	
2	2	Seconds	00 - 59
3	3	Minutes	00 - 59
4	4	Hours	00 - 23
5	5	Day of month	01 - 31
6	6	Month	01 - 12
7	7	Year	00 - 99
8	8	Week day	01 - 07
9	9	Week number	00 - 52
Address Command Space			
14	E	Copy_RAM_to_clock	
15	F	Copy_clock_to_ RAM	

Table 6

Commands

Two commands are available (see Table 6). The Copy_RAM_to_clock command is used to set the current time and date in the clock and the Copy_clock_ to_RAM command to copy the current time and date from the clock to the RAM. The Copy_RAM_to_clock command, address data E hex, causes the clock time and date to be overwritten by the time and date stored in the RAM at addresses 2 to 9. Address 1 is also cleared (see section "Time and Date Status Bits"). Prior to using this command, the desired time and date must be loaded into the RAM using write data cycles and the time set lock bit, address 0, bit 7, must be clear (see section "Time Set Lock"

Status Information

The RAM addresses 0 and 1 contain status and control data for the V 3021. The function of each bit (0 to 7) within address locations 0 and 1 is shown in Tables 7a and 7b respectively.

Status Word

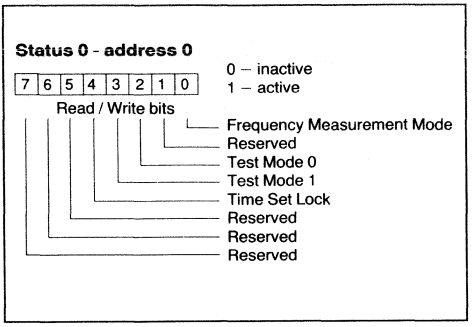


Table 7a

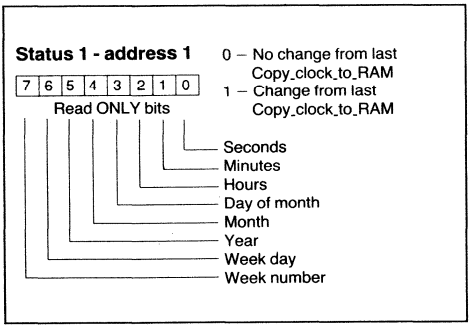


Table 7b

Reset and Initialization

Upon microprocessor recovery from a system reset, the V 3021 must be initialized by software in order to guarantee that it is expecting a communication cycle (i.e. the internal serial buffer is waiting for the address bit A0). Software can initialize the V 3021 to expect a communication cycle by executing 8 microprocessor reads (see Fig. 6).

Initializing Access to the V 3021

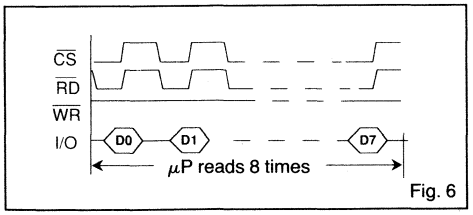


Fig. 6

On first startup or whenever power has failed ($V_{DD} < 2.0$ V) the status register 0 and the clock must be initialized by software. Having initialized the interface to expect the address bit A0, write 0 to status register 0, then set the clock (see section "Clock and Calendar").

Time and Date Status Bits

There are time and date status bits at address 1 in the RAM. Upon executing a Copy_clock_to_RAM command, the time and date status bits in the RAM show which time and date parameters changed since the last time this command was used. A logic 1 in the seconds status bit (address 1, bit 0) in the RAM indicates that the seconds location in the RAM (address 2) changed since the last Copy_clock_to_RAM command and thus needs to be read. The seconds location must change before any other time or date location can change. If the seconds status bit is clear, then no time or date location changed since the last Copy_clock_to_RAM command and so the RAM need not be read by software.

Table 7b shows the seconds, minutes, hours, day of month, month, year, week day, and week number status bit locations. They are set or cleared similar to the seconds location. It should be noted that if the minutes status bit is clear, then the seconds bit may be set, but all other status bits are clear. Similarly with hours, the bits representing the units less than hours may have been set, but the bits for the higher units will be clear. This rule holds true for the week day or day of month locations also.

The time and date status bits can be used to drive software routines which need to be executed every

- second,
- minute,
- hour,
- day of month / week day,
- month,
- year,

or - week.

In this application it is necessary to poll the V 3021 at least once every time interval used as it does not generate an interrupt. Upon executing a Copy_RAM_ to_clock command, the time and date status bits in the RAM are cleared.

Time Set Lock

The time set lock control bit is located at address 0, bit 4 (see Table 7a). When set by software, the bit disables the Copy_RAM_to_clock command (see section "Commands".) A set bit prevents unauthorized overwriting of the current time and date in the clock. Clearing the time set lock bit by software will re-enable the Copy_RAM_to_clock command. On first startup or whenever power has failed ($V_{DD} < 2.0$ V), the time set lock bit must be setup by software.

Reading the Current Time and Date

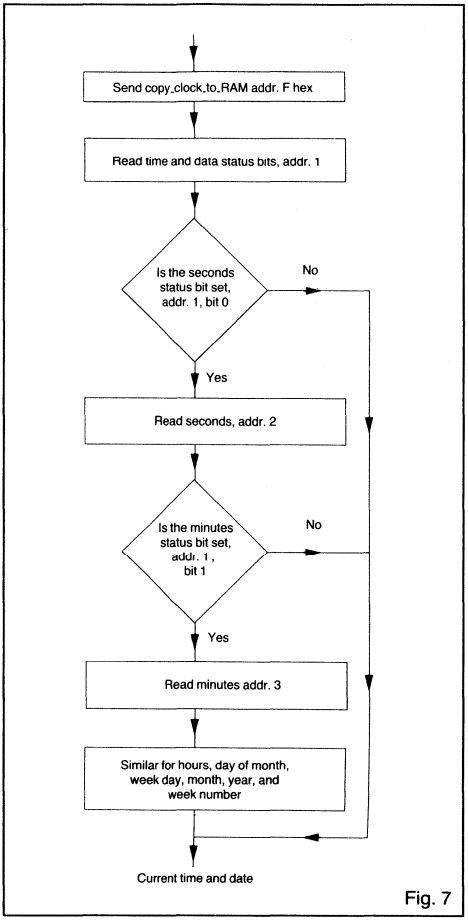


Fig. 7

Clock and Calendar

The time and date addresses in the RAM (see Table 6) provide access to the seconds, minutes, hours, day of month, month, year, week day, and week number. These parameters have the ranges indicated on Table 6 and are in BCD format. If a parameter is found to be out of range, it will be cleared on its being next incremented. The V 3021 incorporates leap year correction and week number calculation. The week number changes only at the incrementation of the day number from 7 to 1. If week 52 day 7 falls on the 25th, 26th or 27th of December, then the week number will change to 0 otherwise it will be week 1. Week days are numbered from 1 to 7 with Monday as 1.

Reading of the current time and date must be preceded by a Copy_clock_to_RAM command. The time and date status bits will indicate which time and date addresses changed since the last time the command was used (see Fig. 7). The time and date from the last Copy_clock_to_RAM command is held unchanged in the RAM, except when power (V_{DD}) has failed totally. To change the current time and date in the clock, the desired time and date must first be written to the RAM, the time set lock bit cleared, and then a Copy_RAM_to_clock command sent (see Fig. 8). The time set lock bit can be used to prevent unauthorized setting of the clock.

Setting the Current Time and Date

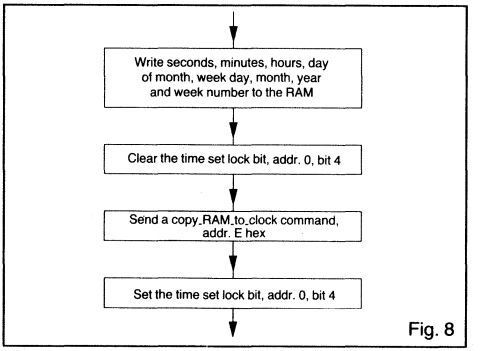


Fig. 8

Frequency Measurement

Setting bit 0 at address 0 will put a pulsed current source (25 μA) onto the I/O pin, when the device is not chip selected (i.e. CS input high). The current source will be pulsed on/off at 256 Hz. The period for $\pm$ 0 ppm time keeping is 3.90625 ms. To measure the frequency signal on pin I/O, the data bus must be high impedance. The best way to ensure this is to hold the microprocessor and peripherals in reset mode while measuring the frequency. The clarity of the signal measured at pin I/O will depend on both the probe input impedance (typically 1 MΩ) and the magnitude of the leakage current from other devices driving the line connected to pin I/O. If the signal measured is unclear, put a 200 kΩ resistor from pin I/O to V_{SS}. It should be noted that the magnitude of the current source (25 μA) is not sufficient to drive the data bus line in case of any other device driving the line, but it is sufficient to take the line to a high logic level when the data bus is in high impedance.

Use a crystal of nominal C_L = 8.2 pF as specified in the section "Operating Conditions". The MX series from Microcrystal is recommended. The accuracy of the time keeping is dependent upon the frequency tolerance and the load capacitance of the crystal. 11.57 ppm corresponds to one second a day.

Test

From the various test features added to the V 3021 some may be activated by the user. Table 7a shows the test mode bits. Table 8 shows the 3 available test modes and how they can be activated. Test mode 0 is activated by setting bit 2, address 0, and causes all time keeping to be accelerated by 32. Test mode 1 is activated by setting bit 3, address 0, and causes all the time and date locations, address 2 to address 9, to be incremented in parallel at 1 Hz with no carry over (independent of each other). The third test mode combines the previous two resulting in parallel incrementing at 32 Hz.

Test Modes

Addr. 0 bit 3	Addr. 0 bit 2	Function
0	0	Normal operation
0	1	All time keeping accelerated by 32
1	0	Parallel increment of all time data at 1 Hz with no carry over
1	1	Parallel increment of all time data at 32 Hz with no carry over

Table 8

An external signal generator can be used to drive the divider chain of the V 3021. Fig. 9 shows how to connect the signal generator. The speed can be increased by increasing the signal generator frequency to a maximum of 128 kHz. An external signal generator and test modes can be combined.
To leave test both test bits (address 0, bits 2 and 3) must be cleared by software. Test corrupts the current time and date and so the time and date should be reloaded after a test session.

Signal Generator Connection

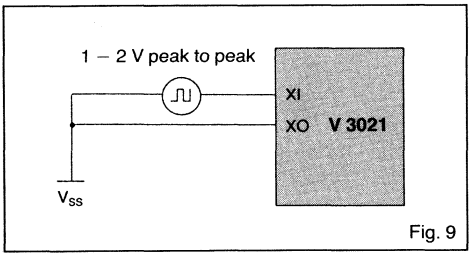


Fig. 9

Note: The peak value of the signal provided by the signal generator should not exceed 2 V.

Crystal Layout

In order to ensure proper oscillator operation we recommend the following standard practices:
– Keep traces as short as possible.
– Use a guard ring around the crystal.
Fig. 10 shows the recommended layout.

Oscillator Layout

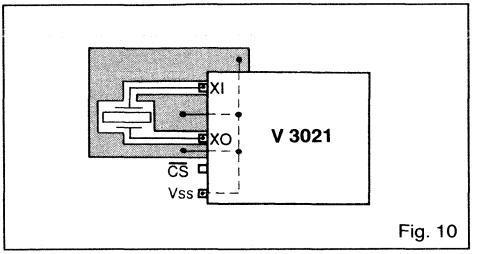


Fig. 10

Access Considerations

The section "Communication Cycles" describes the serial data sequences necessary to complete a communication cycle. In common with all serial peripherals, the serial data sequences are not re-entrant, thus a high priority interrupt, or another software task, should not attempt to access the V 3021 if it is already in the middle of a cycle. A semaphore (software flag) on access would allow the V 3021 to be shared with other software tasks or interrupt routines. There is not time limit on the duration of a communication cycle and thus interrupt routines (which do not use the V 3021) can be fully executed in mid cycle without any consequences for the V 3021.

Typical Applications

V 3021 Interfaced with Intel CPU ($\overline{RD}/\overline{WR}$ Pulse)

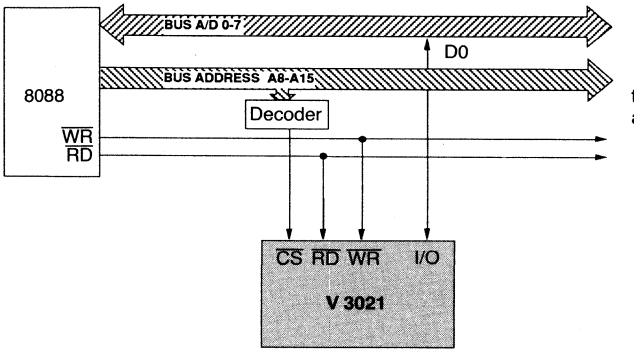


Fig. 11

V 3021 Interfaced with Motorola CPU (Advanced R/$\overline{W}$)

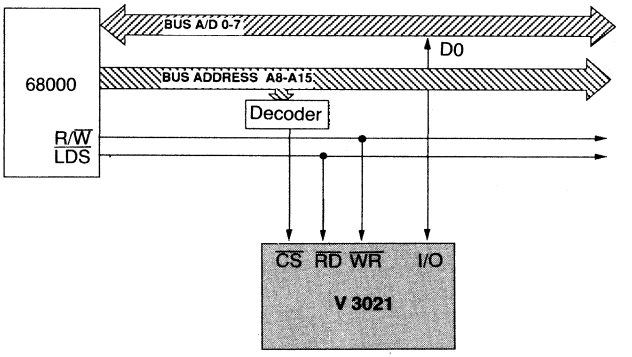
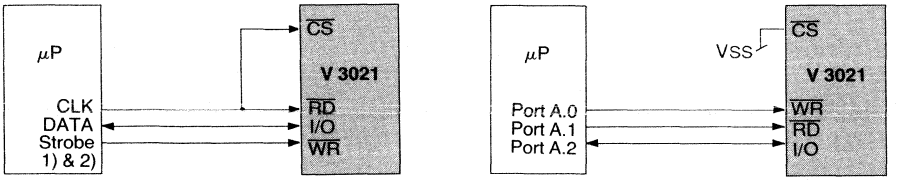


Fig. 12

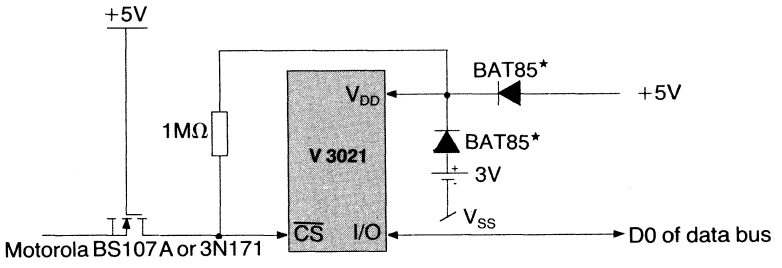
3 Wire Serial Interface



1) With strobe low bits are written to the V 3021, and with strobe high bits are read from the V 3021
2) For serial ports with byte transfer only, an address command cycle should be combined with every data cycle to give 8 address bits and 8 data bits. For example to read the current minutes, write address data F + 3 (1111 + 0011) and then read 8 data bits.

Fig. 13

Battery Switch Over Circuit

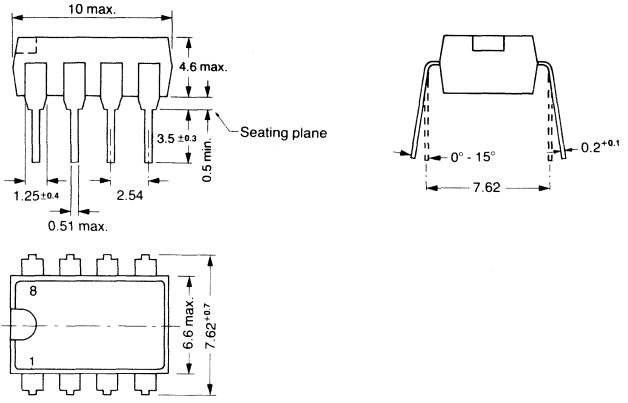


* Use Schottky barrier diodes. The BAT85 has a typical V_F of 250 mV at an I_F of 1 mA. The reverse current is typically 200 nA at a V_R of 5 V. The reverse recovery time is 5 ns. For surface mount applications use the Philips BAT17 in SOT23 or other.

Fig. 14

Package and Ordering Information

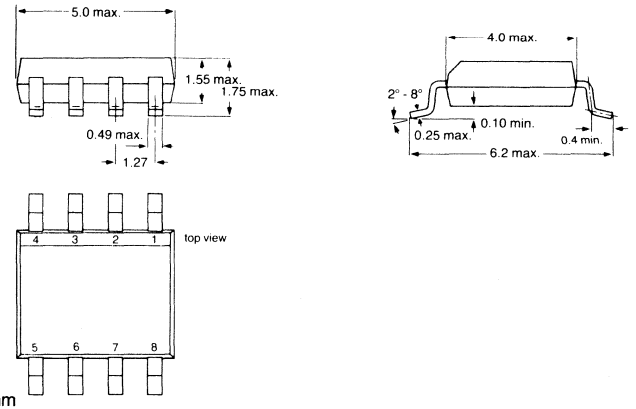
Dimensions of DIP Package



Dimensions in mm

Fig. 15

Dimensions of SO Package



Dimensions in mm

Fig. 16

Ordering Information

The V 3021 is available in the following package:

DIP 8 plastic package	V 3021 8P
SO 8 plastic package	V 3021 8S

When ordering, please specify the complete part number.

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8 Bit Real Time Clock Module

Features

- **Built-in crystal with digital trimming and temperature compensation facilities**
- Standby on power down typically 1.2 μA
- Simple 8 bit interface with no delays or busy flags
- Universal interface compatible with both Intel and Motorola
- 50 ns access time
- Power fail input disables during power up / down or reset
- Bus can be tri-state in power fail mode
- Wide voltage range, 2.0 V to 5.5 V
- 12 or 24 hour data formats
- Time to 1/100 of a second
- Leap year correction and week number calculation
- Alarm and timer interrupts
- Programmable interrupts: 10 ms, 100 ms, s or min
- Sleep mode capability
- Alarm programmable up to one month
- Timer measures elapsed time up to 24 hours
- Packages DIP18 and SO28

Description

The V 3022 is a low power CMOS real time clock with a built-in crystal. Standby current is typically 1.2 μA and the access time is 50 ns. The interface is 8 bits with multiplexed address and data bus. Multiplexing of address and data is handled by the input line $\overline{A}$/D. There are no busy flags in the V 3022, internal time update cycles are invisible to the user's software. Time data can be read from the V 3022 in 12 or 24 hour data formats. An external signal puts the V 3022 in standby mode. Even in standby, the V 3022 pulls the $\overline{IRQ}$ pin active low on an internal alarm interrupt. Calendar functions include leap year correction and week number calculation. Time precision can be achieved by digital trimming.

Applications

- Industrial controllers
- Alarm systems with periodic wake up
- PABX and telephone systems
- Point of sale terminals

Typical Operating Configuration

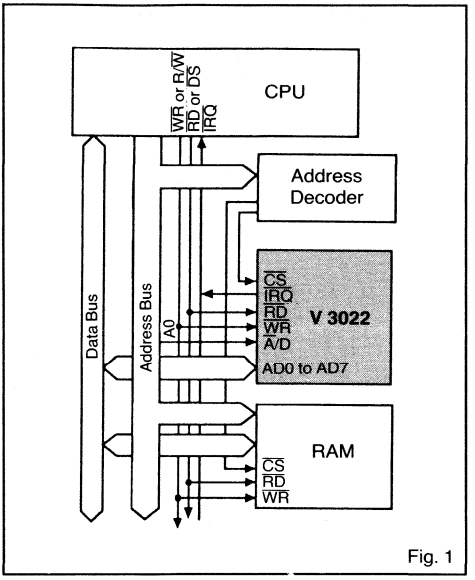


Fig. 1

Pin Assignment

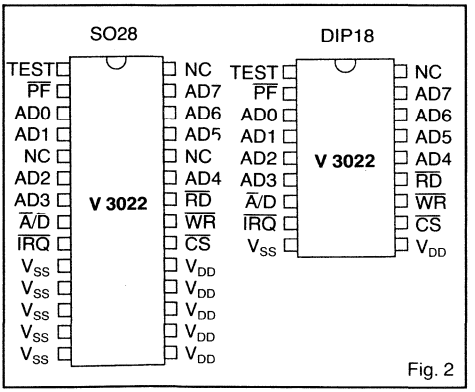


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS} + 7.0V
Max. voltage at remaining pins	V_{max}	V_{DD} + 0.3V
Min. voltage on all pins	V_{min}	V_{SS} − 0.3V
Maximum storage temperature	T_{STOmax}	+125°C
Minimum storage temperature	T_{STOmin}	−55°C
Maximum electrostatic discharge to MIL-STD-883C method 3015	V_{Smax}	1000V
Maximum soldering conditions	T_{Smax}	250°C x 10 s
Shock resistance		5000 g, 0.3 ms, ½ sine

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	+2.0	+5.0	+5.5	V
Supply voltage dv/dt (power-up and down)	dv/dt			6	V/µs
Decoupling capacitor			100		nF

Table 2

Electrical Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = −40°C to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby current	I_{DD}	V_{DD} = 3 V, $T_A \leq 25°C$, $\overline{PF}$ = 0		1.2		µA
		V_{DD} = 3 V, $\overline{PF}$ = 0			15	µA
		$T_A \leq 25°C$, $\overline{PF}$ = 0		2		µA
Dynamic current	I_{DD}	all outputs open, $\overline{CS}$ = 4 MHz $\overline{RD} = V_{SS}$, $\overline{WR} = V_{DD}$ [1]			1.5	mA
$\overline{IRQ}$ (open drain)						
Output low voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Output low voltage	V_{OL}	I_{OL} = 1 mA, V_{DD} = 2 V			0.4	V
Inputs and Outputs						
Input logic low	V_{IL}	T_A = 25°C			0.2 · V_{DD}	V
Input logic high	V_{IH}	T_A = 25°C	0.8 · V_{DD}			V
Output logic low	V_{OL}	I_{OL} = 6mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 6mA	2.4			V
$\overline{PF}$ activation voltage	V_{PFL}			0.5 · V_{DD}		V
$\overline{PF}$ hysteresis	V_H			100		mV
Input leakage	I_{IN}	$V_{SS} < V_{IN} < V_{DD}$		10	1000	nA
Output tri-state leakage	I_{TS}	$\overline{CS}$ = 1		10	1000	nA
Oscillator Characteristics						
Starting voltage	V_{STA}	$T_A \geq 25°C$	2			V
				2.5		V
Start-up time	T_{STA}			1		s
Frequency Characteristics						
Frequency tolerance	△f/f	T_A = 25°C addr. 10 hex = 00hex	150	210[3]	255	ppm
Frequency stability	f_{sta}	2 V ≤ V_{DD} ≤ 5.5 V [2]		1	5	ppm/V
Temperature stability	t_{sta}	addr. 10hex = 00hex		see Fig. 5		ppm
Aging	t_{ag}	T_A = 25°C, first year			± 5	ppm/year

Table 3

[1] Dynamic current is measured with all inputs to V_{DD} and all outputs open.
[2] At a given temperature.
[3] See Fig. 4

Typical Standby Current at $V_{DD} = 5$ V

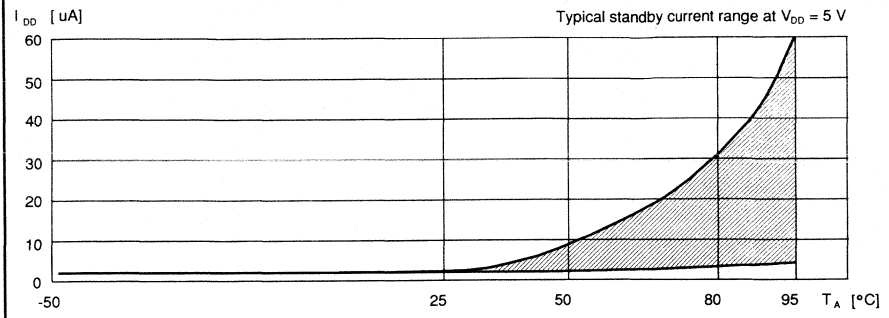


Fig. 3

Typical Frequency on $\overline{IRQ}$

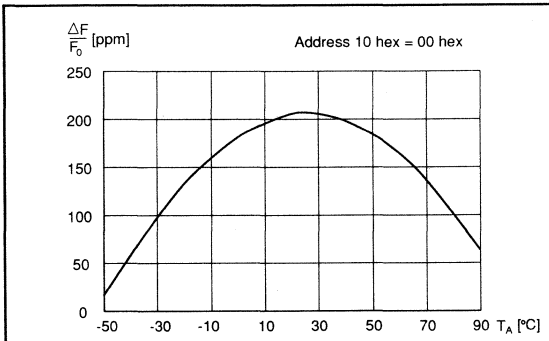
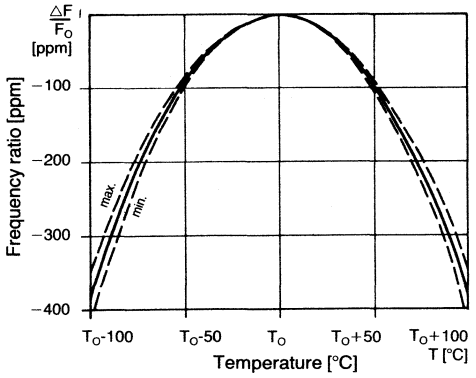


Fig. 4

Module Characteristic



$$\frac{\Delta F}{F_O} = -0.038 \frac{ppm}{°C^2} (T - T_O)^2 \pm 10\%$$

$\Delta F/FO$ = the ratio of the change in frequency to the nominal value expressed in ppm (It can be thought of as the frequency deviation at any temperature.)

T = the temperature of interest in °C

T_O = the turnover temperature (25 ± 5°C)

To determine the clock error (accuracy) at a given temperature, add the frequency tolerance at 25°C to the value obtained from the formula above.

Fig. 5

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, and T_A = −40°C to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Chip select duration, write cycle	t_{CS}		50			ns
Write pulse duration	t_{WR}		50			ns
Time between two transfers	t_W		100			ns
RAM access time[1]	t_{ACC}	C_{LOAD} = 50 pF		50	60	ns
Data valid to Hi-impedance[2]	t_{DF}		10	30	40	ns
Write data settle time[3]	t_{DW}		50			ns
Data hold time[4]	t_{DH}		10			ns
Advance write time	t_{ADW}		10			ns
$\overline{PF}$ response delay	t_{PF}				100	ns
Rise time (all timing waveform signals)	t_R				200	ns
Fall time (all timing waveform signals)	t_F				200	ns
$\overline{CS}$ delay after $\overline{A}$/D[5]	$t_{\overline{A}/Ds}$		5			ns
$\overline{CS}$ delay to $\overline{A}$/D	$t_{\overline{A}/Dt}$		10			ns

Table 4

[1] t_{ACC} starts from $\overline{RD}$ ($\overline{DS}$) or $\overline{CS}$, whichever activates last
[2] t_{DF} starts from $\overline{RD}$ ($\overline{DS}$) or $\overline{CS}$, whichever deactivates first
[3] t_{DW} ends at $\overline{WR}$ (R/$\overline{W}$) or $\overline{CS}$, whichever deactivates first
[4] t_{DH} starts from $\overline{WR}$ (R/$\overline{W}$) or $\overline{CS}$, whichever deactivates first
[5] A/D must come before $\overline{CS}$ and $\overline{RD}$ or a $\overline{CS}$ and $\overline{WR}$ combination. The user has to guarantee this.

Timing Waveforms

Read Timing for Intel ($\overline{RD}$ and $\overline{WR}$ pulse) and Motorola ($\overline{DS}$ or $\overline{RD}$ pin tied to $\overline{CS}$, and R/$\overline{W}$)

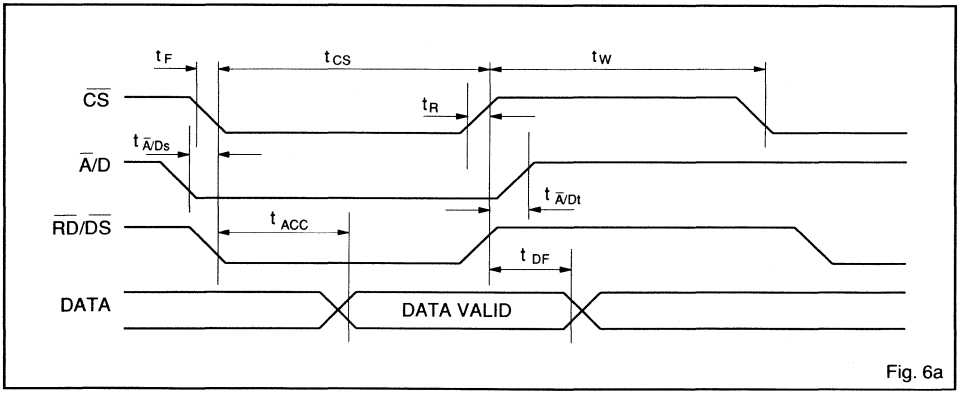


Fig. 6a

Intel Interface

Write Timing

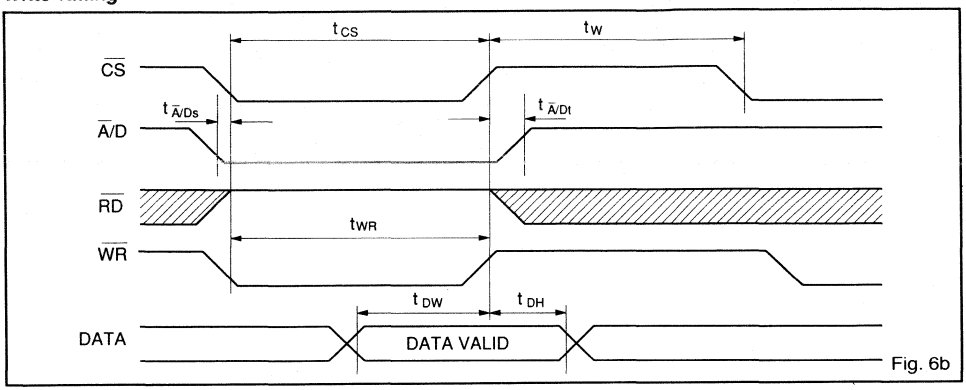


Fig. 6b

Write

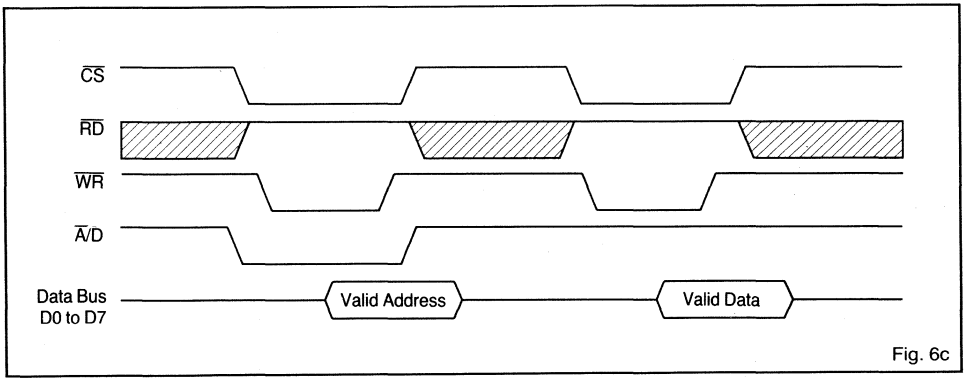


Fig. 6c

Read

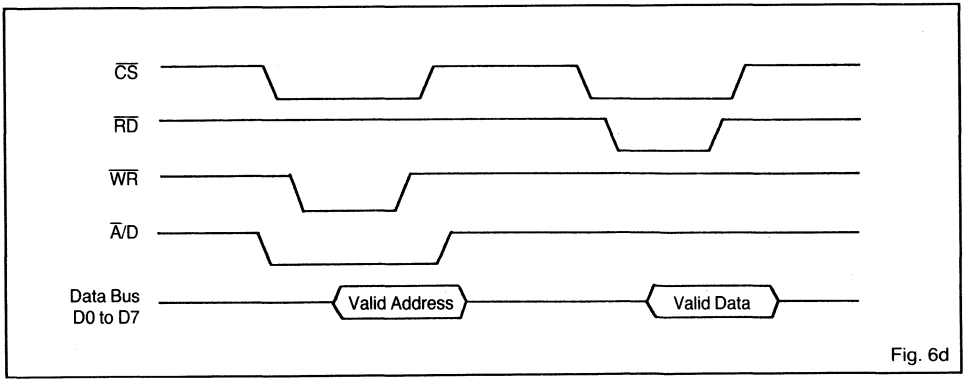


Fig. 6d

Motorola Interface

Motorola Write

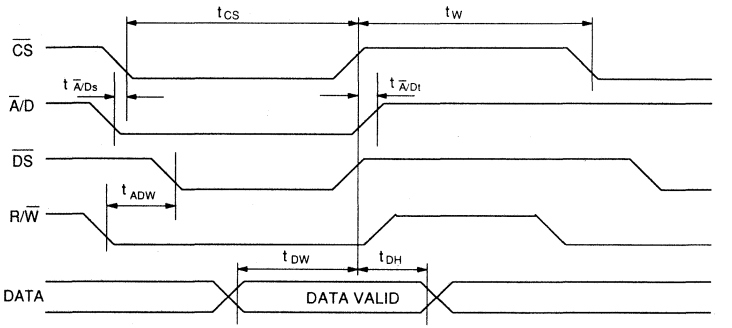


Fig. 6e

Write

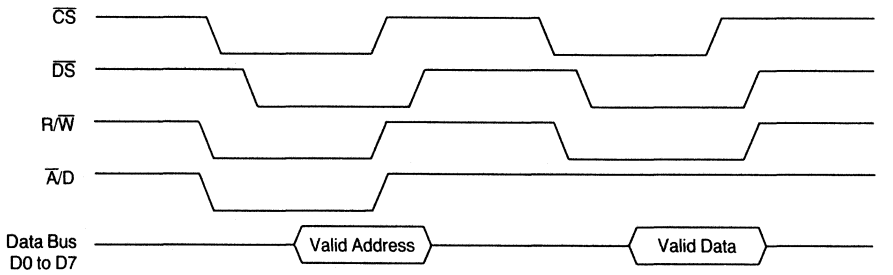


Fig. 6f

Read

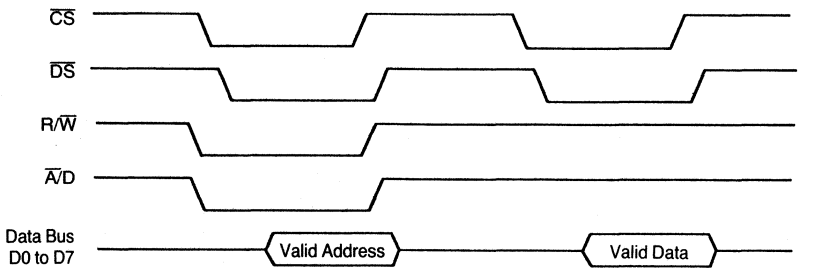


Fig. 6g

Block Diagram

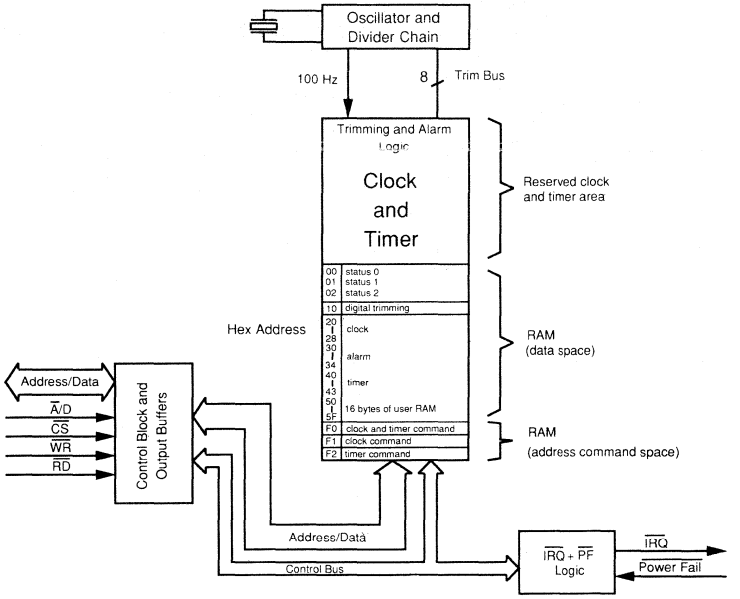


Fig. 7

Pin Description

DIP18 Package

Pin	Name	Description	
1	TEST	Do not connect, factory test pin	I
2	$\overline{PF}$	Power fail	I
3	AD0	Bit 0 from MUX address/data bus	I/O
4	AD1	Bit 1 from MUX address/data bus	I/O
5	AD2	Bit 2 from MUX address/data bus	I/O
6	AD3	Bit 3 from MUX address/data bus	I/O
7	$\overline{A/D}$	Address/data decode	I
8	$\overline{IRQ}$	Interrupt request	O
9	V_{SS}	Supply ground (substrate)	GND
10	V_{DD}	Positive supply terminal	PWR
11	$\overline{CS}$	Chip select	I
12	$\overline{WR}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola)	I
13	$\overline{RD}$	$\overline{RD}$ (Intel) or $\overline{DS}$ (Motorola)	I
14	AD4	Bit 4 from MUX address/data bus	I/O
15	AD5	Bit 5 from MUX address/data bus	I/O
16	AD6	Bit 6 from MUX address/data bus	I/O
17	AD7	Bit 7 from MUX address/data bus	I/O
18	NC	No connection	-

Table 5a

SO28 Package

Pin	Name	Description	
1	TEST	Do not connect, factory test pin	I
2	$\overline{PF}$	Power fail	I
3	AD0	Bit 0 from MUX address/data bus	I/O
4	AD1	Bit 1 from MUX address/data bus	I/O
5	NC	No connection	-
6	AD2	Bit 2 from MUX address/data bus	I/O
7	AD3	Bit 3 from MUX address/data bus	I/O
8	$\overline{A/D}$	Address/data decode	I
9	$\overline{IRQ}$	Interrupt request	O
10-14	V_{SS}	Supply ground (substrate)	GND
15-19	V_{DD}	Positive supply terminal	PWR
20	$\overline{CS}$	Chip select	I
21	$\overline{WR}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola)	I
22	$\overline{RD}$	$\overline{RD}$ (Intel) or $\overline{DS}$ (Motorola)	I
23	AD4	Bit 4 from MUX address/data bus	I/O
24	NC	No connection	-
25	AD5	Bit 5 from MUX address/data bus	I/O
26	AD6	Bit 6 from MUX address/data bus	I/O
27	AD7	Bit 7 from MUX address/data bus	I/O
28	NC	No connection	-

Table 5b

Functional Description

Data Retention and Standby

The V 3022 is put in standby mode by activating the $\overline{PF}$ input. When pulled logic low, $\overline{PF}$ will disable the input lines, and immediately take to high impedance the lines AD 0 - 7. Input states must be under control whenever $\overline{PF}$ is deactivated. If no specific power fail signal can be provided, $\overline{PF}$ can be tied to the system $\overline{RESET}$. Even in standby the interrupt request pin $\overline{IRQ}$ will pull to ground upon an unmasked alarm interrupt occurring.

Initialisation

When power is first applied to the V 3022 all registers have a random value.

To initialise the V 3022, software must first write a 1 to the initialisation bit (addr. 2 bit 4) and then a 0. This sets the Frequency Tuning bit and clears all other status bits.

The time and date parameters should then be loaded into the RAM (addr. 20 to 28 hex) and then transferred to the reserved clock area using the clock command followed by a write.

The digital trimming register must then be initialised by writing 210 (D2hex) to it, if Frequency Tuning is not required. After having written a value to the digital trimming register the frequency tuning mode bit can be cleared.

RAM Configuration

The RAM area of the V 3022 has a reserved clock and timer area, a data space, and an address command space (see Table 9 or Fig. 7). The reserved clock and timer area is not directly accessible to the user, it is used for internal time keeping and contains the current time and date plus the timer parameters.

Data Space

All locations in the data space are Read/Write. The data space is directly accessible to the user and is divided into five areas:

Status Registers - three registers used for status and control data for the device (see Tables 6, 7 and 8).

Digital Trimming Register - a special function described under "Frequency Tuning".

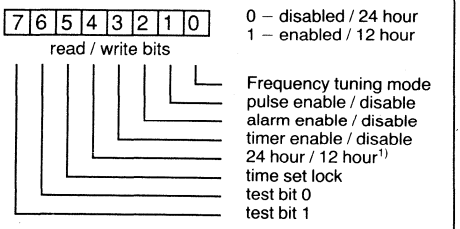
Time and Date Registers - 9 time and date locations which are loaded with, either the current time and date parameters from the reserved clock area or the time and date parameters to be tranferred to the reserved clock area.

Alarm Registers - 5 locations used for setting the alarm parameters.

Timer Registers - 4 locations which are loaded with either the timer parameters from the reserved timer area or the timer parameters to be transferred to the reserved timer area.

Status Words

Status 0 - Address 00 Hex



1) The alarm hours, address 33 hex, must always be rewritten after a change between 12 and 24 hour formats

Table 6

Status 1 - Address 01 Hex

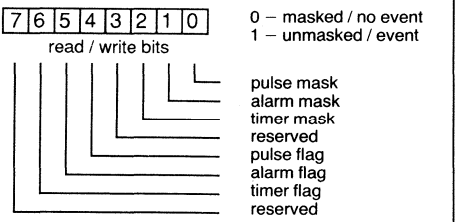


Table 7

Status 2 - Address 02 Hex

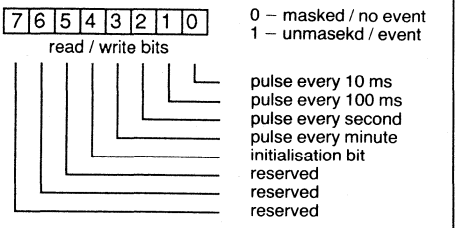


Table 8

Address Command Space

This space contains the three commands used for carrying out the transfers between the Time and Date Register and/or the Timer Registers and the reserved clock and timer area.

RAM Map

Address Dec	Hex	Parameter	Range
		Data Space	
Status			
00	00	status 0	
01	01	status 1	
02	02	status 2	
Special purpose			
16	10	digital trimming	0-255
Clock			
32	20	1/100 second	00-99
33	21	seconds	00-59
34	22	minutes	00-59
35	23	hours [1]	00-23
36	24	date	01-31
37	25	month	01-12
38	26	year	00-99
39	27	week day	01-07
40	28	week number	00-53
Alarm			
48	30	1/100 seconds	00-99
49	31	seconds	00-59
50	32	minutes	00-59
51	33	hours [1][2]	00-23
52	34	date	01-31
Timer			
64	40	1/100 seconds	00-99
65	41	seconds	00-59
66	42	minutes	00-59
67	43	hours	00-23
		Address Command Space	
240	F0	clock and timer transfer	
241	F1	clock transfer	
242	F2	timer transfer	

Table 9

[1] The MSB (bit 7) of the hours byte (addr. 23 hex for the clock and 33 hex for the alarm) are used as AM/PM indicators in the 12 hour time data format and reading of the hours byte must be preceded by masking of the AM/PM bit. A set AM/PM bit indicates PM. In the 24 hour time data format the bit will always be zero.

[2] The alarm hours, addr. 33 hex, must always be rewritten after a change between 12 and 24 hour modes.

Communication

Data transfer is in 8 bit parallel form. All time data is in packed BCD format with tens data on lines AD 7 - 4 and units on lines AD 3 - 0. To access information within the RAM (see Fig. 7) first write the RAM address, then read or write from or to this location. Fig. 8 shows the two steps needed.

The lines AD 0 - 7 will be treated as an address when pin $\overline{A}/D$ is low, and as data when $\overline{A}/D$ is high. Pin $\overline{A}/D$ must not change state during any single read or write access. One line of the address bus (e.g. A0) can be used to implement the $\overline{A}/D$ signal (see "Typical Operating Configuration", Fig. 1). Until a new address is written, data accesses ($\overline{A}/D$ high) will always be to the same RAM address.

Communication Sequence

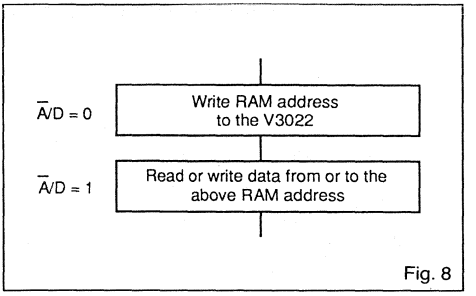


Fig. 8

Access Considerations

The communication sequence shown in Fig. 8 is re-entrant. When the address is written to the V 3022 (ie. first step of the communication sequence) it is stored in an internal address latch. Software can read the internal address latch at any time by holding the $\overline{A}/D$ line low during a read from the V 3022. So, for example, an interrupt routine can read the address latch and push it onto a stack, popping it when finished to restore the V 3022.
N.B. Alarm and timer interrupt routines can reprogram the alarm and timer without it being necessary to read or reprogram the clock.

Commands

The commands allow software to transfer the clock and timer parameters in a sequence (eg. seconds, minutes, hours, etc.), without any danger of an internal time update with carry over corrupting the data. They also avoid delaying internal time updates while using the V 3022, as updates occurring in the reserved clock and timer area are invisible to software. Software writes or reads parameters to or from the RAM only.
There are three commands that occupy the command address space in the RAM.
The function of these commands is to transfer data from the reserved clock and timer area to the RAM or to transfer data in the opposite direction, from the RAM to the reserved clock and timer area. The commands take place in two steps as do all other communications. The command address is sent with $\overline{A}/D$ low. This is followed by either a read ($\overline{RD}$) or a write ($\overline{WR}$), with $\overline{A}/D$ high, to determine the direction of the transfer. If the second step is a read then the data is transferred from the reserved clock and timer area to the RAM and if the second step is a write then the data that has already been loaded into the RAM clock and/or timer locations is transferred to the reserved clock and/or timer area.

Clock and Calendar

The time and date locations in RAM (see Table 9) provide access to the 1/100 seconds, seconds, minutes, hours, date, month, year, week day, and week number. These parameters have the ranges indicated in Table 9. The V 3022 can be programmed for 12 or 24 hour time format (see section "12/24 Data Format"). If a parameter is found to be out of range, it will be cleared when the units value on its being next incremented is equal to or greater than 9 eg. B2 will be set to 00 after the units have incremented to 9 (ie. B9 to 00). The device incorporates leap year correction and week number calculation at the beginning of a year. If the first day of the year is day 05, 06 or 07 of the week, then it is given a zero week number, otherwise it becomes week one. Week days are numbered from 1 to 7 with Monday as day 1.

Reading of the current time and date must be preceded by a clock command. The time and date from the last clock command is held unchanged in RAM.

When transferring data to the reserved clock and timer area remember to clear the time set lock bit first.

Timer

The timer can be used either for counting elapsed time, or for giving an interrupt ($\overline{IRQ}$) on being incremented from 23:59:59:99 to 00:00:00:00. The timer counts up with a resolution of 1/100 second in the timer reserved areas. The timer enable / disable bit (addr. 00 hex, bit 3) must be set by software to allow the timer to be incremented. The timer is incremented in the reserved timer area, every internal time update (10 ms). The timer flag (addr. 01 hex, bit 6) is set when the timer rolls over from 23:59:59:99 to 00:00:00:00 and the $\overline{IRQ}$ becomes active if the timer mask bit (addr. 01, bit 2) is set. The $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the timer flag. The timer is incremented in the standby mode, however it will not cause $\overline{IRQ}$ to become active until power (V_{DD}) has been restored.

Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the timer flag.

Reading the Clock

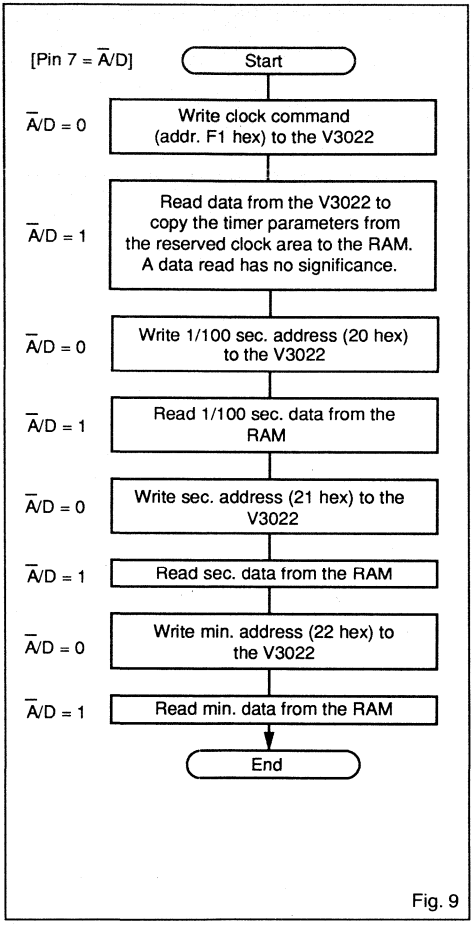


Fig. 9

Setting the Timer (Time Set Lock Bit = 0)

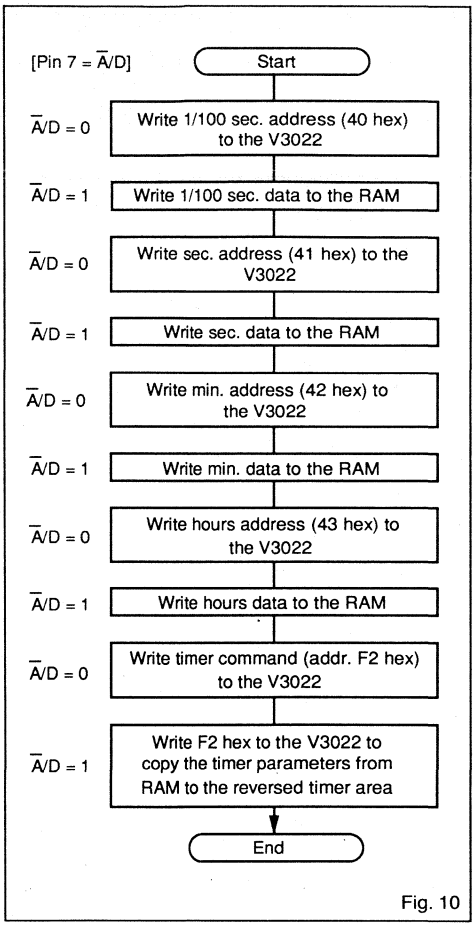


Fig. 10

Note: Commands are only valid as commands when the Ā/D line is low. Writing F2 hex with the Ā/D line high, as in the last box of Fig. 8, serves only to activate the V 3022 write pin which determines the direction of transfer.

Alarm

An alarm date and time may be preset in RAM addresses 30 to 34 hex. The alarm function can be activated by setting the alarm enable / disable bit (addr. 00 hex, bit 2). Once enabled the preset alarm time and date are compared, every internal time update cycle (10 ms), with the clock parameters in the reserved clock area. When the clock parameters equal the alarm parameters the alarm flag (addr. 01 hex, bit 5) is set. If the alarm mask bit (addr. 01 hex, bit 1) is set, the $\overline{IRQ}$ pin goes active. The alarm flag indicates to software the source of the interrupt. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the alarm flag. If the alarm is enabled, and an alarm address set to FF hex, this parameter is not compared with the associated clock parameter. Thus it is possible to achieve a repeat feature where an alarm occurs every programmed number of seconds, or seconds and minutes, or seconds, minutes and hours. The V 3022 pulls the open drain $\overline{IRQ}$ line active low during standby when an alarm interrupt occurs.

If the 12/24 hour mode is changed then the alarm hours must be re-initialised.

Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the alarm flag.

$\overline{IRQ}$

The $\overline{IRQ}$ output is used by 4 of the V 3022's features. These are:

1) Pulse, to provide periodic interrupts to the microprocessor at preprogrammed intervals;
2) Alarm to provide an interrupt to the microprocessor at a preprogrammed time and date;
3) Timer, to provide an interrupt to the microprocessor when the timer rolls over from 23:59:59:99 to 00:00:00:00; and
4) Frequency trimming (see section "Frequency Trimming").

The first 3 features listed are similar in the way they provide interrupts to the microprocessor. Each of the 3 has an enable / disable bit, a flag bit, and an interrupt mask bit. The enable / disable bit allows software to select a feature or not. A set flag bit indicates that an enabled feature has reached its interrupt condition. Software must clear the flag bit. The interrupt mask bit allows or disallows the $\overline{IRQ}$ output to become active when the flag bit is set. The $\overline{IRQ}$ output becomes active whenever any interrupt flag is set which also has its mask bit set. For all sources of maskable interrupts within the V 3022, the $\overline{IRQ}$ output will remain active until software clears the interrupt flag. The $\overline{IRQ}$ output is the logical OR of all the unmasked interrupt flags. The $\overline{IRQ}$ output is open drain so an external pullup to V_{DD} is needed. In standby ($\overline{PF}$ active) the $\overline{IRQ}$ output will be active if the alarm mask bit (addr. 01 hex, bit 1) is set and the alarm flag is also set. The timer or the pulse feature cannot cause the $\overline{IRQ}$ output to become active while in standby.

Pulse

There are 4 programmable pulse frequencies available on the V 3022, these are every 10 ms, 100 ms, second or minute. The pulse feature is activated by setting the pulse enable / disable bit at address 00, bit 1. The pulse frequency is selected by setting one of the bits 0 to 3 at address 02 hex (see Table 8). If more than one of the pulse bits are set then the feature is disabled. At the selected interval the pulse flag bit (addr. 01 hex, bit 4) is set. If the pulse mask bit (addr. 01 hex, bit 0) is set then the $\overline{IRQ}$ pin goes active. The pulse flag indicates to software the source of the interrupt. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the pulse flag. The pulse feature is disabled while in standby. Upon power restoration the pulse feature is enabled if enabled prior to standby. See also the section "Frequency Tuning".

Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the pulse flag.

Time Set Lock

The time set lock control bit is located at address 00 hex, bit 5 (see Table 6). When set by software, this bit disables any transfer from the RAM to the reserved clock and timer area as well as inhibiting any write to the digital trimming register at address 10 hex. When the time set lock bit is set the following transfer operations are disabled:

The clock command followed by write,
the timer command followed by write,
the clock and timer command followed by write, and
writing to the digital trimming register.

A set bit prevents unauthorized overwriting of the reserved clock and timer area. Reading of the reserved clock and timer area, using the commands, is not effected by the time set lock bit. Clearing the time set lock bit by software will re-enable the above listed commands. On initialisation the time set lock bit is cleared.

Frequency Tuning

The frequency tuning mode is entered during initialisation by writing a 1 to the initialisation bit (addr. 2, bit 4) followed by a 0. This sets the frequency tuning mode bit and places a pulsed signal with a 20% duty cycle on the $\overline{IRQ}$ pin for frequency measurement and digital trimming at addr. 10 hex. All measurements must be made relative to the falling edges.

The V 3022 can be digitally frequency tuned to within ± 0.5 ppm via the digital trimming register at addr. 10 hex. The trimming range is from 0 ppm to +255 ppm. The time keeping of the V 3022 is slowed by 1 ppm for each addition of 1 to the digital trimming register.

If the user does not want to use the digital trimming facility on the V 3022 then he must write 210 (D2hex) to the digital trimming register.

Ideally the period of the frequency tuning signal should be 10 ms. For every 10 ns of difference from the ideal period the V 3022 should be trimmed by +1 ppm in the digital trimming register (addr. 10 hex).

If the user wants to use the digital trimming facility then

he must first set the digital register to zero and measure the frequency of the pulses on the $\overline{IRQ}$ pin. The nominal frequency is 100 Hz and the number of ppm in excess for the sake of adjustment is shown by the three digits following the first zero after the decimal point. This number should be entered into the digital trimming register. For example, if the digital register is set to zero and 100.0150 appears at the $\overline{IRQ}$ pin then 150 (96 hex) must be entered into the digital trimming register. The frequency tuning mode is disabled by clearing the frequency tuning bit (addr. 00 hex, bit 0). The range of frequency values appearing at the $\overline{IRQ}$ pin when the digital trimming register is set to zero and with a normal crystal of 32.768 kHz, should be 100.0086 to 100.0286.

Time Correction with Change of Temperature

If greater time accuracy is needed and there is digitised temperature available the setting of the digital trimming register can be continuously altered to reflect the changing temperature. If, for example, the temperature was +75°C, the value entered into the digital trimming register according to the graph in Fig. 4 would be 210 − 100 = 110 ppm or 6E hex. All of the values corresponding to the different temperatures would be entered in a table. The values corresponding to temperatures that differ from 25°C should always be subtracted from 186 (BA hex) or the trimmed turnover value at 25°C.

12 / 24 Hour Data Format

The V 3022 can run in 12 hour or 24 hour data format. On initialisation the 12/24 hour bit addr. 00 bit 4 is cleared putting the V 3022 in 24 hour data format. If the 12 hour data format is required then bit 4 at addr. 00 must be set. In the 12 hour data format the AM/PM indicator is the MSB of the hours register addr. 23 bit 7. A set bit indicates PM. When reading the hours in the 12 hour data format software should mask the MSB of the hours register. In the 24 hour data format the MSB is always zero. The internal clock registers change automatically between 12 and 24 hour mode when the 12/24 hour bit is changed. **The alarm hours however must be rewritten.**

Test

From the various test features added to the V 3022 some may be activated by the user. Table 6 shows the test bits. Table 10 shows the three available modes and how they may be activated.

The first accelerates the incrementing of the parameters in the reserved clock and timer area by 32.

The second causes all clock and timer parameters, in the reserved clock and timer area, to be incremented in parallel at 100 Hz with no carry over, ie. independently of each other.

The third test mode combines the previous two resulting in parallel incrementing at 3.2 kHz.

While test bit 1 is set (addr. 00 hex, bit 7) the digital trimming action is disabled and no pulses are removed from the divider chain. Test bit 0 (addr. 00 hex, bit 6) can be combined with digital trimming (see section "Frequency Tuning").

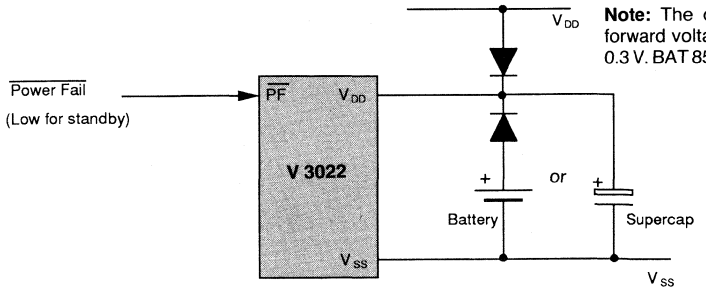
To leave test, the test bits (addr. 00 hex, bits 6 and 7) must be cleared by software. Test corrupts the clock and timer parameters and so all parameters should be re-initialised after a test session.

Test Modes

Addr. 00hex bit 7	Addr. 00 hex bit 6	Function
0	0	Normal operation
0	1	Acceleration by 32
1	0	Parallel increment of all clock and timer parameters at 100 Hz with no carry over; dependent on the status of bit 3 at address 00 hex
1	1	Parallel increment of all clock and timer parameters at 3.2 kHz with no carry over; dependent on the status of bit 3 at address 00 hex

Table 10

Battery or Supercap Connection



Note: The diodes must have a forward voltage drop of less than 0.3 V. BAT 85 s are recommended.

Fig. 11

Typical Applications

V 3022 Interfaced with Intel CPU ($\overline{RD}$ and $\overline{WR}$ pulse)

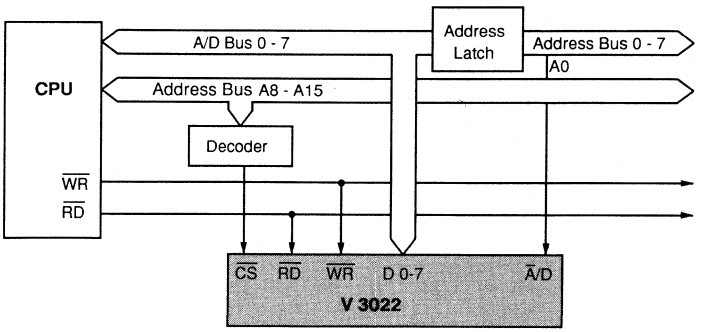


Fig. 12

V 3022 Interfaced with Motorola CPU ($\overline{DS}$ or $\overline{RD}$ pin tied to $\overline{CS}$, and R/$\overline{W}$)

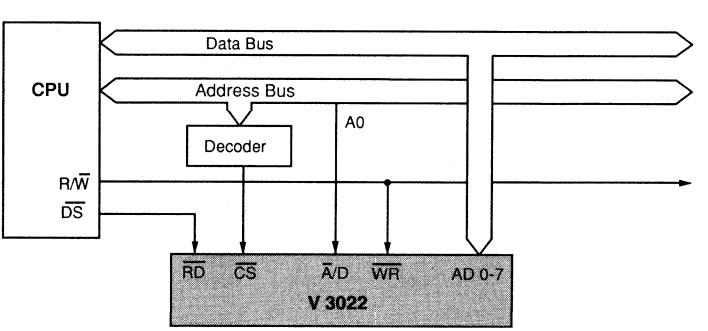


Fig. 13

Process Application

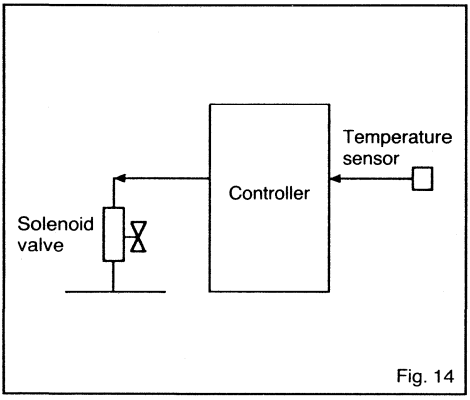
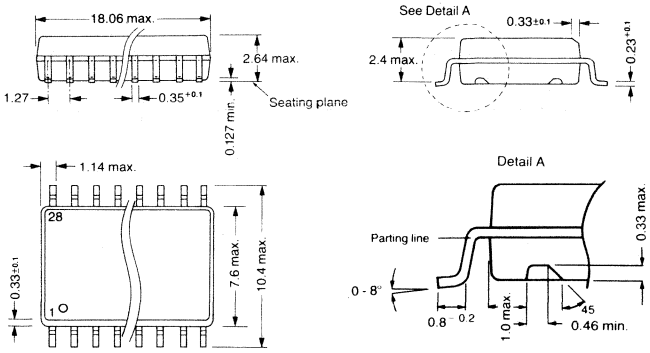


Fig. 14

- The formula in Fig. 5 is used by software to continually update the digital trimming register and so compensate the V 3022 for the ambient temperature.
- The timer is used to measure the duration the valve is on.
- The alarm feature is used to turn the controller power on and off at the time programmed by software. The V 3022 pulls $\overline{IRQ}$ active low on an alarm even in standby and thus can control the power on/off switch for the controller.

Package and Ordering Information

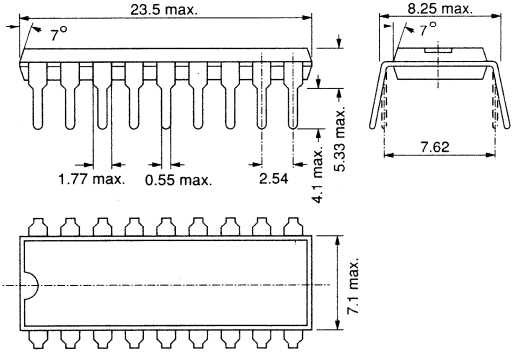
Dimensions of SO28 Package



Dimensions in mm

Fig. 15

Dimensions of DIP18 Package



Dimensions in mm

Fig. 16

Ordering Information

The V 3022 is available in the following packages:

DIP18 pin plastic package	V 3022 18P
SO28 pin plastic package	V 3022 28S

When ordering, please specify the complete part number and package.

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8 Bit Real Time Clock Module

Features

- 16 bytes of user RAM
- Can be synchronized to 50 Hz or nearest s/min
- **Built-in crystal with digital trimming and temperature compensation facilities**
- Standby on power down typically 1.2 μA
- Simple 8 bit interface with no delays or busy flags
- Universal interface compatible with both Intel and Motorola
- 50 ns access time
- Power fail input disables during power up / down or reset
- Bus can be tri-state in power fail mode
- Wide voltage range, 2.0 V to 5.5 V
- 12 or 24 hour data formats
- Time to 1/100 of a second
- Leap year correction and week number calculation
- Alarm and timer interrupts
- Programmable interrupts: 10 ms, 100 ms, s or min
- Sleep mode capability
- Alarm programmable up to one month
- Timer measures elapsed time up to 24 hours
- Packages DIP18 and SO28

Description

The V 3023 is a low power CMOS real time clock with a built-in crystal. Standby current is typically 1.2 μA and the access time is 50 ns. The interface is 8 bits with multiplexed address and data bus. Multiplexing of address and data is handled by the input line $\overline{A}$/D. There are no busy flags in the V 3023, internal time update cycles are invisible to the user's software. Time data can be read from the V 3023 in 12 or 24 hour data formats. An external signal puts the V 3023 in standby mode. Even in standby, the V 3023 pulls the $\overline{IRQ}$ pin active low on an internal alarm interrupt. Calendar functions include leap year correction and week number calculation. Time precision can be achieved by digital triming. The V 3023 can be synchronized to an external 50 Hz signal or to the nearest second or minute.

Applications

- Industrial controllers
- Alarm systems with periodic wake up
- PABX and telephone systems
- Point of sale terminals

Typical Operating Configuration

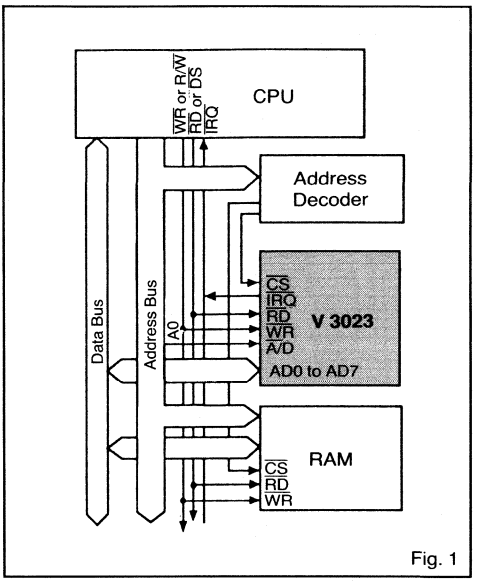


Fig. 1

Pin Assignment

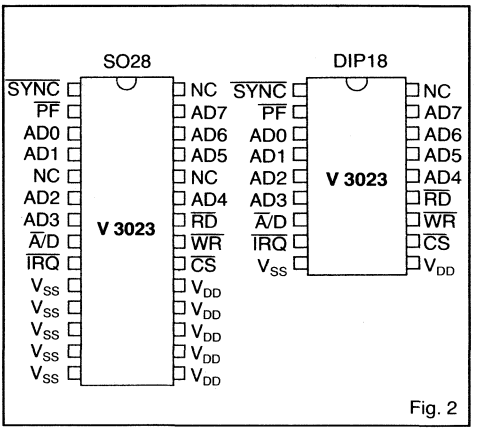


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS} + 7.0V
Max. voltage at remaining pins	V_{max}	V_{DD} + 0.3V
Min. voltage on all pins	V_{min}	V_{SS} − 0.3V
Maximum storage temperature	T_{STOmax}	+125°C
Minimum storage temperature	T_{STOmin}	−55°C
Maximum electrostatic discharge to MIL-STD-883C method 3015	V_{Smax}	1000V
Maximum soldering conditions	T_{Smax}	250°C x 10 s
Shock resistance		5000 g, 0.3 ms, ½ sine

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	+2.0	+5.0	+5.5	V
Supply voltage dv/dt (power-up and down)	dv/dt			6	V/µs
Decoupling capacitor			100		nF

Table 2

Electrical Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = −40°C to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby current	I_{DD}	V_{DD} = 3 V, $T_A \leq 25°C$, $\overline{PF}$ = 0		1.2		µA
		V_{DD} = 3 V, $\overline{PF}$ = 0			15	µA
		$T_A \leq 25°C$, $\overline{PF}$ = 0		2		µA
Dynamic current	I_{DD}	all outputs open, CS = 4 MHz, $\overline{RD} = V_{SS}$, $\overline{WR} = V_{DD}$ [1]			1.5	mA
$\overline{IRQ}$ (open drain)						
Output low voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Output low voltage	V_{OL}	I_{OL} = 1 mA, V_{DD} = 2 V			0.4	V
Inputs and Outputs						
Input logic low	V_{IL}	T_A = 25°C			0.2 · V_{DD}	V
Input logic high	V_{IH}	T_A = 25°C	0.8 · V_{DD}			V
Output logic low	V_{OL}	I_{OL} = 6 mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 6 mA	2.4			V
$\overline{PF}$ activation voltage	V_{PFL}			0.5 · V_{DD}		V
$\overline{PF}$ hysteresis	V_H	T_A = 25°C		100		mV
Pullup on $\overline{SYNC}$	I_{LS}	V_{ILS} = 0.8 V	20			µA
Input leakage	I_{IN}	$V_{SS} < V_{IN} < V_{DD}$		10	1000	nA
Output tri-state leakage	I_{TS}	$\overline{CS}$ = 1		10	1000	nA
Oscillator Characteristics						
Starting voltage	V_{STA}	$T_A \geq 25°C$	2			V
				2.5		V
Frequency Characteristics						
Start-up time	T_{STA}			1		s
Frequency tolerance	$\Delta f/f$	T_A = 25°C addr. 10 hex = 00 hex	150	210[3]	255	ppm
Frequency stability	f_{sta}	2 V ≤ V_{DD} ≤ 5.5 V[2]		1	5	ppm/V
Temperature stability	t_{sta}	addr. 10 hex = 00 hex		see Fig. 5		ppm
Aging	t_{ag}	T_A = 25°C, first year			± 5	ppm/year

[1] Dynamic current is measured with all inputs to V_{DD} and all outputs open.
[2] At a given temperature.
[3] See Fig. 4

Table 3

Typical Standby Current at V_{DD} = 5 V

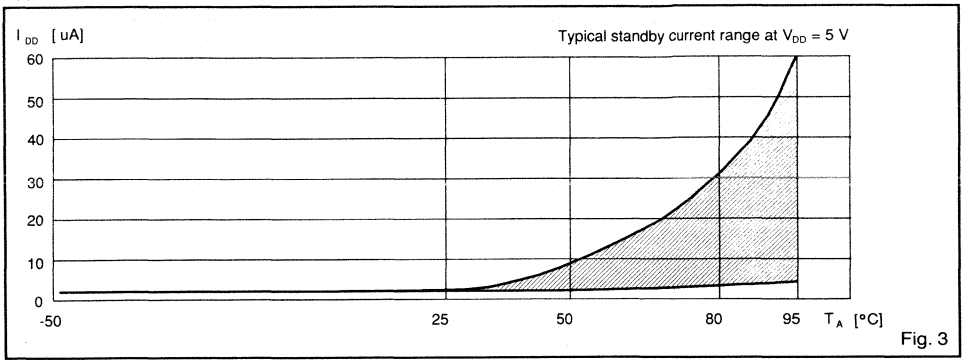


Fig. 3

Typical Frequency on $\overline{IRQ}$

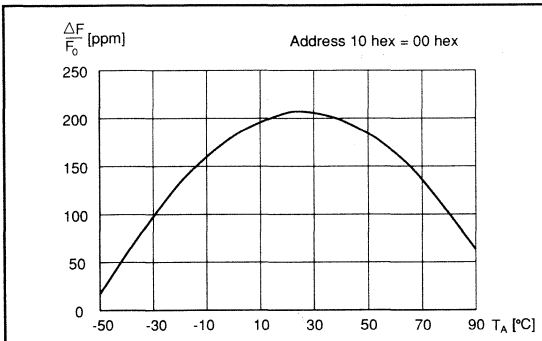
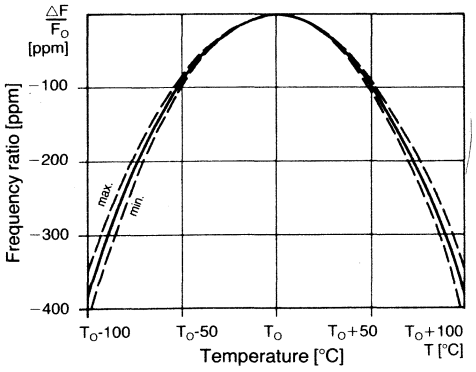


Fig. 4

Module Characteristic



$$\frac{\Delta F}{F_O} = -0.038 \frac{ppm}{°C^2} (T - T_O)^2 \pm 10\%$$

$\Delta F/FO$ = the ratio of the change in frequency to the nominal value expressed in ppm (It can be thought of as the frequency deviation at any temperature.)

T = the temperature of interest in °C

T_O = the turnover temperature (25 ± 5°C)

To determine the clock error (accuracy) at a given temperature, add the frequency tolerance at 25°C to the value obtained from the formula above.

Fig. 5

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, and T_A = −40°C to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Chip select duration, write cycle	t_{CS}		50			ns
Write pulse duration	t_{WR}		50			ns
Time between two transfers	t_W		100			ns
RAM access time[1]	t_{ACC}	C_{LOAD} = 50 pF		50	60	ns
Data valid to Hi-impedance[2]	t_{DF}		10	30	40	ns
Write data settle time[3]	t_{DW}		50			ns
Data hold time[4]	t_{DH}		10			ns
Advance write time	t_{ADW}		10			ns
$\overline{PF}$ response delay	t_{PF}				100	ns
Rise time (all timing waveform signals)	t_R				200	ns
Fall time (all timing waveform signals)	t_F				200	ns
$\overline{CS}$ delay after $\overline{A}$/D[5]	$t_{\overline{A}/Ds}$		5			ns
$\overline{CS}$ delay to $\overline{A}$/D	$t_{\overline{A}/Dt}$		10			ns

Table 4

[1] t_{ACC} starts from $\overline{RD}$ ($\overline{DS}$) or $\overline{CS}$, whichever activates last
[2] t_{DF} starts from $\overline{RD}$ ($\overline{DS}$) or $\overline{CS}$, whichever deactivates first
[3] t_{DW} ends at $\overline{WR}$ (R/$\overline{W}$) or $\overline{CS}$, whichever deactivates first
[4] t_{DH} starts from $\overline{WR}$ (R/$\overline{W}$) or $\overline{CS}$, whichever deactivates first
[5] $\overline{A}$/D must come before a $\overline{CS}$ and $\overline{RD}$ or a $\overline{CS}$ and $\overline{WR}$ combination. The user has to guarantee this.

Timing Waveforms

Read Timing for Intel ($\overline{RD}$ and $\overline{WR}$ pulse) and Motorola ($\overline{DS}$ or $\overline{RD}$ pin tied to $\overline{CS}$, and R/$\overline{W}$)

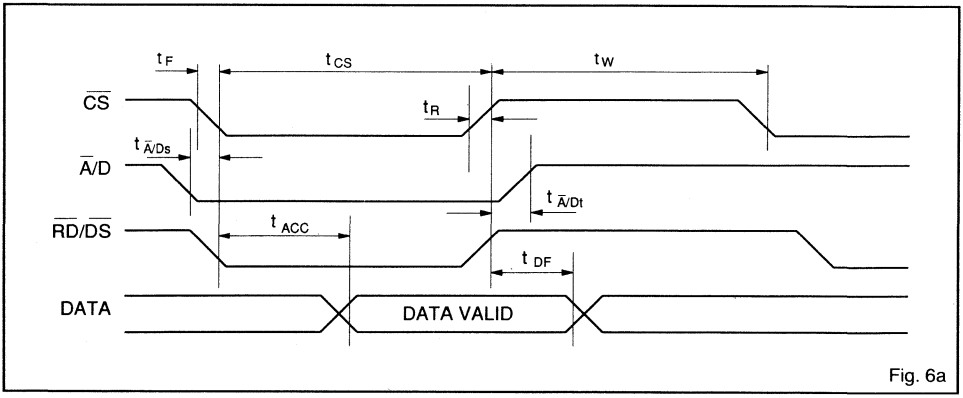


Fig. 6a

Intel Interface

Write Timing

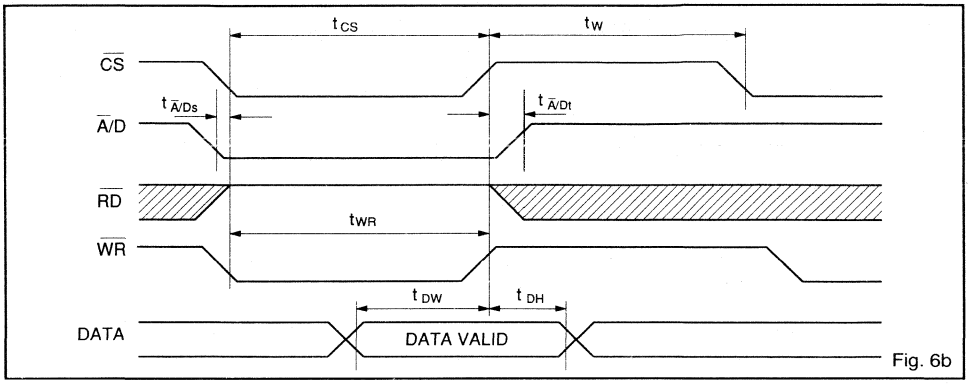


Fig. 6b

Write

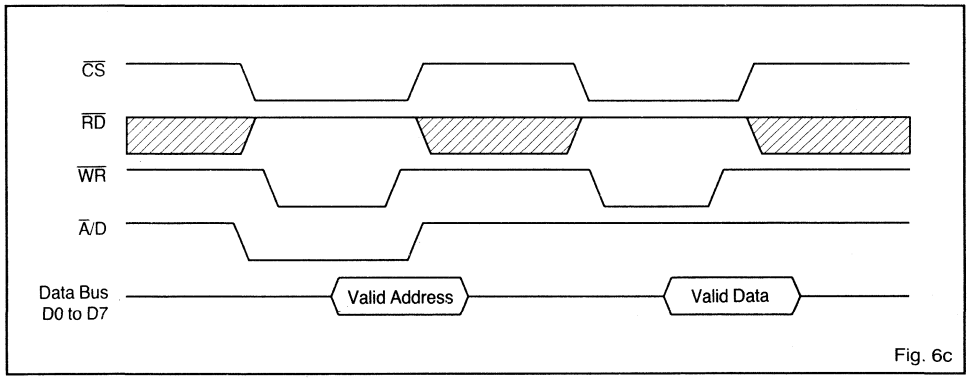


Fig. 6c

Read

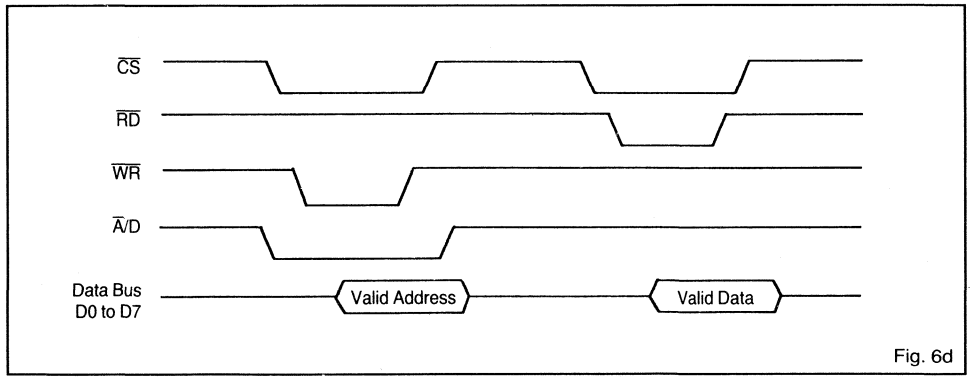


Fig. 6d

Motorola Interface

Motorola Write

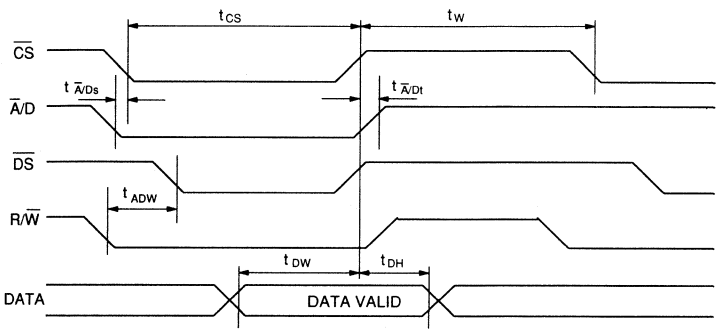


Fig. 6e

Write

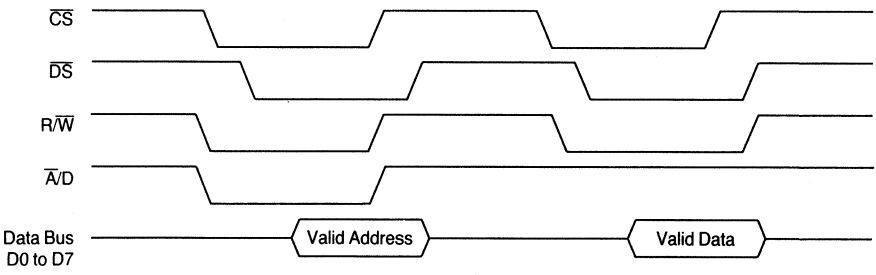


Fig. 6f

Read

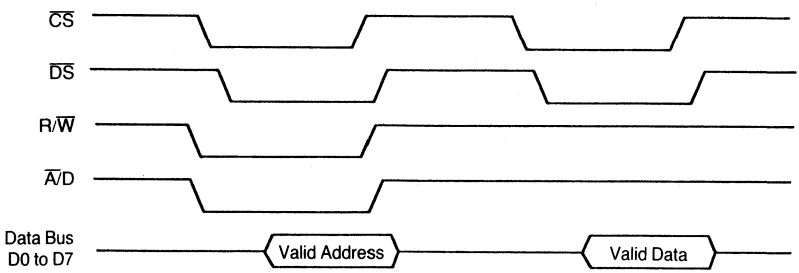


Fig. 6g

Block Diagram

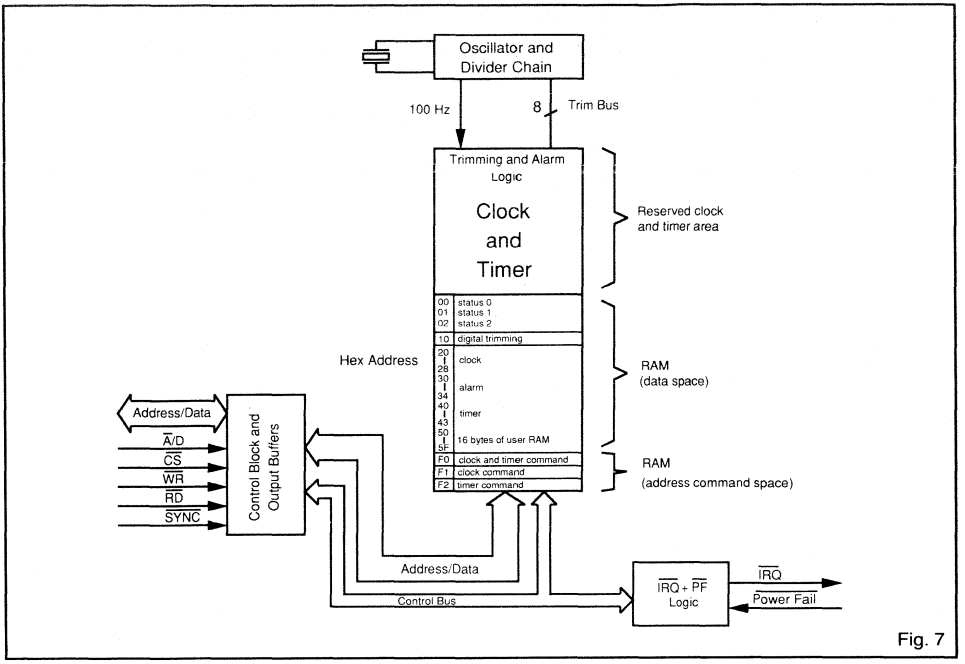


Fig. 7

Pin Description

DIP18 Package

Pin	Name	Description	
1	$\overline{SYNC}$	Time synchronization	I
2	$\overline{PF}$	Power fail	I
3	AD0	Bit 0 from MUX address/data bus	I/O
4	AD1	Bit 1 from MUX address/data bus	I/O
5	AD2	Bit 2 from MUX address/data bus	I/O
6	AD3	Bit 3 from MUX address/data bus	I/O
7	A/D	Address/data decode	I
8	$\overline{IRQ}$	Interrupt request	O
9	V_{SS}	Supply ground (substrate)	GND
10	V_{DD}	Positive supply terminal	PWR
11	$\overline{CS}$	Chip select	I
12	$\overline{WR}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola)	I
13	$\overline{RD}$	$\overline{RD}$ (Intel) or $\overline{DS}$ (Motorola)	I
14	AD4	Bit 4 from MUX address/data bus	I/O
15	AD5	Bit 5 from MUX address/data bus	I/O
16	AD6	Bit 6 from MUX address/data bus	I/O
17	AD7	Bit 7 from MUX address/data bus	I/O
18	NC	No connection	-

Table 5a

SO28 Package

Pin	Name	Description	
1	$\overline{SYNC}$	Time synchronization	I
2	$\overline{PF}$	Power fail	I
3	AD0	Bit 0 from MUX address/data bus	I/O
4	AD1	Bit 1 from MUX address/data bus	I/O
5	NC	No connection	-
6	AD2	Bit 2 from MUX address/data bus	I/O
7	AD3	Bit 3 from MUX address/data bus	I/O
8	A/D	Address/data decode	I
9	$\overline{IRQ}$	Interrupt request	O
10-14	V_{SS}	Supply ground (substrate)	GND
15-19	V_{DD}	Positive supply terminal	PWR
20	$\overline{CS}$	Chip select	I
21	$\overline{WR}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola)	I
22	$\overline{RD}$	$\overline{RD}$ (Intel) or $\overline{DS}$ (Motorola)	I
23	AD4	Bit 4 from MUX address/data bus	I/O
24	NC	No connection	-
25	AD5	Bit 5 from MUX address/data bus	I/O
26	AD6	Bit 6 from MUX address/data bus	I/O
27	AD7	Bit 7 from MUX address/data bus	I/O
28	NC	No connection	-

Table 5b

Functional Description

Power Supply, Data Retention and Standby

The V 3023 is put in standby mode by activating the $\overline{PF}$ input. When pulled logic low, $\overline{PF}$ will disable the input lines, and immediately take to high impedance the lines AD 0 - 7. Input states must be under control whenever $\overline{PF}$ is deactivated. If no specific power fail signal can be provided, $\overline{PF}$ can be tied to the system $\overline{RESET}$. Even in standby the interrupt request pin $\overline{IRQ}$ will pull to ground upon an unmasked alarm interrupt occurring.

Initialisation

When power is first applied to the V 3022 all registers have a random value.

To initialise the V 3023, software must first write a 1 to the initialisation bit (addr. 2 bit 4) and then a 0. This sets the Frequency Tuning bit and clears all other status bits.

The time and date parameters should then be loaded into the RAM (addr. 20 to 28 hex) and then transferred to the reserved clock area using the clock command followed by a write.

The digital trimming register must then be initialised by writing 210 (D2hex) to it, if Frequency Tuning is not required. After having written a value to the digital trimming register the frequency tuning mode bit can be cleared.

RAM Configuration

The RAM area of the V 3023 has a reserved clock and timer area, a data space, user RAM and an address command space (see Table 9 or Fig. 7). The reserved clock and timer area is not directly accessible to the user, it is used for internal time keeping and contains the current time and date plus the timer parameters.

Data Space

All locations in the data space are Read/Write. The data space is directly accessible to the user and is divided into five areas:

Status Registers - three registers used for status and control data for the device (see Tables 6, 7 and 8).

Digital Trimming Register - a special function described under "Frequency Tuning".

Time and Date Registers - 9 time and date locations which are loaded with, either the current time and date parameters from the reserved clock area or the time and date parameters to be tranferred to the reserved clock area.

Alarm Registers - 5 locations used for setting the alarm parameters.

Timer Registers - 4 locations which are loaded with either the timer parameters from the reserved timer area or the timer parameters to be transferred to the reserved timer area.

User RAM

The V 3023 has 16 bytes of general purpose RAM available for the users applications. This RAM block is located at addresses 50 to 5F hex and is maintained even in the standby mode ($\overline{PF}$ active). The commandes, or the time set lock bit, have no effect on the user RAM block. Reading or writing to the user RAM is similar to reading or writing to any system RAM address.

Status Words

Status 0 - Address 00 Hex

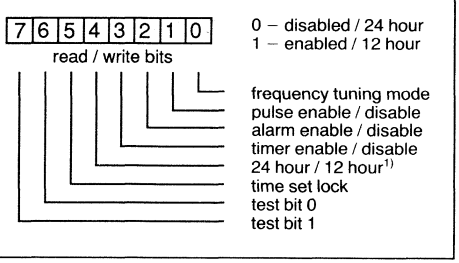


Table 6

Status 1 - Address 01 Hex

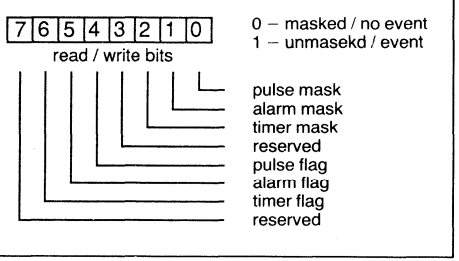


Table 7

Status 2 - Address 02 Hex

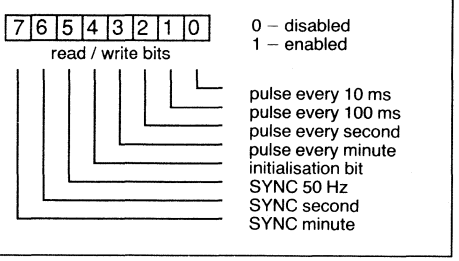


Table 8

Address Command Space

This space contains the three commands used for carrying out the transfers between the Time and Date Register and/or the Timer Registers and the reserved clock and timer area.

RAM Map

Address Dec	Address Hex	Parameter	Range
		Data Space	
Status			
00	00	status 0	
01	01	status 1	
02	02	status 2	
Special purpose			
16	10	digital trimming	0-255
Clock			
32	20	1/100 second	00-99
33	21	seconds	00-59
34	22	minutes	00-59
35	23	hours [1]	00-23
36	24	date	01-31
37	25	month	01-12
38	26	year	00-99
39	27	week day	01-07
40	28	week number	00-53
Alarm			
48	30	1/100 seconds	00-99
49	31	seconds	00-59
50	32	minutes	00-59
51	33	hours [1][2]	00-23
52	34	date	01-31
Timer			
64	40	1/100 seconds	00-99
65	41	seconds	00-59
66	42	minutes	00-59
67	43	hours	00-23
User RAM			
80	50	user RAM, byte 0	
81	51	user RAM, byte 1	
82	52	user RAM, byte 2	
83	53	user RAM, byte 3	
84	54	user RAM, byte 4	
85	55	user RAM, byte 5	
86	56	user RAM, byte 6	
87	57	user RAM, byte 7	
88	58	user RAM, byte 8	
89	59	user RAM, byte 9	
90	5A	user RAM, byte 10	
91	5B	user RAM, byte 11	
92	5C	user RAM, byte 12	
93	5D	user RAM, byte 13	
94	5E	user RAM, byte 14	
95	5F	user RAM, byte 15	
		Address Command Space	
240	F0	clock and timer transfer	
241	F1	clock transfer	
242	F2	timer transfer	

Table 9

[1] The MSB (bit 7) of the hours byte (addr. 23 hex for the clock and 33 hex for the alarm) are used as AM/PM indicators in the 12 hour time data format and reading of the hours byte must be preceded by masking of the AM/PM bit. A set AM/PM bit indicates PM. In the 24 hour time data format the bit will always be zero.

[2] The alarm hours, addr. 33 hex, must always be rewritten after a change between 12 and 24 hour modes.

Communication

Data transfer is in 8 bit parallel form. All time data is in packed BCD format with tens data on lines AD 7 - 4 and units on lines AD 3 - 0. To access information within the RAM (see Fig. 7) first write the RAM address, then read or write from or to this location. Fig. 8 shows the two steps needed.

The lines AD 0 - 7 will be treated as an address when pin $\overline{A}$/D is low, and as data when $\overline{A}$/D is high. Pin $\overline{A}$/D must not change state during any single read or write access. One line of the address bus (e.g. A0) can be used to implement the $\overline{A}$/D signal (see "Typical Operating Configuration", Fig. 1). Until a new address is written, data accesses ($\overline{A}$/D high) will always be to the same RAM address.

Communication Sequence

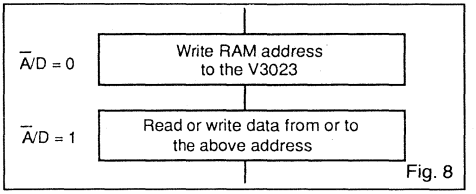


Fig. 8

Access Considerations

The communication sequence shown in Fig. 8 is re-entrant. When the address is written to the V 3023 (ie. first step of the communication sequence) it is stored in an internal address latch. Software can read the internal address latch at any time by holding the $\overline{A}$/D line low during a read from the V 3023. So, for example, an interrupt routine can read the address latch and push it onto a stack, popping it when finished to restore the V 3023. NB. Alarm and timer interrupt routines can reprogram the alarm and timer without it being necessary to read or reprogram the clock.

Commands

The commands allow software to transfer the clock and timer parameters in a sequence (eg. seconds, minutes, hours, etc.) without any danger of an internal time update with carry over corrupting the data. They also avoid delaying internal time updates while using the V 3023, as updates occuring in the reserved clock and timer area are invisible to software. Software writes or reads parameters to or from the RAM only.

There are three commands that occupy the command address space in the RAM. The function of these commands is to transfer data from the reserved clock and timer area to the RAM or to transfer data in the opposite direction, from the RAM to the reserved clock and timer area.

The commands take place in twqo steps as do all other communications. The command address is sent with

$\overline{A/D}$ low. This is followed by either a read ($\overline{RD}$) or a write ($\overline{WR}$), with $\overline{A/D}$ high, to determine the direction of the transfer. If the second step is a read then the data is transferred from the reserved clock and timer area to the RAM and if the second step is a write then the data that has already been loaded into the RAM clock and/or timer locations is transferred to the reserved clock and/or timer area.

Clock and Calendar

The time and date locations in RAM (see Table 9) provide access to the 1/100 seconds, seconds, minutes, hours, date, month, year, week day, and week number. These parameters have the ranges indicated in Table 9. The V 3023 may be programmed for 12 or 24 hour time format (see section "12/24 Data Format"). If a parameter is found to be out of range, it will be cleared when the units value on its being next incremented is equal to or greater than 9 eg. B2 will be set to 00 after the units have incremented to 9 (ie. B9 to 00). The device incorporates leap year correction and week number calculation at the beginning of a year. If the first day of the year is day 05, 06 or 07 of the week, then it is given a zero week number, otherwise it becomes week one. Week days are numbered from 1 to 7 with Monday as day 1.

Reading of the current time and date must be preceded by a clock command. The time and date from the last clock command is held unchanged in RAM.

When transferring data to the reserved clock and timer area remember to clear the time set lock bit first.

Timer

The timer can be used either for counting elapsed time, or for giving an interrupt ($\overline{IRQ}$) on being incremented from 23:59:59:99 to 00:00:00:00. The timer counts up with a resolution of 1/100 second in the timer reserved areas. The timer enable / disable bit (addr. 00 hex, bit 3) must be set by software to allow the timer to be incremented. The timer is incremented in the reserved timer area, every internal time update (10 ms). The timer flag (addr. 01 hex, bit 6) is set when the timer rolls over from 23:59:59:99 to 00:00:00:00 and the IRQ becomes active if the timer mask bit (addr. 01, bit 2) is set. The $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the timer flag. The timer is incremented in the standby mode, however it will not cause $\overline{IRQ}$ to become active until power (V_{DD}) has been restored.

Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the timer flag.

Reading the Clock

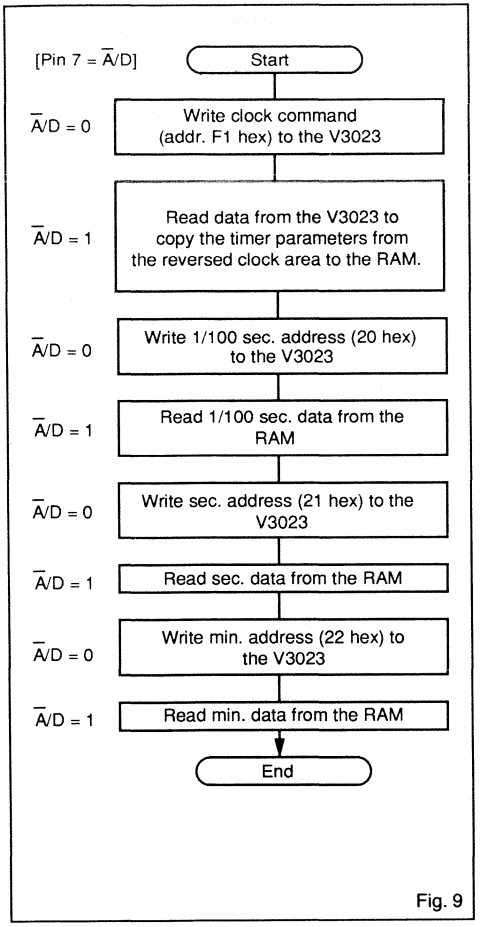


Fig. 9

Setting the Timer (Time Set Lock Bit = 0)

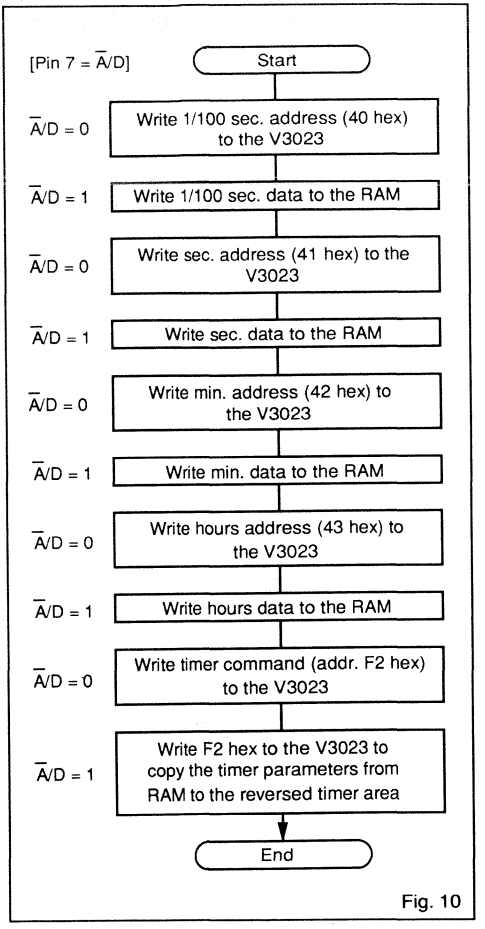


Fig. 10

Note: Commands are only valid as commands when the $\overline{A}$/D line is low. Writing F2 hex with the $\overline{A}$/D line high, as in the last box of Fig. 8, serves only to activate the V 3023 write pin which determines the direction of transfer.

Alarm
An alarm date and time may be preset in RAM addresses 30 to 34 hex. The alarm function can be activated by setting the alarm enable / disable bit (addr. 00 hex, bit 2). Once enabled the preset alarm time and date are compared, every internal time update cycle (10 ms), with the clock parameters in the reserved clock area. When the clock parameters equal the alarm parameters the alarm flag (addr. 01 hex, bit 5) is set. If the alarm mask bit (addr. 01 hex, bit 1) is set, the $\overline{IRQ}$ pin goes active. The alarm flag indicates to software the source of the interrupt. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the alarm flag. If the alarm is enabled, and an alarm address set to FF hex, this parameter is not compared with the associated clock parameter. Thus it is possible to achieve a repeat feature where an alarm occurs every programmed number of seconds, or seconds and minutes, or seconds, minutes and hours. The V 3023 pulls the open drain $\overline{IRQ}$ line active low during standby when an alarm interrupt occurs.
If the 12/24 hour mode is changed then the alarm hours must be re-initialised.
Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the alarm flag.

$\overline{IRQ}$
The $\overline{IRQ}$ output is used by 4 of the V 3023's features. These are:
1) Pulse, to provide periodic interrupts to the microprocessor at preprogrammed intervals;
2) Alarm to provide an interrupt to the microprocessor at a preprogrammed time and date;
3) Timer, to provide an interrupt to the microprocessor when the timer rolls over from 23:59:59:99 to 00:00:00:00; and
4) Frequency trimming (see section "Frequency Trimming").

The first 3 features listed are similar in the way they provide interrupts to the microprocessor. Each of the 3 has an enable / disable bit, a flag bit, and an interrupt mask bit. The enable / disable bit allows software to select a feature or not. A set flag bit indicates that an enabled feature has reached its interrupt condition. Software must clear the flag bit. The interrupt mask bit allows or disallows the $\overline{IRQ}$ output to become active when the flag bit is set. The $\overline{IRQ}$ output becomes active whenever any interrupt flag is set which also has its mask bit set. For all sources of maskable interrupts within the V 3023, the $\overline{IRQ}$ output will remain active until software clears the interrupt flag. The $\overline{IRQ}$ output is the logical OR of all the unmasked interrupt flags. The $\overline{IRQ}$ output is open drain so an external pullup to V_{DD} is needed. In standby ($\overline{PF}$ active) the $\overline{IRQ}$ output will be active if the alarm mask bit (addr. 01 hex, bit 1) is set and the alarm flag is also set. The timer or the pulse feature cannot cause the $\overline{IRQ}$ output to become active while in standby.

Synchronization
There are 3 ways to synchronize the V 3023. It can be synchronized to 50 Hz, the nearest second, or the nearest minute. Synchronization mode is selected by setting one of the bits 5 to 7 at addr. 02 hex, in accordance with Table 8. If more than one bit is set then all the synchronization bits are disabled. If the $\overline{SYNC}$ input is set low for longer than 200 μs, while in the synchronization mode, the clock will synchronize to the falling edge of the signal. Synchronization to the nearest second implies that the 1/100 seconds are cleared to zero and if the contents were > 50, the seconds register is incremented. Synchronization to the nearest minute implies that the seconds are cleared to zero and if the contents were $>$ 30, the minutes register is incremented. Fractions of seconds are cleared.

Pulse
There are 4 programmable pulse frequencies available on the V 3023, these are every 10 ms, 100 ms, second or minute. The pulse feature is activated by setting the pulse enable / disable bit at address 00, bit 1. The pulse frequency is selected by setting one of the bits 0 to 3 at address 02 hex (see Table 8). If more than one of the pulse bits are set then the feature is disabled. At the selected interval the pulse flag bit (addr. 01 hex, bit 4) is set. If the pulse mask bit (addr. 01 hex, bit 0) is set then the $\overline{IRQ}$ pin goes active. The pulse flag indicates to software the source of the interrupt. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the pulse flag. The pulse feature is disabled while in standby. Upon power restoration the pulse feature is enabled if enabled prior to standby. See also the section "Frequency Tuning".
Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the pulse flag.

Time Set Lock
The time set lock control bit is located at address 00 hex, bit 5 (see Table 6). When set by software, this bit disables any transfer from the RAM to the reserved clock and timer area as well as inhibiting any write to the digital trimming register at address 10 hex. When the time set lock bit is set the following transfer operations are disabled:
The clock command followed by write,
the timer command followed by write,
the clock and timer command followed by write, and
writing to the digital trimming register.
A set bit prevents unauthorized overwriting of the reserved clock and timer area. Reading of the reserved clock and timer area, using the commands, is not effected by the time set lock bit. Clearing the time set lock bit by software will re-enable the above listed commands. On initialisation the time set lock bit is cleared. The time set lock bit does not affect the user RAM (addr. 50 to 5F hex).

Frequency Tuning
The frequency tuning mode is entered during initialisation by writing a 1 to the initialisation bit (addr. 2 bit 4) followed by a 0. This sets the frequency tuning mode bit and places a pulsed signal with a 20% duty cycle on the $\overline{IRQ}$ pin for frequency measurement and digital trimming at addr. 10 hex. All measurements must be made rela-

tive to the falling edges.
The V 3023 can be digitally frequency tuned to within ±0.5 ppm via the digital trimming register at addr. 10 hex. The trimming range is from 0 ppm to +255 ppm. The time keeping of the V 3023 is slowed by 1 ppm for each addition of 1 to the digital trimming register.
If the user does not want to use the digital trimming facility on the V 3023 then he must write 210 (D2hex) to the digital trimming register.
Ideally the period of the frequency tuning signal should be 10 ms. For every 10 ns of difference from the ideal period the V 3023 should be trimmed by +1 ppm in the digital trimming register (addr. 10 hex).
If the user wants to use the digital trimming facility then he must first set the digital register to zero and measure the frequency of the pulses on the $\overline{IRQ}$ pin. The nominal frequency is 100 Hz and the number of ppm in excess for the sake of adjustment is shown by the three digits following the first zero after the decimal point. This number should be entered into the digital trimming register. For example, if the digital register is set to zero and 100.0150 appears at the $\overline{IRQ}$ pin then 150 (96 hex) must be entered into the digital trimming register. The frequency tuning mode is disabled by clearing the frequency tuning bit (addr. 00 hex, bit 0). The range of frequency values appearing at the $\overline{IRQ}$ pin when the digital trimming register is set to zero and with a normal crystal of 32.768 kHz, should be 100.0086 to 100.0286.

Time Correction with Change of Temperature
If greater time accuracy is needed and there is digitised temperature available the setting of the digital trimming register can be continuously altered to reflect the changing temperature. If, for example, the temperature was +75°C, the value entered into the digital trimming register according to the graph in Fig. 5 would be 210 − 100 = 110 ppm or 6E hex. All of the values corresponding to the different temperatures would be entered in a table. The values corresponding to temperatures that differ from 25°C should always be subtracted from 186 (BA-hex) or the trimmed turnover value at 25°C.

12 / 24 Hour Data Format
The V 3023 can run in 12 hour or 24 hour data format. On initialisation the 12/24 hour bit ad addr. 00 bit 4 is cleared putting the V 3023 in 24 hour data format. If the 12 hour data format is required then bit 4 at addr. 00 must be set.
In the 12 hour data format the AM/PM indicator is the MSB of the hours register addr. 23 bit 7. A set bit indicates PM. When reading the hours in the 12 hour data format software should mask the MSB of the hours register.
In the 24 hour data format the MSB is always zero.
The internal clock registers change automatically between 12 and 24 hour mode when the 24/12 hour bit is changed. **The alarm hours however must be rewritten.**

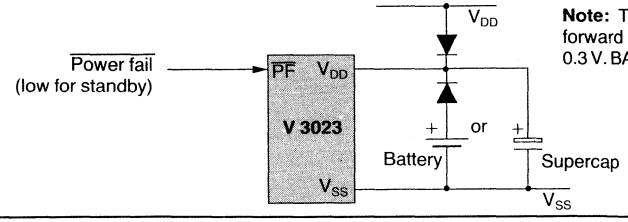
Test
From the various test features added to the V 3023 some may be activated by the user. Table 6 shows the test bits. Table 10 shows the three available modes and how they may be activated.
The first accelerates the incrementing of the parameters in the reserved clock and timer area by 32.
The second causes all clock and timer parameters, in the reserved clock and timer area, to be incremented in parallel at 100 Hz with no carry over, ie. independently of each other.
The third test mode combines the previous two resulting in parallel incrementing at 3.2 kHz.
While test bit 1 is set (addr. 00 hex, bit 7) the digital trimming action is disabled and no pulses are removed from the divider chain. Test bit 0 (addr. 00 hex, bit 6) can be combined with digital trimming (see section "Frequency Tuning").
To leave test, the test bits (addr. 00 hex, bits 6 and 7) must be cleared by software. Test corrupts the clock and timer parameters and so all parameters should be re-initialised after a test session.

Test Modes

Addr. 00hex bit 7	Addr. 00 hex bit 6	Function
0	0	Normal operation
0	1	Acceleration by 32
1	0	Parallel increment of all clock and timer parameters at 100 Hz with no carry over; dependent on the status of bit 3 at address 00 hex
1	1	Parallel increment of all clock and timer parameters at 3.2 kHz with no carry over; dependent on the status of bit 3 at address 00 hex

Table 10

Battery or Supercap Connection



Note: The diodes must have a forward voltage drop of less than 0.3 V. BAT 85 s are recommended.

Fig. 11

Typical Applications

V 3023 Interfaced with Intel CPU ($\overline{RD}$ and WR pulse)

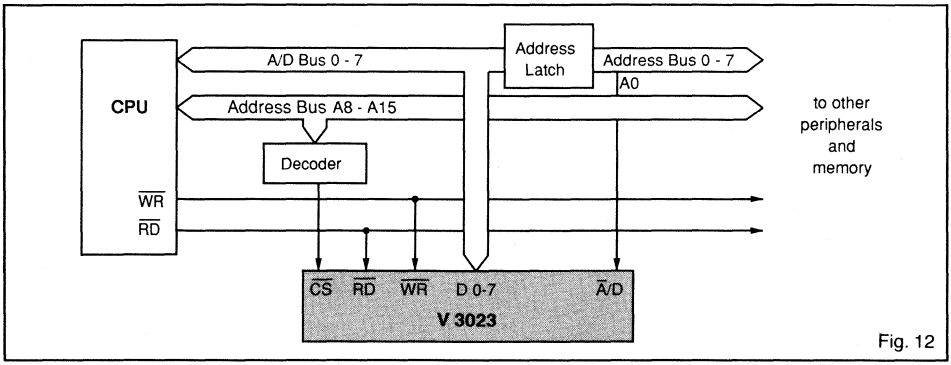


Fig. 12

V 3023 Interfaced with Motorola CPU ($\overline{DS}$ or $\overline{RD}$ pin tied to $\overline{CS}$, and R/$\overline{W}$)

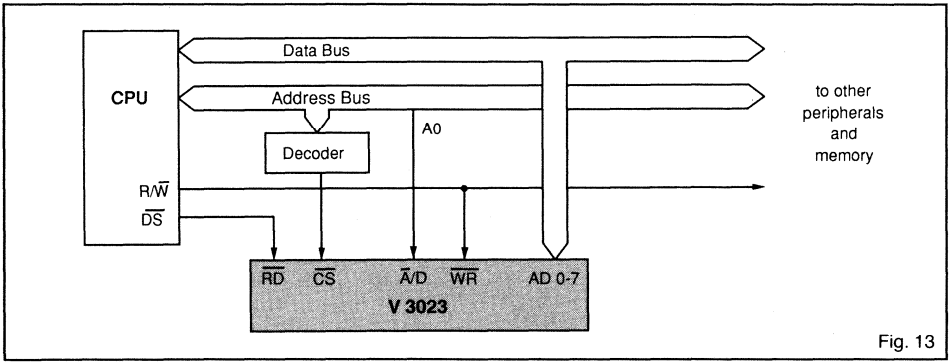


Fig. 13

Process Application

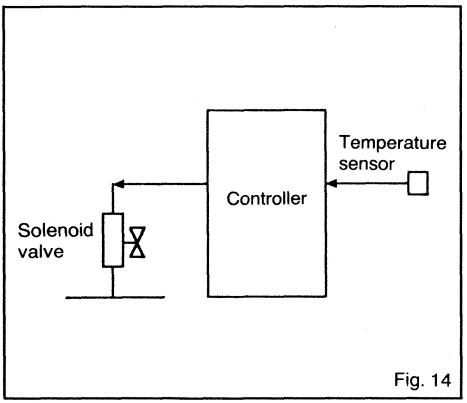
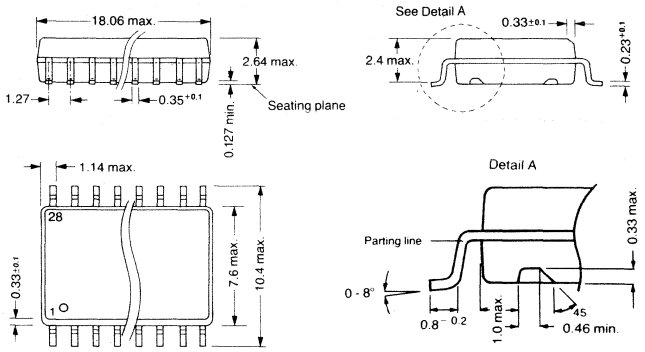


Fig. 14

- The formula in Fig. 5 is used by software to continually update the digital trimming register and so compensate the V 3023 for the ambient temperature.
- The timer is used to measure the duration the valve is on.
- The alarm feature is used to turn the controller power on and off at the time programmed by software. The V 3023 pulls $\overline{IRQ}$ active low on an alarm even in standby and thus can control the power on/off switch for the controller.
- The user RAM provides the controller with non volatile RAM for vital parameters. For example:
  1) the total on time for the valve to enable software to compute energy usage and also to identify when service is needed - 3 bytes
  2) average on time for the valve - 2 bytes
  3) maximum temperature ever encountered together with the time and date - 6 bytes
  4) date of last service and service man's ID - 4 bytes
  5) identification code for the controller - 1 byte

Package and Ordering Information

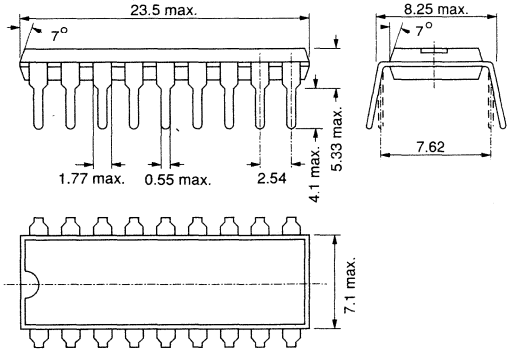
Dimensions of SO28 Package



Dimensions in mm

Fig. 15

Dimensions of DIP18 Package



Dimensions in mm

Fig. 16

Ordering Information

The V 3023 is available in the following packages:

DIP18 pin plastic package	V 3023 18P
SO28 pin plastic package	V 3023 28S

When ordering, please specify the complete part number and package.

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Table of Contents

CMOS Circuit for Analog Quartz Clocks with Bipolar Stepping Motor Drive

Features

- 32kHz quartz oscillator
- Integrated capacitors, mask selectable
- Single battery operation
- 0.8μA typical current consumption
- Low resistance outputs for bipolar stepping motor
- Mask options for pad designation, motor period and pulse width, alarm frequency, modulation and duty cycle
- Alarm output function compatible with either NPN or PNP-driver transistors
- Alarm input function
- 1024Hz output on AL_{IN} pad for oscillator frequency verification
- Fast test function
- ESD protected terminals
- Integrated capacitor for digital trimming

Description

The H 1063 is a low power 32kHz analog clock integrated in HCMOS technology to drive a bipolar stepping motor. Frequency trimming is carried out by selecting on chip oscillator input capacitances through pad bonding. Both the motor pulse period and the motor pulse width are mask-programmable. **See page 6 for already available options.**

Application

- Analog clocks

Functional Diagram

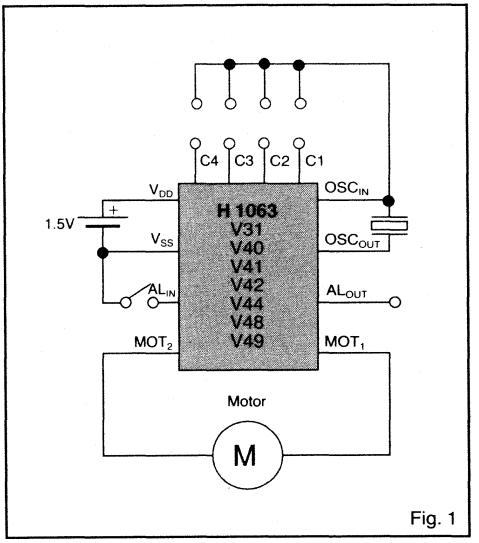


Fig. 1

Pin Assignment

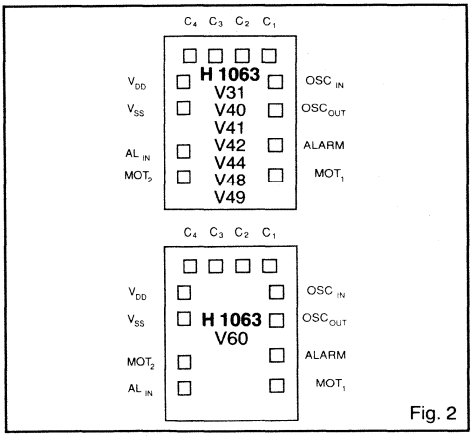


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage range	V_{DD} - V_{SS}	−0.3	+5	V
Input voltage	V_{IN}	V_{SS}	V_{DD}	V
Storage temperature	T_{STOR}	−55	+125	°C

Table 1

Stresses beyond these listed maximum ratings may cause permanent damage to the device. Exposure to conditions beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device contains circuitry to protect the terminals against damage due to high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Recommended Operating Conditions

Parameter	Symbol	Value	Units
Ambient temperature	T	25	°C
Quartz frequency	f_Q	32768	Hz
Quartz series resistance	R_Q	30	kΩ
Motor coil resistance	R_M	200	Ω
Positive supply	V_{DD}	1.5	V
Negative supply	V_{SS}	0	V

Table 2

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_{OPR}	−20		+70	°C
Quartz series resistance			30	50	kΩ

Table 3

Electrical and Switching Characteristics

at recommended operating conditions (valid unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}	Operating	+1.1		+1.8	V
Supply current	I_{DD}	Without motor, AL_{IN}, C1, C2, C3, C4 open		0.8	2.0	µA
Motor Output						
Current into load	I_M	V_{DD} = 1.2V, R_M = 200Ω	±4.3			mA
Pulse period	T_1			Mask option*		s
Pulse width	t_W			Mask option*		ms
Alarm Output						
Frequency	f_A			Mask option*		Hz
Modulation	f_{A1}			Mask option*		Hz
Cycle time	t_2			Mask option*		s
Pulse duration	t_P			Mask option*		s
Output current for	I_{ALOUTN}	V_{DD} = 1.2V, V_{OL} = 0.2V	0.5			µA
driving NPN-transistor	I_{ALOUTP}	V_{DD} = 1.2V, V_{OH} = 0.7V	0.3			mA
Output current for	I_{ALOUTN}	V_{DD} = 1.2V, V_{OL} = 0.5V	0.3			mA
driving PNP-transistor	I_{ALOUTP}	V_{DD} = 1.2V, V_{OH} = 1.0V	0.5			µA
Alarm Input						
Test In/Output						
Alarm input delay	t_{ALD}		125		570	ms
Test frequency	f_T			1024		Hz
Input current (alarm)	I_{IN}	Input at V_{SS}	−1	−8	−10	µA
Input current	I_{IN}	Input at V_{DD}	1	20	30	µA
Oscillator						
Build-up time	t_{START}	V_{DD} = 1.2V			2	s
Stability against supply	$\frac{\triangle f}{\triangle V_{DD} \cdot f}$	C_{IN} = C_{OUT} = 20pF				
voltage variations		1.1V ≤ V_{DD} ≤ 1.8V		7	10	ppm/V
Integrated capacitance	C_{OUT}			± (C_{OUT} · 0.1 + 0.5)		pF
	C_{IN}			± (C_{IN} · 0.1 + 0.5)		pF
Integrated capacitances	C1	Without external stray		3		pF
for bonding options	C2	capacitance		4		pF
	C3			5		pF
	C4			6		pF

* : See "Available options" on page 6.

Table 4

Timing Waveforms

Motor Output Waveform

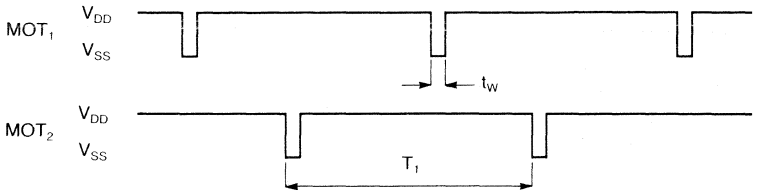


Fig. 3

Alarm Output Waveform

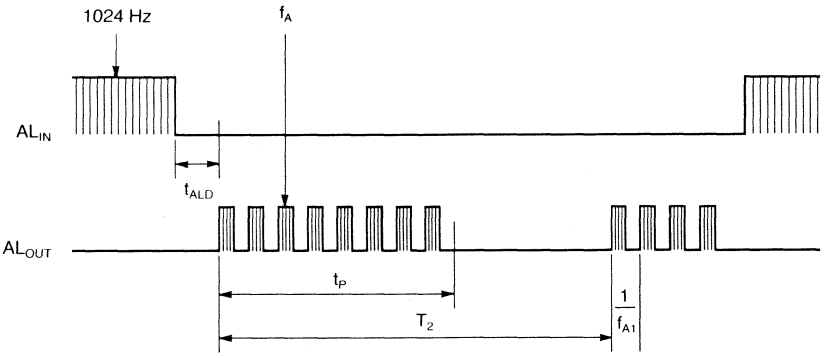


Fig. 4

Functional Description

Oscillator

The quartz oscillator consists of an inverter, internal feedback resistor to bias the input, series output resistance to improve stability and two fixed capacitors on OSC_{OUT} and OSC_{IN}. They are both variable by mask option. In addition to this there are also 4 pads selectable capacitors at OSC_{IN}. Frequency trimming is achieved by selecting one or more of the 4 capacitors which allows the input capacitance to be increased by 3 pF to 18 PF in 1 pF steps.

Motor Drive Output

The circuit contains two push-pull output buffers for driving bipolar stepping motors. Between two pulses, both P-channel transistors conduct. During an output pulse, the N-channel transistor of one buffer and the P-channel transistor of the other buffer are conducting. The outputs are protected against inductive voltage spikes with diodes to both supply pins.
Both the motor pulse period and motor pulse width are programmable by metal mask over a wide range of values (see page 6 for available options).

Alarm Output

The alarm is activated by connecting AL_{IN} to V_{SS} and is deactivated by opening the connection. A metal mask option is available to program a continuous activation of the alarm output.
The alarm output driver contains a push-pull output buffer to drive an external sound source by means of an external bipolar transistor. A metal mask option is available to allow the use of NPN or PNP-transistors.
The tone frequency, modulation frequency and cycle time (ON/OFF time) are metal mask selectable.

Test Mode

The AL_{IN} pin fulfills three functions:

a) For normal operation, the AL_{IN} pin is left open. The circuit provides a square wave signal of 1024Hz which can be used to tune the oscillator.
b) If the pin is connected to V_{SS}, the alarm signal is provided at pin AL_{OUT}.
c) If the AL_{IN} pin is connected to V_{DD}, all output frequencies are increased by a factor of 64, the alarm modulations of f_{A1} = 8Hz and f_A = 2kHz are suppressed.

Test configuration

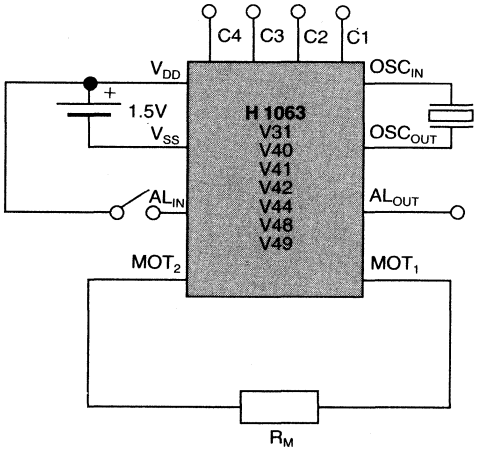
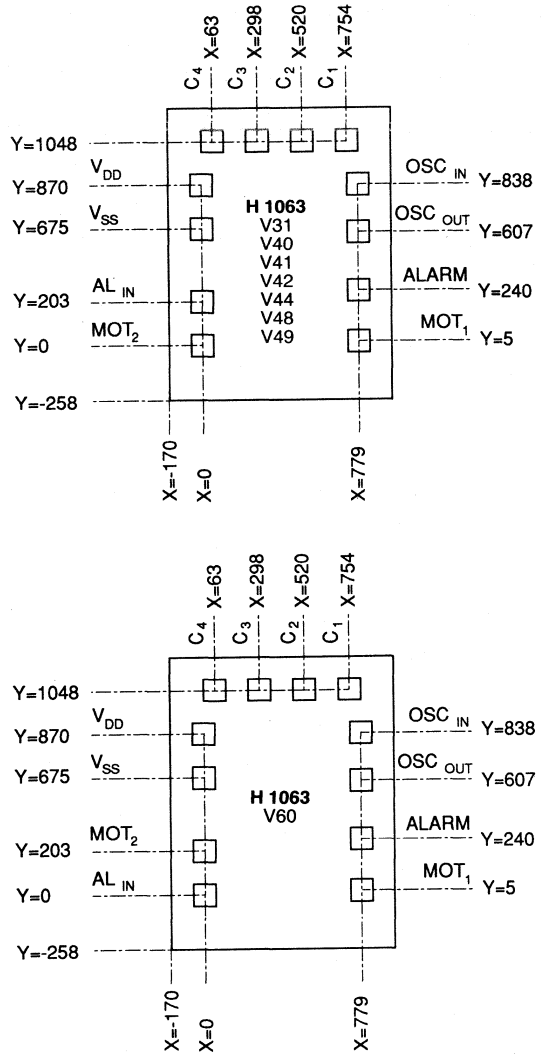


Fig. 5

Pad Location Diagram

All dimensions in μm



Chip size is X = 1117 by Y = 1523 microns or X = 44 by Y = 60 mils
Note: The origin (0,0) is the lower left coordinate of center pads.
The lower left corner of the chip shows distances to origin.

Fig. 6

Available Options

Option	Motor		Alarm Output				Integrated Capacitance		Alarm Output Transistor
	Period (T_1)	Pulse width (t_W)	Frequency (f_A)	Modulation (f_{A1})	Cycle Time (T_2)	Pulse Duration (t_P)	Fix (C_{IN})	Fix (C_{OUT})	
V31	2 s	31.24 ms	2048 Hz	8 Hz	1 s	0.5 s	8 pF	20 pF	NPN
V40	2 s	46.8 ms	2048 Hz	8 Hz	4 s	1 s	8 pF	20 pF	NPN
V41	2 s	31.24 ms	2048 Hz	8 Hz	4 s	1 s	8 pF	20 pF	NPN
V42	2 s	15.6 ms	2048 Hz	8 Hz	4 s	1 s	8 pF	20 pF	NPN
V44	2 s	23.4 ms	2048 Hz	8 Hz	4 s	1 s	8 pF	20 pF	NPN
V48	2 s	46.8 ms	2048 Hz	8 Hz	1 s	0.5 s	8 pF	20 pF	NPN
V49	2 s	31.24 ms	2048 Hz	8 Hz	1 s	0.5 s	8 pF	20 pF	PNP
V60	2 s	46.8 ms	2048 Hz	8 Hz	4 s	1 s	8 pF	20 pF	NPN

Table 5

© 1994 EM Microelectronic-Marin SA, 09/94, Rev. B/073

CMOS Circuit for Analog Quartz Watches

atures

:2kHz quartz oscillator
)perating voltage range −1.2V to −1.8V
ligh oscillator stability
ntegrated capacitors, mask selectable
Mask options for pad designation, motor period and notor pulse width
horted motor coil between motor pulses
ast motor test function
SD protected terminals
12Hz output on TEST pad for quartz frequency neasurement
ully debounced TEST input and RESET input

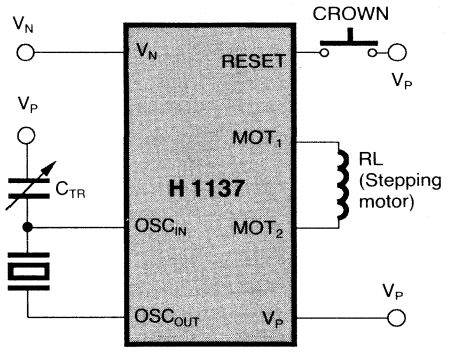
scription

H 1137 is a low power 32kHz analog watch chip design- o drive a stepping motor. Motor pulse width is program- ble from 0.9765 to 14.65 milliseconds in steps of 0.9765 seconds. Motor pulse period is programmable from 2 x 2 x 60 seconds in steps of 1 second. Motor pulse period so programmable from 2 x 0,25 to 2 x 15,75 seconds in s of 0,25 seconds. Input and output capacitors are inte- ed on the chip. Their values are metal mask selectable. selection of width, period and capacitance are metal ons and do not require additional bonds.

plication

nalog watches

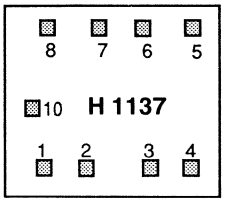
Functional Diagram



Operating range of trimmer
Capacitance: 3pF ≤ C_{TR} ≤ 30 pF

Fig. 1

Pin Assignment



Pad	Function	Pad Locations
V_N	Negative supply voltage	1
V_P	Positive supply voltage	5
OSC_{IN}	Oscillator input	3
OSC_{OUT}	Oscillator output	4
MOT_1	Motor drive output 1	7
MOT_2	Motor drive output 2	6
RESET	Reset input	2 or 8
TEST	Test input / output	2 or 8 or 10

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage	V_N	−3.6		+0.2	V
Voltage applied to other terminals		V_N−0.3		V_P+0.3	V
Storage temperature	T_{STOR}	−55		+125	°C

Stresses beyond these listed maximum ratings may cause permanent damage to the device. Exposure to conditions beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device contains circuitry to protect the terminals against damage due to high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Recommended Operating Conditions

Parameter	Symbol	Value	Units
Ambient temperature	T	25	°C
Quartz frequency	f_Q	32768	Hz
Quartz series resistance	R_Q	30	kΩ
Motor coil resistance	R_M	2.0	kΩ
Positive supply	V_P	0	V
Negative supply	V_N	−1.55	V
Supply source resistance	R_I	10	Ω

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_{OPR}	−10		+60	°C
Quartz series resistance			30	50	kΩ
Trimmer capacitance	C_{TR}	3		30	pF

Electrical and Switching Characteristics

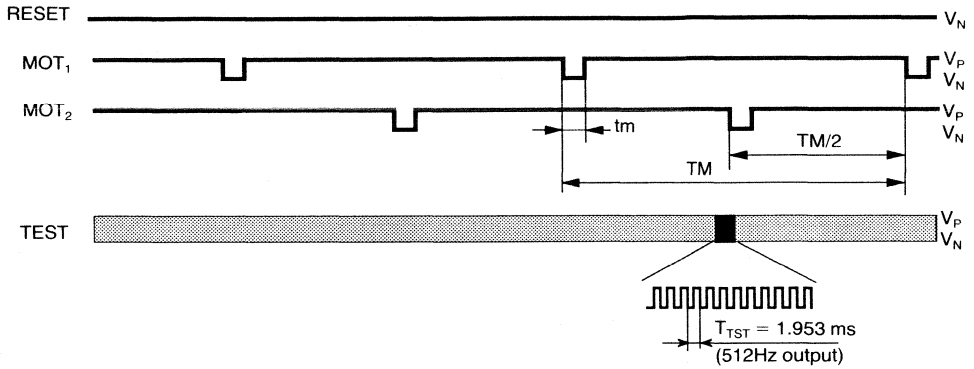
at recommended operating conditions unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply voltage range	V_N		−1.8	−1.55	−1.2	V
Mean dynamic current	I_{DYN}	without motor and quartz, 32kHz and 32kHz inverted square wave forced at OSC_{IN} and OSC_{OUT}, TEST open		90	150	nA
Mean current consumption	I_N	with quartz, without motor, TEST open, C_{TR} = 12pF		200	350	nA
Oscillator						
Transconductance	gm	V_N = −1.2V, V_{PP} = 300mV	2.5			µmho
Starting voltage	V_{ST}	Within 10 seconds		0.75		V
Starting time	T_{ST}	Recommended operating conditions			2	s
Stability df / f* dV_N		Between −1.4V and −1.6V		1.5		ppm/V
Motor Drivers						
Voltage across motor	V_{MOT}	V_N = −1.55V, R_M = 2kΩ	1.35	1.40		V
Voltage across motor	V_{MOT}	V_N = −1.25V, R_M = 2kΩ	1.0	1.10		V
Voltage across motor	V_{MOT}	R_I = 300Ω, T_{OPR}	1.0	1.20		V
Short circuit impedance	R_{CC}	Between motor pulses		150	300	Ω
Test Input / Output						
Amplitude	V_{TST}	ZI = 30pF // 1MΩ	1.35			V_{PP}
Mean current	I_{TST}	Pad connected to V_P		70	250	nA
Reset Input						
Debounce delay	T_S		7.81		23.43	ms
Input current after debounce delay*	I_S	Pad connected to V_P		7	50	nA

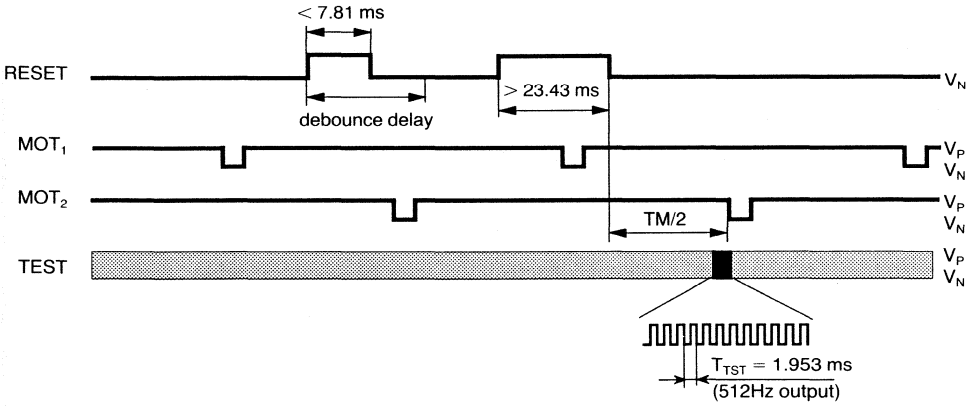
* Is the average input current, modulated by a frequency of 64Hz

ming Waveforms

Motor drive output in normal operation



Motor drive output and reset



Fast motor test mode, TEST = V_P

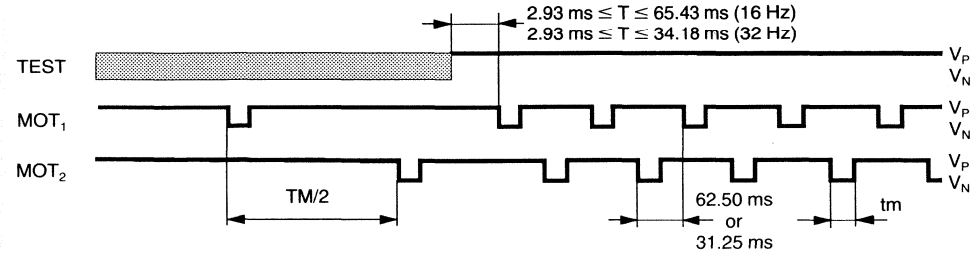


Fig. 3

Block Diagram

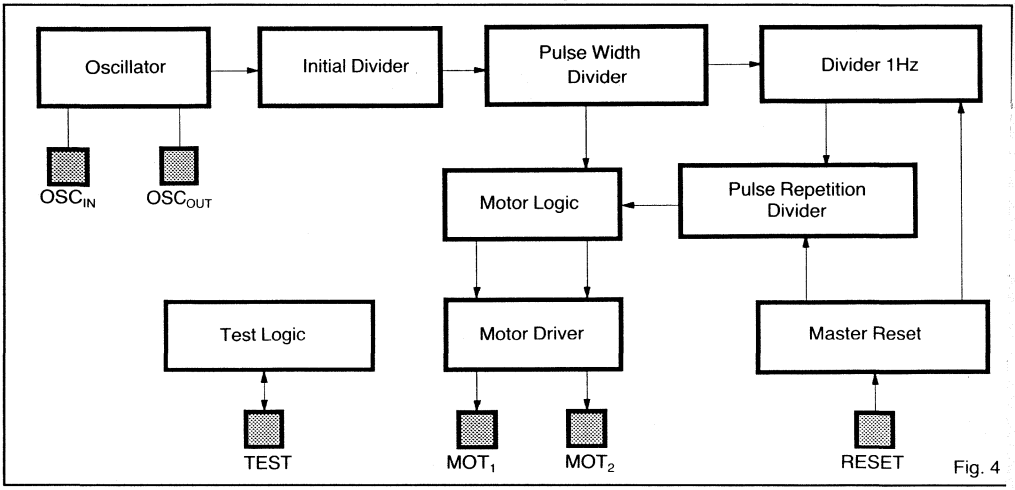


Fig. 4

Pin Assignments

Name	Function
V_N	Negative supply voltage
V_P	Positive supply voltage
OSC_{IN}	Oscillator input
OSC_{OUT}	Oscillator output
MOT_1	Motor drive output 1
MOT_2	Motor drive output 2
RESET	Reset input
TEST	Test input / output

Functional Description

Oscillator

The 32'768Hz clock frequency is generated by a crystal oscillator. Input and output capacitors are integrated in the chip. Their values are metal mask selectable.

Motor drive output

The H 1137 contains two push-pull output buffers for driving bipolar stepping motors (see Fig. 3). Between two pulses, the two p-channel devices are active for motor damping.

Reset

Pulling the RESET input to V_P resets the frequency dividers and disables the motor pulses. Motor pulses in progress when the RESET function is applied, will be completed. After releasing the RESET pad from V_P, the next motor pulse appears with a delay of one half motor cycle on the drive output MOT_1 if the last motor pulse appeared on MOT_2 or vice-versa (see Fig. 3). Due to the debounce circuitry on the RESET input, V_P must be applied for at least 23.4 ms to be accepted as RESET.

Test mode

The TEST pad fulfils two functions:

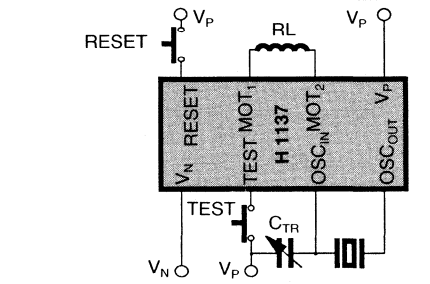
a) For normal operation, the TEST pad is left open. The circuit outputs a square wave signal of 512Hz which can be used for tuning the oscillator.

b) If the TEST pad is connected to V_P, the period for the motor pulses changes to either 2 x 31.25 ms or 2 x 62.5 ms (mask options), while the motor pulse width remains unchanged (fast motor test).

Test

Test Pad	Function	Description
Connected to V_P	Fast motor test	Increase the frequency for the motor pulses to 16Hz (32Hz)
Open	Normal operation	Output of square wave signal (512Hz)

Test configuration



Operating range of trimmer capacitance:
$3pF \leq C_{TR} \leq 30pF$

Fig. 5

etal Mask Option Possibilities

tor pulse and capacitance

m- l	Description	Range min.	Range max.	Range resolut.
1	Motor pulse period	2x1.00s	2x60.00s	1.00s
1	Fast motor TEST	2x31.25ms	2x62.50ms	
	Motor pulse width	0.9765ms	14.65ms	0.9765ms
↓	Oscillator input capacity	2pF	$C_{IN} + C_{OUT}$	1pF
UT	Oscillator output capac.	2.7pF	= 35pF	1pF

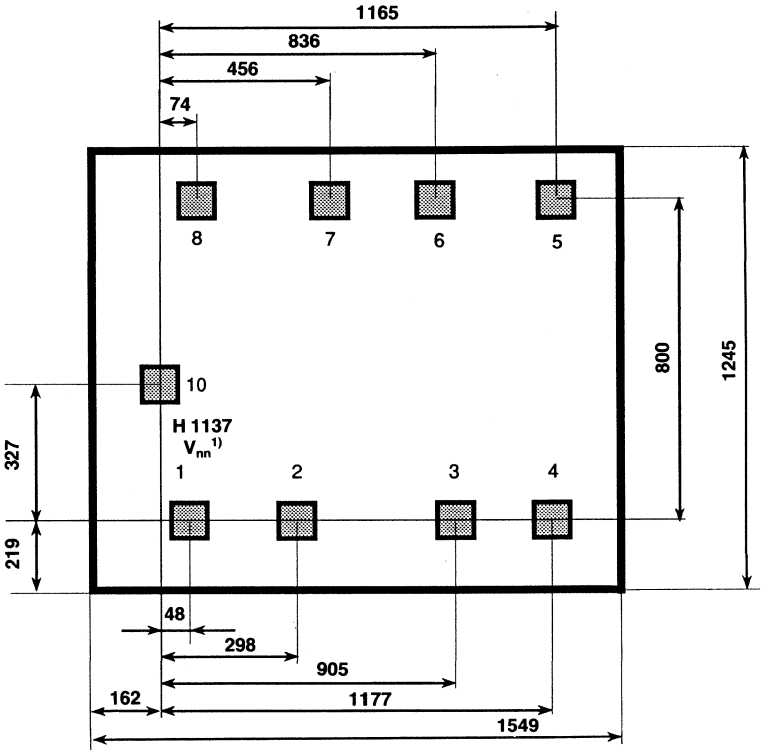
Pad options

Sym- bol	Description	Pad Layout 1	Pad Layout 2	Pad Layout 3
TEST	Pad TEST	Pad 10	Pad 2	Pad 8
RESET	Pad RESET	Pad 8	Pad 8	Pad 2
		Pad 2	Pad 10	Pad 10
		not used	not used	not used

ssible versions Option list (supply voltage – 1.55V)

ersions	Options														Compatible
	Motor output			Integrated capacitor		Designation pad									
	Periods	Pulse width ms	Fast mode ms	OSC_{IN} pF	OSC_{OUT} pF	Pad 1	Pad 2	Pad 3	Pad 4	Pad 5	Pad 6	Pad 7	Pad 8	Pad 10	EUROSIL E1208
1137 V01	2x12	6.8	2x62.5	2	18	V_N	-	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	TEST	A
1137 V02	2x1	3.9	2x62.5	2	14	V_n	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	B
1137 V03	2x10	7.8	2x62.5	2	22	V_N	RESET	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	TEST	-	C
1137 V04	2x12	5.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	D
1137 V05	2x1	6.8	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	E
1137 V07	2x10	5.9	2x62.5	2	16	V_N	RESET	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	TEST	-	G
1137 V08	2x12	6.8	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	H
1137 V09	2x1	7.8	2x62.5	2	20	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	IS
1137 V10	2x1	3.9	2x62.5	2	14	V_N	-	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	TEST	K
1137 V11	2x12	5.9	2x62.5	2	14	V_N	-	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	TEST	L
1137 V12	2x1	6.8	2x62.5	2	14	V_N	-	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	TEST	M
1137 V13	2x12	6.8	2x62.5	2	14	V_N	-	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	TEST	N
1137 V14	2x1	4.9	2x62.5	2	16	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	O
1137 V15	2x1	6.8	2x62.5	2	20	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	P
1137 V16	2x1	5.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	S
1137 V17	2x5	5.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	T
1137 V19	2x20	7.8	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	V
1137 V20	2x20	5.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WA
1137 V21	2x1	4.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WB
1137 V22	2x1	3.9	2x62.5	2	20	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WD
1137 V23	2x1	5.9	2x62.5	2	20	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WE
1137 V24	2x10	6.8	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WF
1137 V25	2x5	7.8	2x62.5	2	20	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WG
1137 V26	2x20	6.8	2x31.25	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	WH
1137 V27	2x0.5	4.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	
1137 V28	2x40	5.9	2x62.5	2	14	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	
1137 V51	2x5	4.9	2x31.25	2	23	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	
1137 V52	2x5	7.8	2x31.25	2	23	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	
1137 V53	2x1	3.9	2x31.25	2	23	V_N	TEST	OSC_{IN}	PSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	
1137 V54	2x20	4.9	2x31.25	2	23	V_N	TEST	OSC_{IN}	OSC_{OUT}	V_P	MOT_2	MOT_1	RESET	-	

Chip Information



All dimensions in microns

Fig. 6

1) nn stands for the version

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CMOS Circuit for Analog Quartz Clocks with Bipolar Stepping Motor Drive

Features

- 32kHz quartz oscillator
- Integrated capacitors, mask selectable
- Single battery operation
- 0.7μA typical current consumption
- Low resistance outputs for bipolar stepping motor
- Mask options for pad designation, motor period and pulse width, alarm frequency, modulation and duty cycle
- Alarm output function compatible with either NPN or PNP-driver transistors
- Alarm input function
- 1024Hz output on AL_{IN} pad for oscillator frequency verification
- Fast test function
- ESD protected terminals

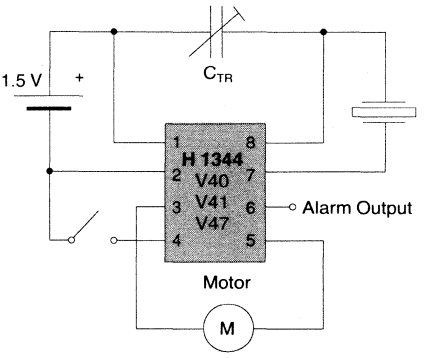
Description

The H 1344 is a low power 32kHz analog clock integrated circuit designed in HCMOS technology to drive a bipolar stepping motor. A set of capacitors is provided on chip to be connected, in any combination, to the two oscillator terminals, with a maximum total capacitance of 48pF. Both the motor pulse period and the motor pulse width are mask-programmable. **See page 6 for already available options.**

Application

- Analog clocks

Functional Diagram



Operating range of trimmer
Capacitance: 1.5pF $\leq C_{TR} \leq$ 30 pF

Fig. 1

Pin Assignment

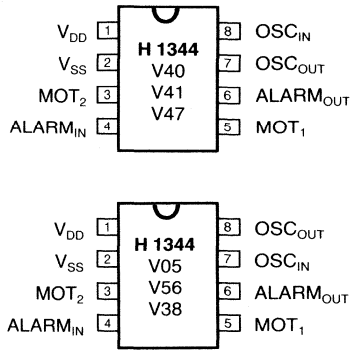


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage range	V_{DD} - V_{SS}	−0.3	+5	V
Input voltage	V_{IN}	V_{SS}	V_{DD}	V
Storage temperature	T_{STOR}	−55	+125	°C

Table 1

Stresses beyond these listed maximum ratings may cause permanent damage to the device. Exposure to conditions beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device contains circuitry to protect the terminals against damage due to high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Recommended Operating Conditions

Parameter	Symbol	Value	Units
Ambient temperature	T	25	°C
Quartz frequency	f_Q	32768	Hz
Quartz series resistance	R_Q	30	kΩ
Motor coil resistance	R_M	200	Ω
Positive supply	V_{DD}	1.55	V
Negative supply	V_{SS}	0	V

Table 2

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_{OPR}	−20		+70	°C
Quartz series resistance			30	50	kΩ
Trimmer capacitance	C_{TR}	1.5		30	pF

Table 3

Electrical and Switching Characteristics

at recommended operating conditions (valid unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}	operating	+1.1		+1.8	V
Supply current	I_{DD}	without motor, AL_{IN} open		0.7	2.0	μA
Motor Output						
Current into load	I_M	V_{DD} = 1.2V, R_M = 200Ω	±4.0			mA
Pulse period	T_1			Mask option*		s
Pulse width	t_W			Mask option*		ms
Alarm Output						
Frequency	f_A			Mask option*		Hz
Modulation	f_{A1}			Mask option*		Hz
Cycle time	t_2			Mask option*		s
Pulse duration	t_P			Mask option*		s
Output current for	I_{ALOUTN}	V_{DD} = 1.2V, V_{OL} = 0.2V	0.5			μA
driving NPN-transistor	I_{ALOUTP}	V_{DD} = 1.2V, V_{OH} = 0.7V	0.3			mA
Output current for	I_{ALOUTN}	V_{DD} = 1.2V, V_{OL} = 0.5V	0.3			mA
driving PNP-transistor	I_{ALOUTP}	V_{DD} = 1.2V, V_{OH} = 1.0V	0.5			μA
Alarm Input Test In/Output						
Alarm input delay	t_{ALD}		125		570	ms
Test frequency	f_T			1024		Hz
Input current (alarm)	I_{IN}	Input at V_{SS}, V_{DD} = 1.4V	−1	−5	−10	μA
Input current	I_{IN}	Input at V_{DD}	1	15	30	μA
Oscillator						
Build-up time	t_{START}	V_{DD} = 1.2V			2	s
Stability against supply voltage variations	$\frac{\triangle f}{\triangle V_{DD} \times f}$	1.1V ≤ V_{DD} ≤ 1.8V		5	12	ppm/V
Output capacitance	C_{OUT}			Mask option*		pF
Input capacitance	C_{IN}			Mask option*		pF

* : See "Available options" on page 6.

Table 4

Timing Waveforms

Motor Output Waveform

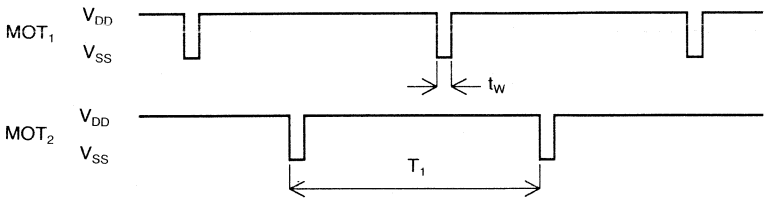


Fig. 3

Alarm Output Waveform

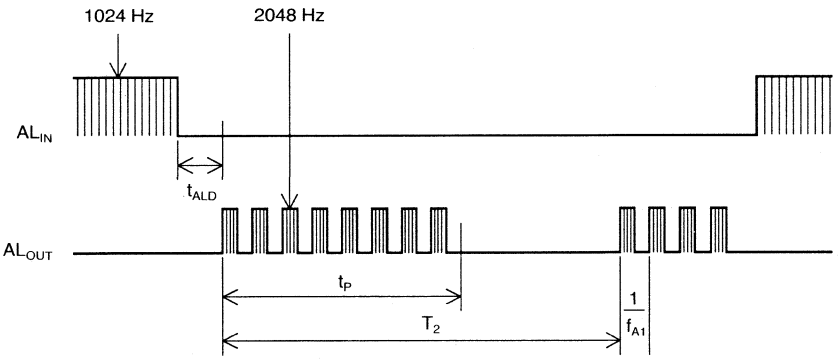


Fig. 4

Functional Description

Oscillator and Frequency Divider

The quartz oscillator consists of an inverter, internal feedback resistor to bias the input, series output resistance to improve stability and integrated capacitors. The values of the integrated capacitors are selectable by metal mask. The oscillator is designed for 32768Hz.

Motor Drive Output

The circuit contains two push-pull output buffers for driving bipolar stepping motors. Between two pulses, both P-channel transistors conduct. During an output pulse, the N-channel transistor of one buffer and the P-channel transistor of the other buffer are conducting. The outputs are protected against inductive voltage spikes with diodes to both supply pins.
Both the motor pulse period and motor pulse width are programmable by metal mask over a wide range of values (see page 6 for available options).

Alarm Output

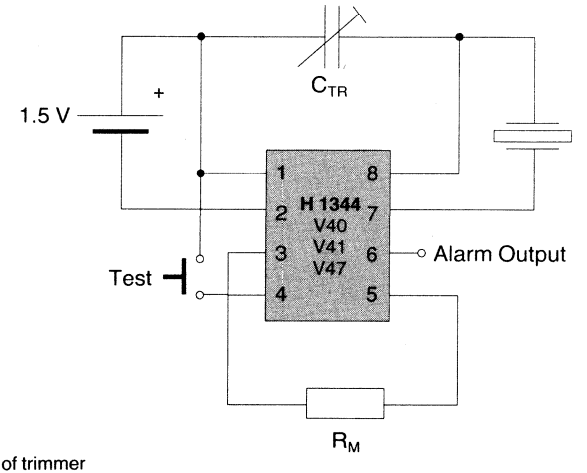
The alarm is activated by connecting $ALARM_{IN}$ to V_{SS} and is deactivated by opening the connection. A metal mask option is available to program a continuous activation of the alarm output.
The alarm output driver contains a push-pull output buffer to drive an external sound source by means of an external bipolar transistor. A metal mask option is available to allow the use of NPN or PNP-transistors.
The tone frequency, modulation frequency and cycle time (ON/OFF time) are metal mask selectable.

Test Mode

The $ALARM_{IN}$ pin fulfills three functions:

a) For normal operation, the $ALARM_{IN}$ pin is left open. The circuit provides a square wave signal of 1024Hz, which can be used to tune the oscillator.
b) If the pin is connected to V_{SS}, the alarm signal is provided at pin 6.
c) If the $ALARM_{IN}$ pin is connected to V_{DD}, all output frequencies are increased by a factor of 64, the alarm modulations of f_{A1} = 8Hz and f_A = 2kHz are suppressed.

Test configuration

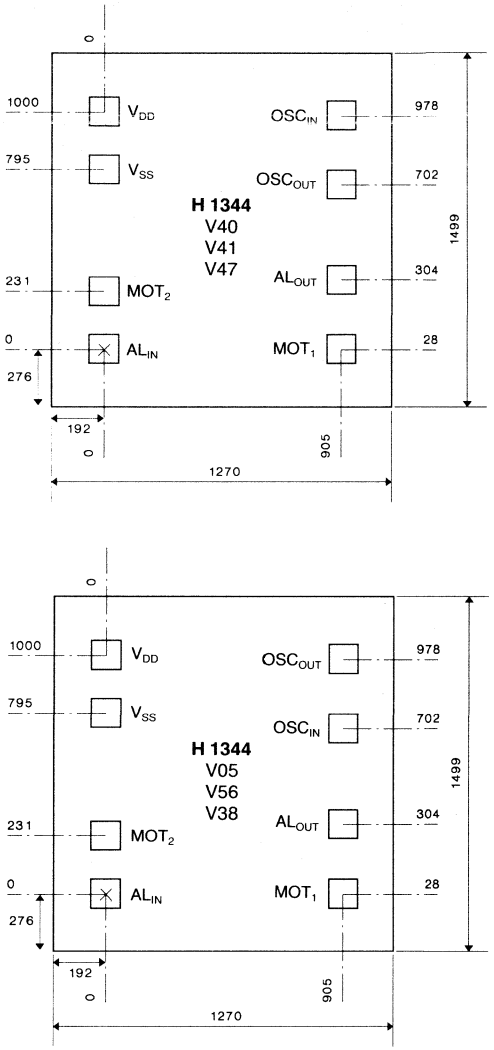


Operating range of trimmer
Capacitance: 1.5 pF ≤ C_{TR} ≤ 30 pF

Fig. 5

Pad Location Diagram

All dimensions in μm



Chip size: 1270 x 1499 microns
50 x 59 mils

Fig. 6

Available Options

Option	Motor		Alarm Output				Integrated Capacitance		Alarm Output Transistor
	Period (T_1)	Pulse width (t_W)	Frequency (f_A)	Modulation (f_{A1})	Cycle Time (T_2)	Pulse Duration (t_P)	(C_{IN})	(C_{OUT})	
V05*	2s	46.8ms	2048Hz	8Hz	4s	1s	16pF	23pF	NPN
V38	2s	46.8ms	2048Hz	8Hz	4s	1s	3pF	28pF	NPN
V40	2s	46.8ms	2048Hz	8Hz	4s	1s	3pF	20pF	NPN
V41	2s	23.4ms	2048Hz	8Hz	4s	1s	3pF	20pF	NPN
V47	2s	31.24ms	2048Hz	8Hz	1s	0.5s	3pF	20pF	NPN
V56*	2s	46.8ms	2048Hz	8Hz	4s	1s	19pF	23pF	NPN

* : Without external trimmer (quartz classes to be matched).

Table 5

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CMOS Car Clock Circuit

Features

- 4.19 MHz quartz oscillator
- Frequency is programmable via a 5 bit E^2PROM (no trimming capacitor required)
- LCD drive voltage adjustable via 5 bit E^2PROM for best contrast and largest viewing angle
- Temperature compensated LCD drive voltage for best contrast and largest viewing angle
- 12 hour or 24 hour display mode selectable via MODE input
- Colon flash option selectable via FLASH input
- Operating ambient temperature range: −40 to +85°C
- 28 lead mini package (SO28)
- Auto-increment mask programmable to 1 Hz, 2 Hz or 4 Hz
- DATA and V_{PP} are normal logical inputs
- Excellent immunity from electromagnetic radiation

Description

The H 5050 is a 4.19 MHz CMOS car clock circuit providing hours and minutes display. It is designed to drive a 3¾ digit, 2:1 multiplexed 7 segment clock display with AM and PM functions (e.g. Philips LTD133 liquid crystal display).
Time setting functions are accomplished via 2 inputs S1 and S2. Oscillator frequency and LCD drive voltage are programmable via on-chip E^2PROM.

Applications

- Car clocks

Typical Operating Configuration

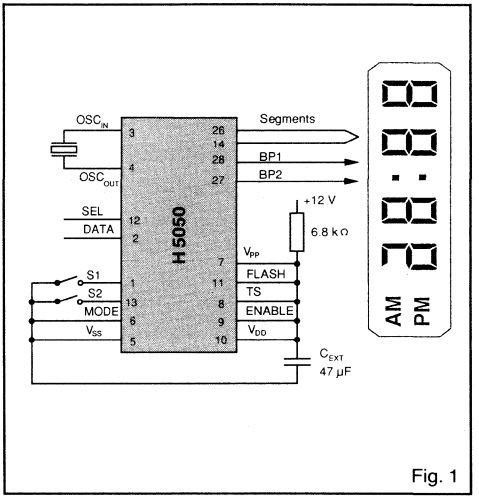


Fig. 1

Pin Assignment

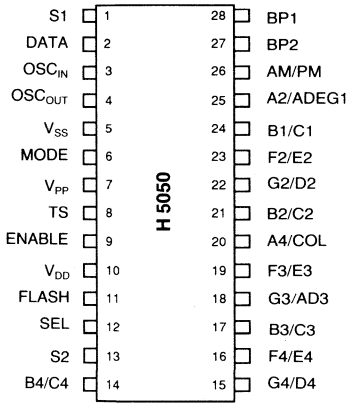


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}	with relation to V_{SS}	-		8	V
Supply current	I_{DD}		-		3	mA
Voltage applied to input pins	V_I	with relation to V_{SS}	−0.3		V_{DD}+0.3	V
Storage temperature	T_{STO}		−65		+150	°C
Operating temperature range	T_A		−40		+85	°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Electrical Characteristics

V_{DD} = 3 ÷ 6 V, T_A = −40 to +85°C, quartz: frequency = 4.194304 MHz, max. frequency tolerance = ± 30*10^{-6}, R_S = 50 Ω, C_L = 12 pF, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply						
Supply voltage	V_{DD}	Programmable	3	-	6	V
Supply voltage variation	$\triangle V_{DD}$	S1 or S2 closed	-	-	50	mV
Supply voltage variation due to temperature	TC	V_{DD} = 4.5 V	-	−0.35	-	%/°K
			-	−16	-	mV/°K
Supply current	I_{DD}	Note [1]	500		2000	µA
Capacitance	C_{EXT}	External capacitor	22	47	-	µF
Oscillator						
Start time	t_{OSC}		-	-	200	ms
Frequency stability	$\triangle f/f \cdot \triangle V_{DD}$	$\triangle V_{DD}$ = 100 mV	-	-	1	ppm/V
Input capacitance	C_I		-	16	-	pF
Output capacitance	C_O			16		pF
Feedback resistance	R_{fb}		300	1000	3000	kΩ
Inputs						
Pull-up resistance	R_{Pu}	S1, S2, TS, SEL, DATA and V_{PP}	45	90	180	kΩ
Pull-up/down resistance	$R_{Pu/d}$	MODE	100	300	1000	kΩ
Debounce time	t_{Deb}	S1 and S2 only	78	-	110	ms
Backplane						
Output resistance	R_{BP}	High/low level ± 100 µA	-	-	3	kΩ
Segments						
Output resistance	R_{SEG}	± 100 µA	-	-	5	kΩ
DC offset voltage	V_{dc}	200 kΩ/1 nF	-	-	50	mV

Table 2

[1] A suitable external resistor R must be selected:
Example: V_{DD} = 5 V, R_{min} = (12 V − 5 V) / 2000 µA = 3.5 kΩ

Pin Description

Pin	Name	Function
1	S1	Hour adjustment input
2	DATA	E^2PROM data input
3	OSC_{IN}	Oscillator input
4	OSC_{OUT}	Oscillator output
5	V_{SS}	Negative supply voltage
6	MODE	12/24 hour mode select input
7	V_{PP}	Programming input
8	TS	Test speed-up mode input
9	ENABLE	Enable input for S1 and S2
10	V_{DD}	Positive supply voltage
11	FLASH	Colon option input
12	SEL	E^2PROM select input
13	S2	Minute adjustment input
14	B4/C4	Segment driver
15	G4/D4	Segment driver
16	F4/E4	Segment driver
17	B3/C3	Segment driver
18	G3/AD3	Segment driver
19	F3/E3	Segment driver
20	A4/COL	Segment driver
21	B2/C2	Segment driver
22	G2/D2	Segment driver
23	F2/E2	Segment driver
24	B1/C1	Segment driver
25	A2/ADEG1	Segment driver
26	AM/PM	Segment driver
27	BP2	Backplane 2
28	BP1	Backplane 1

Table 3

Segment designation of LCD display

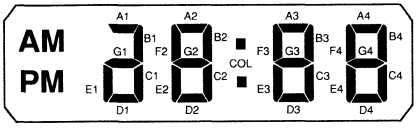


Fig.3

Functional Description

Outputs

The circuit presents LCD data at pins 14 to 26. Two way (1:2) multiplex driving is used in order to save circuit pins. The backplane signals appear at pin 27 and 28 respectively. In Fig. 3 the corresponding waveforms are shown.

Backplane and Segment Waveforms

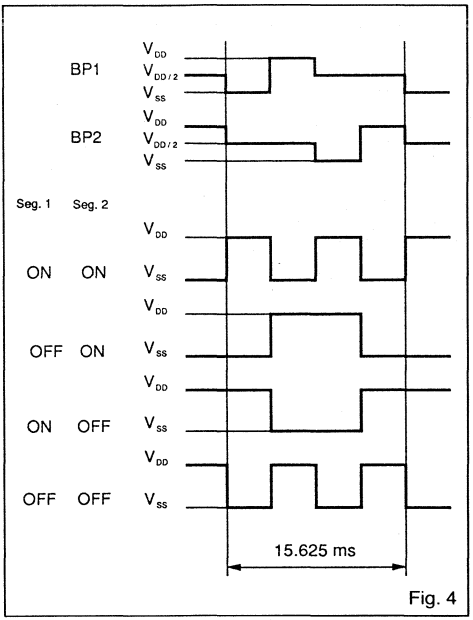


Fig. 4

The average voltages across the segments have the following values:

$V_{ON(ms)} = 0.79\ V_{DD}$

$V_{OFF(ms)} = 0.35\ V_{DD}$

LCD Driving Voltage

The on-chip shunt regulator controls the value of supply voltage according to ambient temperature and the content of the 5 bit voltage E^2PROM. This guarantees best contrast and largest viewing angle for the whole temperature range (see section "LCD Voltage Programming").

12/24 Hour Mode

Operation of 12 hour or 24 hour mode is selected via MODE input. If MODE input is floating and a reset occurs (see section "Segment Test and Reset"), the mode will change from 12 hour to 24 hour or vice versa.

Power-Up

After power-up the actual mode and LCD display is set according to connection of the mode input:

1 : 00 AM 12 hour mode when MODE input is connected to V_{DD}

1 : 00 24 hour mode when MODE input is floating or connected to V_{SS}.

Colon
If FLASH input is held at V_{DD} colon will flash at 1 Hz (duty cycle 50%). Connecting FLASH to V_{SS} displays a stable colon.

Time Setting
Time setting is accomplished via the two inputs S1 and S2. These two inputs are pulled to V_{DD} via on-chip resistors of about 90 kΩ. This in conjunction with debouncer circuitry (debouncing time 78 ÷ 110 ms), allows the use of simple single-throw switches.

Set Enable
Connecting ENABLE to V_{DD} enables inputs S1 and S2, connecting ENABLE to V_{SS} makes S1 and S2 inactive.

Hours Setting
When S1 is pulled to V_{SS} the hours counter is incremented by 1 immediately (after debounce time). If S1 is held at V_{SS}, after a pause of 1 ÷ 1.25 s, the hours counter is auto-incremented at a rate of 1, 2 or 4 Hz (depending on metal mask version) until S1 is released again. In hours setting mode the carry from minutes counter is not propagated.

Minutes Setting
When S2 is pulled to V_{SS} the minutes counter is incremented by 1 immediately (after debounce time). If S2 is held at V_{SS}, after a pause of 1 ÷ 1.25 s, the minutes counter is auto-incremented at a rate of 1, 2 or 4 Hz (depending on metal version) until S2 is released again. In minutes setting mode the carry is not propagated to the hours counter. In addition to minutes setting, the seconds counter is reset to zero.

Segment Test and Reset
If S1 and S2 are pulled to V_{SS} together, all LCD segments are turned ON. Releasing both switches resets the clock and the display is set according to MODE input:

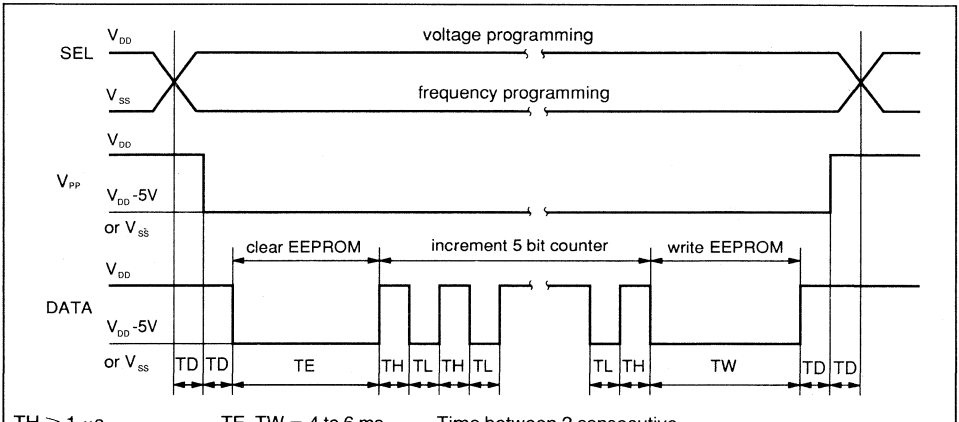
1 : 00 AM if MODE input is connected to V_{DD}
0 : 00 if MODE input is connected to V_{SS}

Display mode changes if MODE input is floating.
If DATA input is hold low during segment test, no reset occurs.

Test Mode
In normal operating mode TS input must be connected to V_{DD}. Connecting TS to V_{SS} allows quick testing of the display via the inputs S1 and S2. Debounce time and auto-increment rate are 64 times faster than normally. Additionally the carry to the seconds counter is inhibited. TS has an internal pull-up resistor, however for safety reasons it should be connected to V_{DD}.

E^2PROM Programming
The inputs DATA, SEL and V_{PP} are used to program the voltage and frequency E^2PROMs. SEL input is used to select between voltage E^2PROM (SEL high or floating) and frequency E^2PROM (SEL low). When pulled to V_{SS} or −5 V in reference to V_{DD}, V_{PP} enables E^2PROM programming sequence. DATA input serves for two purposes: any negative pulse (V_{SS} or −5 V in reference to V_{DD}) increments a 5 bit programming counter by 1 (on the positive edge), if the pulse width is between 4 to 6 ms the selected E^2PROM is erased (first long pulse after V_{PP} has gone low) or programmed with the content of the programming counter (second long pulse after V_{PP} has gone low). If the programming counter has reached its maximum value and an additional pulse is applied, the programming counter is reset to 0 again.
During programming sequence (V_{PP} low) the content of the programming counter, instead of the E^2PROM, defines the value of LCD voltage if SEL is high or floating, or the oscillator frequency if SEL is low. This allows the control and interactive adjustment of the appropriate parameter. E^2PROM programming must be done at ambient temperature.

E^2PROM Programming Sequence



TH ≥ 1 μs
TL > 0.5, < 1.5 μs
TE, TW = 4 to 6 ms
TD ≥ 10 μs
Time between 2 consecutive programming cycles: min. 16 ms

Fig. 5

Programming Interconnections

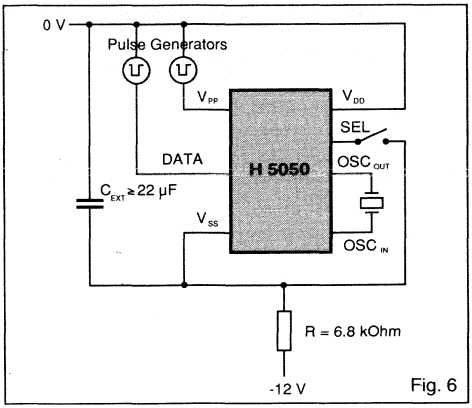


Fig. 6

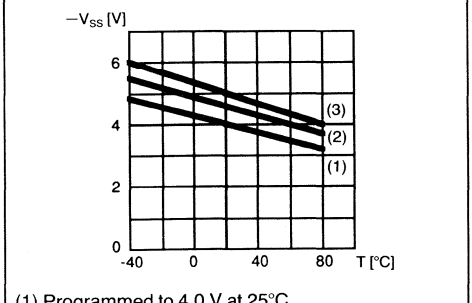
Programming Inputs

The inputs DATA, SEL and V_{PP} have internal pull-up resistors, but for safety reasons V_{PP} should be connected to V_{DD}.

LCD Voltage Programming

To enable LCD voltage programming, SEL is pulled to V_{DD} (or left floating). Then a negative voltage of -5 V in reference to V_{DD} is applied to V_{PP} to enable the programming sequence. A first negative pulse of 4 ÷ 6 ms is applied to the DATA input to clear the 5 bit voltage E^2PROM (the lowest possible LCD voltage is now programmed, and programming counter is set to 1). Any further short pulse (0.5 ÷ 1.5 µs) on the DATA input will increment the programming counter by one and therefore increase LCD voltage by one step of 150 mV typically. When the desired voltage is reached, a second long pulse (4 ÷ 6 ms) writes the value of the programming counter into the voltage E^2PROM. At the end, V_{PP} is pulled to V_{DD} again in order to leave the programming cycle.

Regulated Voltage as a Function of Temperature



(1) Programmed to 4.0 V at 25°C
(2) Programmed to 4.5 V at 25°C
(3) Programmed to 5.0 V at 25°C

Fig. 7

Frequency Programming

To enable frequency programming, SEL is pulled to V_{SS}. Then V_{SS} or -5 V in reference to V_{DD} is applied to V_{PP} to enable the programming sequence. A first negative pulse of 4 ÷ 6 ms is applied to the DATA input to clear the 5 bit frequency E^2PROM (the highest possible oscillator frequency is now programmed, and programming counter is set to 1). Any further short pulse (0.5 ÷ 1.5 µs) on the DATA input will increment the programming counter by one and therefore decrease oscillator frequency by one step (see Table 3). When the desired frequency is reached a second long pulse (4 ÷ 6 ms) writes the value of the programming counter into the frequency E^2PROM. At the end, the V_{PP} input has to be pulled to V_{DD} again in order to leave the programming cycle. Electronic adjustment of the oscillator frequency eliminates the requirement of an external trimming capacitor.

Frequency Programming ($\triangle t = 7.63$ µs)*

Frequency deviation $\triangle f/f$ [ppm]	Number of pulses n	Backplane period* [ms]
0	0	15.625
− 3.8	1	15.633
− 7.6	2	15.641
−11.4	3	15.648
...	...	...
...	...	...
−117.8	31	15.861

* Applies to programming cycle

Table 3

Static Protection and Handling

Static Protection

Input and output pads are protected against electrostatic discharges. The device is designed to withstand the following test:

Conditions: 2 kV pulse from 100 pF capacitor, 1.5 kΩ series resistance with reference to substrate V_{DD}. No degradation of pad characteristic or device performance is permitted. This test is an intrinsic part of the qualification procedure.

Handling

Reasonable care should be taken in handling and mounting operations to avoid the generation and discharge of electrostatic potentials.

Latch-up Protections

Inputs and outputs are protected against latch-up. The device is designed to withstand the following tests:

Static Latch-up

No latch-up triggered with ± 30 mA @ maximum power supply voltage.

Dynamic Latch-up

No latch-up triggered with ± 50 V from 220 pF, 50 Ω series resistance @ maximum power supply voltage.

These tests are an intrinsic part of the qualification procedure.

Typical Application

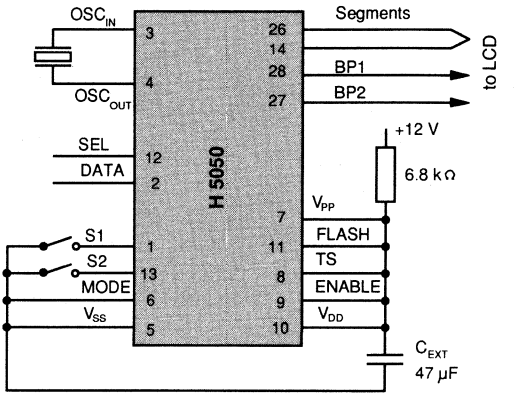


Fig. 8

Package and Ordering Information

Dimensions of SO28 Package

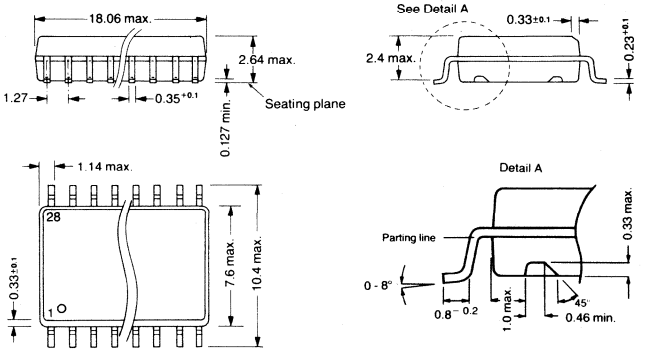


Fig. 9

Ordering Information

Option	Type	Package
1 Hz auto increment	H 5050 - 1H	SO28
2 Hz auto increment	H 5050 - 2H	SO28
4 Hz auto increment	H 5050 - 4H	SO28

Chipform and others on request.

When ordering please specify complete type and package information.

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Table of Contents

Failsafe Watchdog

Features

- Failsafe watchdog function: timeout warning after 1st timeout period, reset after 2nd timeout period, reset remains active to avoid further failures
- Standard timeout period and power-on reset time (10 ms), externally programmable if required
- V_{IN} monitoring with 3 standard or programmable trigger voltages for: power-on reset initialization, advanced power-fail warning ($\overline{SAVE}$), reset at power-down ($\overline{RES}$)
- V_{DD} monitoring: power-on reset initialization enabled only if $V_{DD} >= 3.5$ V
- Internal voltage reference
- Works down to 1.5 V supply voltage
- Push-pull or open-drain outputs
- Low current consumption
- Available for normal and extended temperature range
- DIP8 and SO8 package

Description

The H 6006 is a monolithic low power CMOS device combining a programmable digital timer and a series of voltage comparators on the same chip. The device is specially convenient for Watch-Dog functions such as microprocessor and supply voltage monitoring. The watchdog part is designed to be used in all applications where it is important that after the occurence of a malfunction the microprocessor system is stopped to avoid further damage. The timeout warning signal ($\overline{TO}$) can be used to try to reactivate the system before halting it. The voltage monitoring part provides double security by combining both unregulated voltage and regulated voltage monitoring simultaneously. The H 6006 initializes the power-on reset after V_{IN} reached V_{SH} and V_{DD} raises above 3.5 V. If V_{IN} drops below V_{SL}, the H 6006 gives an advanced warning signal for register saving and if the voltage drops further below V_{RL}, $\overline{RES}$ goes active. The H 6006 functions at any supply voltage down to 1.6V and is therefore particularly suited for start-up and shut-down control of microprocessor systems

Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems

Typical Operating Configuration

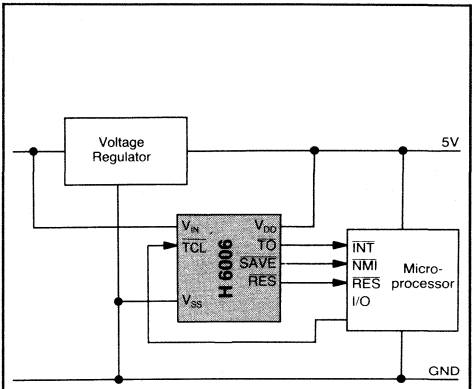


Fig. 1

Pin Assignment

DIP-8 / SO-8

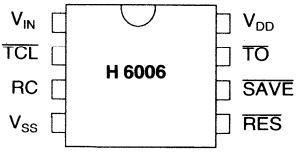


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{DD}	−0.3 to +8V
Voltage at any pin to V_{SS}	V_{MIN}	−0.3
Voltage at any pin to V_{DD} (except V_{IN})	V_{MAX}	+0.3
Voltage at V_{IN} to V_{SS}	V_{INMAX}	+15V
Current at any output	I_{MAX}	±10mA
Storage temperature	T_{STO}	−65...+150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature					
Industrial	T_{AI}	−40		+85	°C
Extended	T_{AX}	−40		+125	°C
Supply voltage	V_{DD}	1.5		5.5	V
Comparator input voltage					
Version A2, A3, B2, B3	V_{IN}	0		V_{DD}	V
Version A1, B1	V_{IN}	0		12	V
RC-oscillator programming (see Fig. 15)					
External capacitance	C1			1	µF
External resistance	R1	10			kΩ

Table 2

Electrical Characteristics

V_{DD} = 5.0 V, T_A = −40 to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{DD} activation threshold	V_{ON}	T_A = 25°C	3		3.5	V
V_{DD} deactivation threshold	V_{OFF}	T_A = 25°C		V_{ON}−1.5		V
Supply current	I_{DD}	RC open, TCL=5V, V_{IN}=0V		50	140	µA
Input V_{IN}, $\overline{TCL}$						
Leakage current	I_{IP}	$V_{SS} <= V_{IP} <= V_{DD}$, T_A = 85°C		0.005	1	µA
Input current on pin V_{IN}	I_{IN}	Versions A1, B1; V_{IN} = 10V		100	180	µA
$\overline{TCL}$ input low level	V_{IL}				0.8	V
$\overline{TCL}$ input high level	V_{IH}		2.4			V
$\overline{TO}$, $\overline{SAVE}$, $\overline{RES}$ Outputs						
Leakage current	I_{OLK}	Versions A1, A2, A3; $V_{OUT} = V_{DD}$		0.05	1	µA
Drive currents (all versions)	I_{OL}	V_{OL} = 0.4V	3.2	8		mA
	I_{OL}	V_{DD} = 3.5V; V_{OL} = 0.4V	2			mA
	I_{OL}	V_{DD} = 1.6V; V_{OL} = 0.4V	80			µA
Drive currents (versions B1, B2, B3)[1]	I_{OH}	V_{OH} = 4.0V	3.2	8		mA
	I_{OH}	V_{DD} = 3.5V; V_{OH} = ≥ 2.8V	2			mA
	I_{OH}	V_{DD} = 1.6V; V_{OH} = V_{DD}−0.4	80			µA

[1] Versions: An = open drain outputs; Bn = push-pull outputs

Table 3

V_{IN} Surveillance

Voltage thresholds at T_A = 25°C

Version[1]	Comparator Reference	Input Resistance R_{VIN}	Thresholds	Threshold Tolerance	Ratio Tolerance[3]
A1, B1	V_{DD}	100kΩ	9.00 8.00 7.00[2]	± 5%	± 2%
A2, B2	V_{DD}	~100MΩ	2.25 2.00 1.75[2]	± 5%	± 2%
A3, B3	Band-gap reference	~100MΩ	2.00 1.95 1.90	±10%	± 2%

[1] Versions: An = open drain outputs; Bn = push-pull outputs

[2] at V_{DD} = 5V

[3] Threshold ratio as V_{SH}/V_{SL} or V_{SL}/V_{RL}

Table 4

Timing Characteristics

V_{DD} = 5.0 V, T_A = −40°C to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{TCL}$ to output pins	T_{DIDO}			250	500	ns
V_{IN} to output pins	T_{AIDO}	Excluding debounce time T_{DB}		4	10	µs
Logic transition times on all output pins	T_{TR}	Load 10kΩ, 100pF		30	100	ns
Timeout period	T_{TO}	RC open, unshielded, T_A = 25°C	6	10	16	ms
	T_{TO}	RC open, unshielded (not tested)	4.5		20	ms
T_{TCL} input pulse width	T_{TCL}		150			ns
Power-on reset debounce	D_{DB}			$T_{TO/32}$		ms

Table 5

Timing Waveforms

Voltage reaction: V_{DD} Monitoring

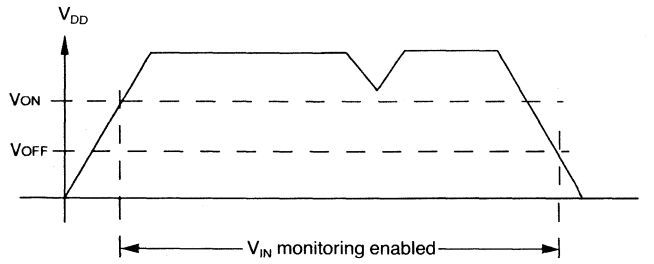
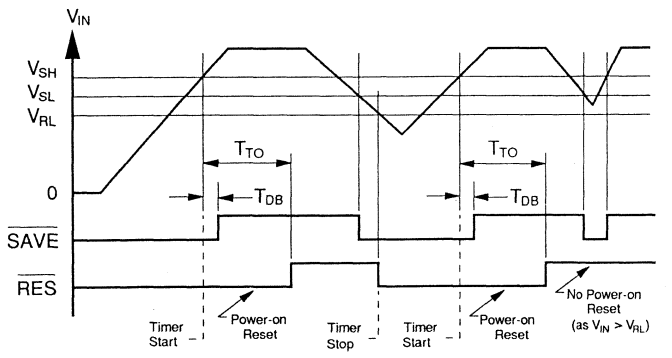


Fig. 3

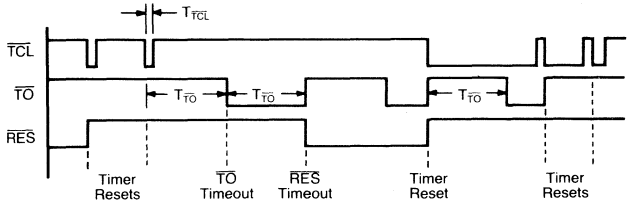
Voltage Reaction: V_{IN} Monitoring



Conditions:
$V_{DD} > V_{ON}$.
No timeout.

Fig. 4

Timer Reaction



Conditions:
$V_{IN} > V_{RL}$ after power-up sequence.

Fig. 5

Combined Voltage and Timer Reaction

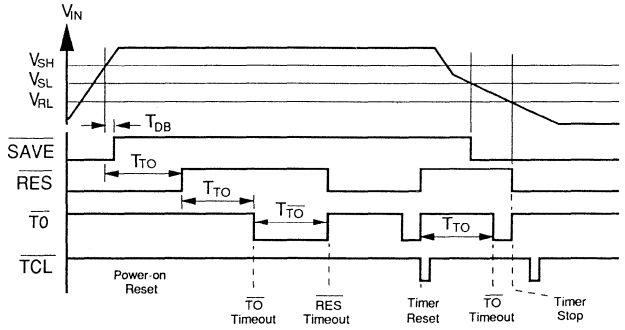
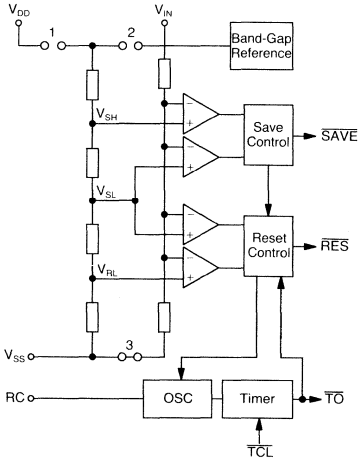


Fig. 6

Block Diagram



Version	Connections
A1, B1	1 and 3
A2, B2	1
A3, B3	2

Fig. 7

Pin Description

Pin	Name	Function
1	V_{IN}	Voltage monitoring input
2	$\overline{TCL}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V_{SS}	GND terminal
5	$\overline{RES}$	Reset output
6	$\overline{SAVE}$	Save output
7	$\overline{TO}$	Timer output signal
8	V_{DD}	Positive supply voltage terminal

Table 6

Functional Description

Supply Lines

The circuit is powered through the V_{DD} and V_{SS} pins. It monitors both its own V_{DD} supply and a voltage applied to the V_{IN} input.

V_{DD} Monitoring

During power-up the V_{IN} monitoring is disabled and $\overline{RES}$ and $\overline{SAVE}$ stay active low as long as V_{DD} is below V_{ON} (3.5V). As soon as V_{DD} reaches the V_{ON} level, the state of the outputs depend on the watchdog timer and the voltage at V_{IN} relative to the thresholds (see Fig. 3 and 4). If the supply voltage V_{DD} falls back below V_{OFF} (1.5V) the watchdog timer and the V_{IN} monitoring are disabled and the outputs $\overline{SAVE}$ and $\overline{RES}$ are active low. The V_{DD} line should be free of spikes.

V_{IN} Monitoring

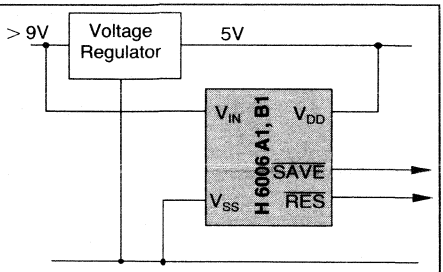
The analog voltage comparators compare the voltage applied to V_{IN} (typically connected to the input of the voltage regulator) with the stabilized supply voltage V_{DD} (versions A1, B1, A2, B2) or with the bandgap voltage (versions A3, B3) (see Fig. 7). At power-up, when V_{DD} reached V_{ON} and V_{IN} reaches the V_{SH} level, the $\overline{SAVE}$ output goes high, and the timer starts running, setting $\overline{RES}$ high after the time T_{TO} (see Fig. 4). If V_{IN} falls below V_{SL}, the $\overline{SAVE}$ output goes low and stays low until V_{IN} rises again above V_{SH}. If V_{IN} falls below the voltage V_{RL}, the $\overline{RES}$ output will go low and the on-chip timer will stop. When V_{IN} rises again above V_{SH}, the timer will initiate a power-up sequence. The $\overline{RES}$ output may however be influenced independently of the voltage V_{IN} by the timer action, see section „Combined Voltage and Timer Action". Monitoring the rough DC side of the regulator as shown in Fig. 12 is the only way to have advanced warning at power-down. Spikes on V_{IN} should be filtered if they are likely to drop below V_{SL}.

The combination of V_{IN} and V_{DD} monitoring provide high system security: if V_{IN} rises much faster than V_{DD}, then the device starts the power-on sequence only when V_{DD} reached V_{ON} (Fig. 3). Short circuits on the regulated supply voltage can be detected.

Voltage Thresholds on V_{IN}

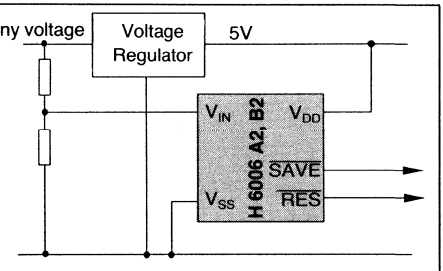
The H 6006 is available with 3 different sets of thresholds:

Version A1, B1: with internal voltage divider, resulting in thresholds for direct monitoring of the unregulated voltage without external components.



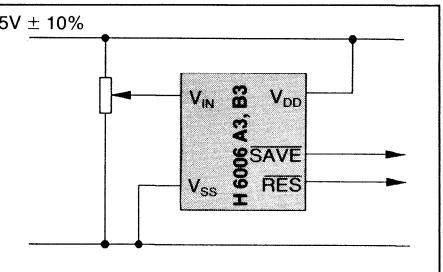
Note: The threshold levels are 9/8/7 V normally. These are divided internally by 4 to give internal thresholds of 2.25 / 2 / 1.75 V. V_{DD} = 5V (thresholds dependent on V_{DD}). R_{VIN} = ~ 100kΩ Fig. 8

Version A2, B2: for monitoring of all unregulated voltage, where custom programming is required. Fix resistor values can be used for programming.



Note: the internal threshold levels are 2.25/2.00/1.75V at V_{DD} = 5V (threshold dependent on V_{DD}). R_{VIN} = ~100MΩ Fig. 9

Version A3, B3: for monitoring of regulated voltage, where no unregulated voltage is available (the tolerance is ± 10%, see Tabel 4. For tighter tolerances, trimming can be used, see Fig. 10).



Note: the internal threshold levels are 2.00/1.95/1.90V (threshold dependent on the internal bandgap reference) R_{VIN} = ~100MΩ Fig. 10

Monitoring of the unregulated voltage require versions A1, B1, A2 and B2. The versions are based on the principle that V_{DD} rises with V_{IN} on power-up and V_{DD} holds up for a certain time after V_{IN} starts dropping on power-down. The version A1 and B1 have a 100kΩ nominal resistance from V_{IN} to V_{SS} (internal voltage divider). The versions A2, B2, A3 and B3 have high impedance V_{IN} inputs (see Fig. 7 and Table 4) for external threshold voltage programming by a voltage divider on pin V_{IN}. The levels obtained are proportional to the internal levels V_{SH}, V_{SL} and V_{RL} on the chip itself (see Electrical Specifications).

Timer Programming

With pin RC unconnected, the on-chip RC oscillator together with its divider chain give a timeout T_{TO} of typically 10ms. For programming a different T_{TO}, an approximation for calculating component values is given by the formula:

$$T_{TO} = \left[0.75 + \frac{(32 + C_1) \cdot 1.6}{5.5 + \frac{V_{DD} - 0.8}{R_1}} \right] \cdot 1.024$$

$R_{1\,min.} = 10\,k\Omega$, $C_{1\,max.} = 1\,\mu F$

If R_1 is in MΩ and C_1 in pF, T_{TO} will be in ms.

Thus, a resistor decreases and a capcitor increases the interval to timeout. By using both external components, excellent temperature stability of T_{TO} can be achieved. With $\overline{TCL}$ tied to either V_{DD} or V_{SS}, a precise square wave of period 2 x T_{TO} is generated at the output $\overline{TO}$. The oscillator and watchdog timer run so long as the chip is powered with at least the minimum positive supply voltage specified (V_{ON}), and so long as V_{IN} remains above the level V_{RL} after a power-up sequence. If the timer function is not required, input $\overline{TCL}$ should be tied to output $\overline{TO}$ to give a simple voltage monitor (see Fig. 14).

Timer Clearing and $\overline{RES}$ Action

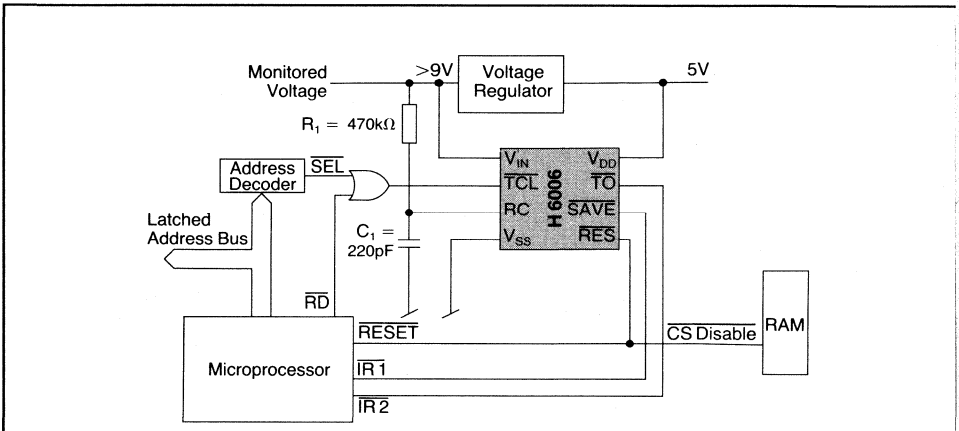
A negative edge or a negative pulse at the $\overline{TCL}$ input longer than 150ns will reset the timer and set $\overline{TO}$ high. If a further $\overline{TCL}$ signal edge or pulse is applied before T_{TO} timeout, $\overline{TO}$ will stay high and the timer will again be reset to zero (see Fig. 5). If no $\overline{TCL}$ signal is applied before the T_{TO} timeout, $\overline{TO}$ will start to generate a square wave of period 2 x T_{TO} starting with a low state. If no $\overline{TCL}$ signal is applied during the first low state of $\overline{TO}$, then the $\overline{RES}$ output will go low and stay low until the next $\overline{TCL}$ signal, or until a fresh power-up sequence.

Combined Voltage and Timer Action

The combination of voltage and timer action is illustrated by the sequence of events shown in Fig. 6. One timeout period after V_{IN} reached V_{SH}, during power-up, $\overline{RES}$ goes inactive high. No $\overline{TCL}$ pulse will have any effect until this power-on reset delay is completed. After completing the power-up sequence the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, the timeout warning $\overline{TO}$ goes active low after one timeout period T_{TO}. After each subsequent timeout period without a timer clear pulse $\overline{TCL}$, $\overline{TO}$ changes its polarity providing a square wave signal. $\overline{RES}$ activates at the end of the first low state of the $\overline{TO}$ signal. A $\overline{TCL}$ pulse clears the watchdog timer and resets the $\overline{TO}$ and $\overline{RES}$ output inactive high again. A voltage drop below the V_{RL} level overrides the timer and immediately forces $\overline{RES}$ and $\overline{SAVE}$ active low and disables $\overline{TO}$. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Typical Applications

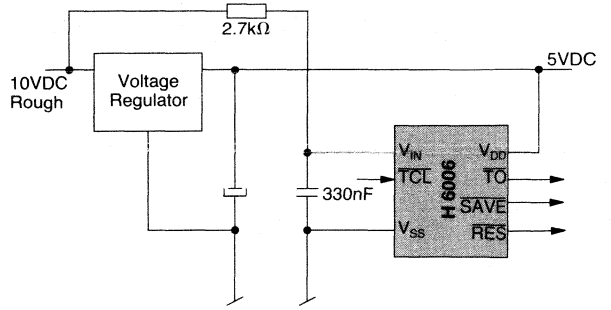
Microprocessor Watchdog with Power-On Reset and Voltage Monitor



T_{TO} = ~ 30 ms

Fig. 11

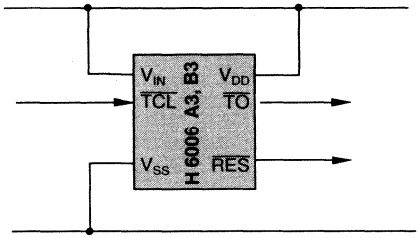
Voltage Monitor with Spike Suppression



Version A1 or B1

Fig. 12

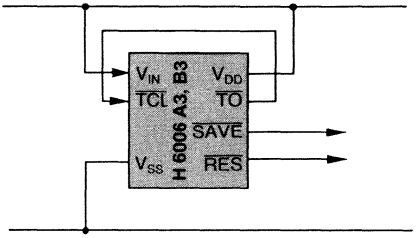
Watchdog and Power-On Reset



If only V_{DD} monitoring is used, (i.e. V_{IN} and V_{DD} common) then the version A3 or B3 with its constant thresholds are recommended. The power-on reset function is still available as the V_{DD} monitoring is active.

Fig. 13

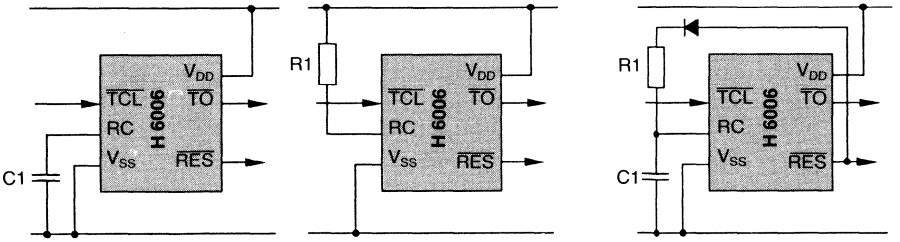
V_{DD} Monitoring and Power-On Reset



V_{IN} monitoring and watchdog function not used. Versions A3 and B3 only.

Fig. 14

External Programming of RC Oscillator



C1 increases T_{TO}

R1 shortens T_{TO}

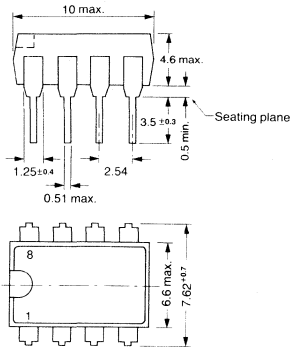
This circuit provides independent programming of both timeout period and power-on reset delay.

Note: using both external components R1 and C1 allows to achieve tighter timeout period tolerances.

Fig. 15

Package and Ordering Information

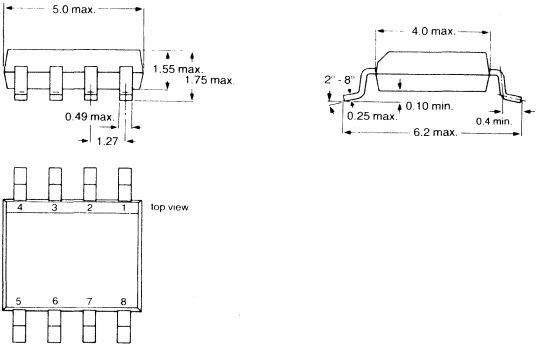
Dimensions of DIP8 Package



Dimensions in mm

Fig. 16

Dimensions of SO8 Package



Dimensions in mm

Fig. 17

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
H 6006 nn 8P	DIP8
H 6006 nn 8S	SO8

Extended temperature range (−40 to +125°C)

Type[1]	Package
H 6006 nnX 8P	DIP8*
H 6006 nnX 8S	SO8*

[1] nn stands for the versions A1*, B1, A2, B2, A3, B3
* and chip form, on request

The H 6006 standard versions are as shown in the electrical specifications:

H 6006 n1
H 6006 n2
H 6006 n3

The device has the option of open-drain or push-pull outputs:

H 6006 An	open-drain outputs
H 6006 Bn	push-pull outputs

When ordering please specify complete part number.

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Self Recovering Watchdog

Features

- Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- Standard timeout period and power-on reset time (100ms), externally programmable if required
- Unregulated DC monitoring (V_{IN}) with 3 standard or programmable trigger voltages for: power-on reset initialization, advanced power-fail warning ($\overline{SAVE}$), reset at power-down ($\overline{RES}$)
- Regulated DC monitoring (V_{DD}): power-on reset initialization enabled only if $V_{DD} >= 3.5V$
- Internal voltage reference
- Works down to 1.6V supply voltage
- Push-pull or open-drain outputs
- Low current consumption
- Available for normal and extended temperature ranges
- DIP8 and SO8 package

Description

The H 6060 is a monolithic low-power CMOS device combining a programmable timer and a series of voltage comparators on the same chip. The device is specially suited for watchdog functions such as microprocessor and supply voltage monitoring. If the μP system malfunctions, the watchdog will recover it by issuing repeated active reset signals. The voltage monitoring part provides double security by combining both the unregulated voltage (V_{IN}) and the regulated voltage (V_{DD}) monitoring simultaneously. The H 6060 initializes the power-on reset after V_{IN} reaches V_{SH} (see table 4) and V_{DD} rises above 3.5V. If V_{IN} drops below V_{SL} (see table 4), the H 6060 gives an advanced warning signal for register saving and if the voltage drops further below V_{RL} (see table 4), $\overline{RES}$ and RES go active. The H 6060 functions at any supply voltage down to 1.6V and is therefore particularly suited for start-up and shut-down control of microprocessor systems.

Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems

Typical Operating Configuration

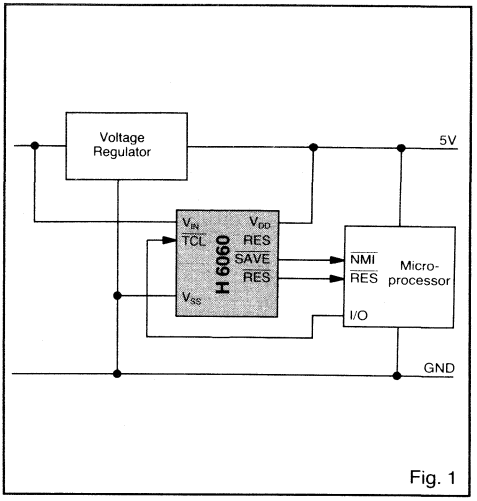


Fig. 1

Pin Assignment

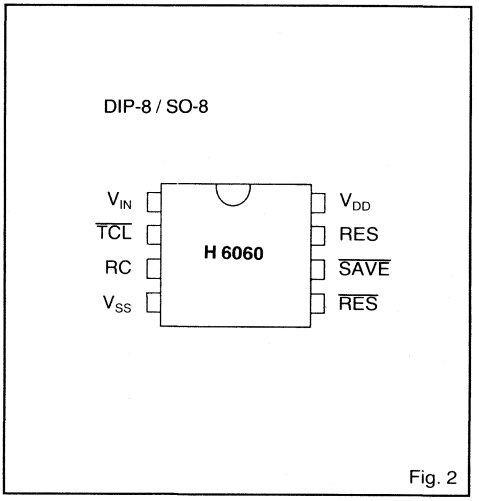


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{DD}	−0.3 to +8V
Voltage at any pin to V_{SS}	V_{MIN}	−0.3
Voltage at any pin to V_{DD} (except V_{IN})	V_{MAX}	+0.3
Voltage at V_{IN} to V_{SS}	V_{INMAX}	+15V
Current at any output	I_{MAX}	±10mA
Storage temperature	T_{STO}	−65...+150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature					
Industrial	T_{AI}	−40		+85	°C
Extended	T_{AX}	−40		+125	°C
Supply voltage	V_{DD}	1.6		5.5	V
Comparator input voltage					
Version 13, 14, 15, 16	V_{IN}	0		V_{DD}	V
Version 11, 12	V_{IN}	0		12	V
RC-oscillator programming (see Fig. 15)					
External capacitance*	C1			1	µF
External resistance	R1	10			kΩ

* Leakage < 1µA

Table 2

Electrical Characteristics

V_{DD} = 5.0 V, T_A = −40 to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{DD} activation threshold	V_{ON}	T_A = 25°C	3		3.5	V
V_{DD} deactivation threshold	V_{OFF}	T_A = 25°C		V_{ON}−0.3		V
Supply current	I_{DD}	RC open, TCL at V_{DD} or V_{SS}		80	140	µA
Input V_{IN}, $\overline{TCL}$						
Leakage current	I_{IP}	$V_{SS} <= V_{IP} <= V_{DD}$; T_A = 85°C		0.005	1	µA
Input current on pin V_{IN}	I_{IN}	Versions 11, 12; V_{IN} = 10V		100	180	µA
$\overline{TCL}$ input low level	V_{IL}				0.8	V
$\overline{TCL}$ input high level	V_{IH}		2.4			V
$\overline{SAVE}$, $\overline{RES}$, RES outputs						
Leakage current	I_{OLK}	Versions 11, 13, 15; V_{OUT} = V_{DD}		0.05	1	µA
Drive currents (all versions)	I_{OL}	V_{OL} = 0.4V	3.2	8		mA
	I_{OL}	V_{DD} = 3.5V; V_{OL} = 0.4V	2			mA
	I_{OL}	V_{DD} = 1.6V; V_{OL} = 0.4V	80			µA
Drive currents (versions 12, 14, 16)[1]	I_{OH}	V_{OH} = 4.0V	3.2	8		mA
	I_{OH}	V_{DD} = 3.5V; V_{OH} = 2.8V	2			mA
	I_{OH}	V_{DD} = 1.6V; V_{OH} = 1.2V	80			µA

[1] Versions: 11, 13, 15 = open drain outputs; 12, 14, 16 = push-pull outputs

Table 3

V_{IN} Surveillance

Voltage thresholds at T_A = 25°C

Version[1]	Comparator Reference	Input Resistance on V_{IN} (R_{VIN})	Thresholds V_{SH}	V_{SL}	V_{RL}	Threshold Tolerance	Ratio Tolerance[3]
11, 12	V_{DD}	100kΩ	9.00	8.00	7.00[2]	± 5%	±2%
13, 14	V_{DD}	~100MΩ	2.25	2.00	1.75[2]	± 5%	±2%
15, 16	Band-gap reference	~100MΩ	2.00	1.95	1.90	±10%	±2%

[1] Versions: 11, 13, 15 = open drain outputs; 12, 14, 16 = push-pull outputs

[2] at V_{DD} = 5V

[3] Threshold ratio tolerance is defined as the tolerance of V_{SH}/V_{SL} and V_{SL}/V_{RL}

Table 4

Timing Characteristics

V_{DD} = 5.0 V, T_A = −40°C to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{TCL}$ to output pins	T_{DIDO}			250	500	ns
V_{IN} to output pins	T_{AIDO}	Excluding debounce time T_{DB}		4	10	µs
Logic transition times on all output pins	T_{TR}	Load 10kΩ, 100pF		30	100	ns
Timeout period	T_{TO}	RC open, unshielded, T_A = 25°C	60	100	160	ms
	T_{TO}	RC open, unshielded (not tested)	45		200	ms
T_{TCL} input pulse width	T_{TCL}		150			ns
Power-on reset debounce	T_{DB}			$T_{TO}/64$		ms
V_{IN} low pulse	T_{VINL}	Where debounce time T_{DB} is guaranteed	10			µs

Table 5

Timing Waveforms

Voltage reaction: V_{DD} Monitoring

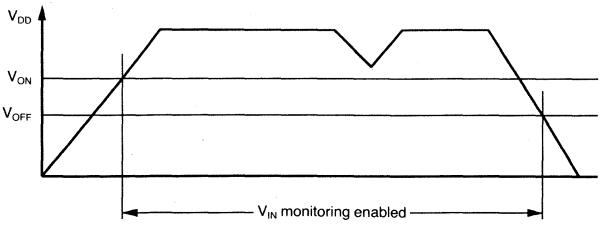
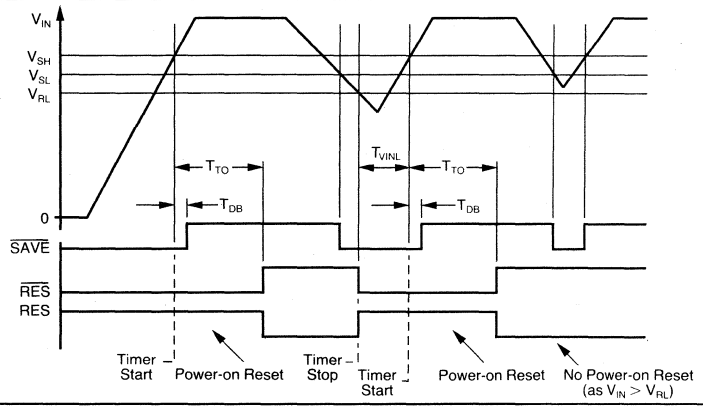


Fig. 3

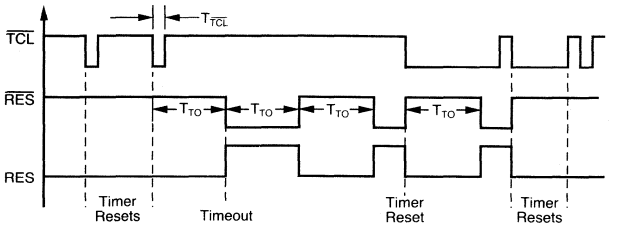
Voltage Reaction: V_{IN} Monitoring



Conditions:
$V_{DD} > V_{ON}$.
No timeout.

Fig. 4

Timer Reaction



Conditions:
$V_{IN} > V_{RL}$ after power-up sequence

Fig. 5

Combined Voltage and Timer Reaction

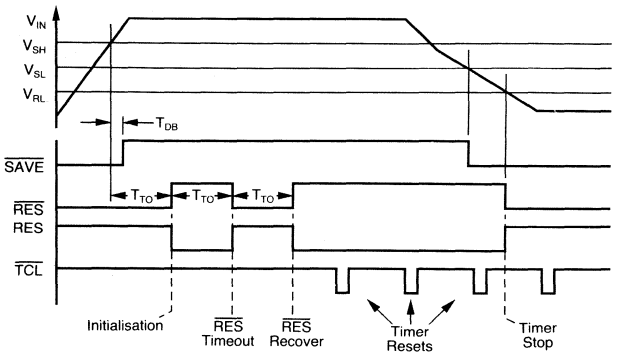
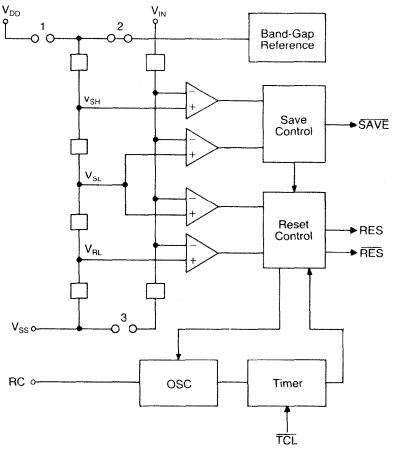


Fig. 6

Block Diagram



Version	Connections
11, 12	1 and 3
13, 14	1
15, 16	2

Fig. 7

Pin Description

Pin	Name	Function
1	V_{IN}	Voltage sense input
2	$\overline{TCL}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V_{SS}	GND terminal
5	$\overline{RES}$	Active low reset output
6	$\overline{SAVE}$	Save output
7	RES	Active high reset output
8	V_{DD}	Positive supply voltage terminal

Table 6

Functional Description

Supply Lines

The circuit is powered through the V_{DD} and V_{SS} pins. It monitors both its own V_{DD} supply and a voltage applied to the V_{IN} input.

V_{DD} Monitoring

During power-up the V_{IN} monitoring is disabled and $\overline{RES}$, RES and $\overline{SAVE}$ stay active low as long as V_{DD} is below V_{ON} (3.5V). As soon as V_{DD} reaches the V_{ON} level, the state of the outputs depend on the watchdog timer and the voltage at V_{IN} relative to the thresholds (see Fig. 4). If the supply voltage V_{DD} falls back below V_{OFF} (V_{ON} - 0.3V) the watchdog timer and the V_{IN} monitoring are disabled and the outputs $\overline{RES}$, RES and $\overline{SAVE}$ become active. The V_{DD} line should be free of voltage spikes.

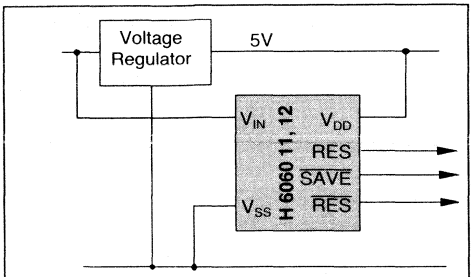
V_{IN} Monitoring

The analog voltage comparators compare the voltage applied to V_{IN} (typically connected to the input of the voltage regulator) with the stabilized supply voltage V_{DD} (versions 11, 12, 13, 14) or with the bandgap voltage (versions 15, 16) (see Fig. 7). At power-up, when V_{DD} reached V_{ON} and V_{IN} reaches the V_{SH} level, the $\overline{SAVE}$ output goes inactive, and the timer starts running, setting $\overline{RES}$ and RES inactive after the time T_{TO} (see Fig. 4). If V_{IN} falls below V_{SL}, the $\overline{SAVE}$ output goes active and stays activeuntil V_{IN} rises again above V_{SH}. If V_{IN} falls below the voltage V_{RL}, $\overline{RES}$ and RES will become active and the on-chip timer will stop. When V_{IN} rises again above V_{SH}, the timer will initiate a power-up sequence. The $\overline{RES}$ and RES outputs may however be influenced independently of the voltage V_{IN} by the timer action, see section „Combined Voltage and Timer Action". Monitoring the rough DC side of the regulator, as shown in Fig. 12, is the only way to have advanced warning of power-down. Spikes on V_{IN} should be filtered if they are likely to exceed the value (V_{SL} - V_{RL}).
The combination of V_{IN} and V_{DD} monitoring provide high system security: if V_{IN} rises much faster than V_{DD}, then the device starts the power-on sequence only when V_{DD} reached V_{ON} (Fig. 11). Short circuits on the regulated supply voltage can be detected.

Voltage Thresholds on V_{IN}

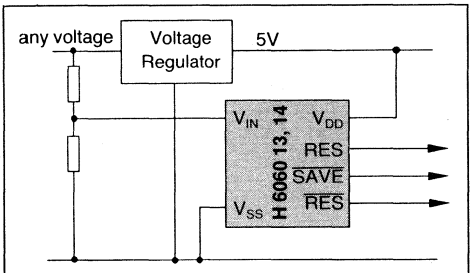
The H 6060 is available with 3 different sets of thresholds:

Version 11, 12: have an internal voltage divider for direct monitoring of the unregulated voltage without external components.



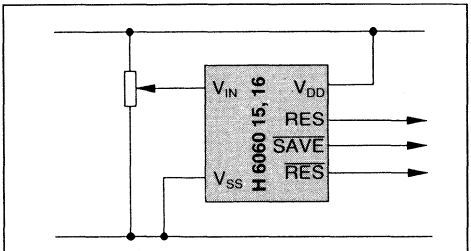
Note: internal threshold levels: 9/8/7V at V_{DD} = 5V (thresholds relative to V_{DD}, see table 4 and fig. 4) R_{VIN} = ~100kΩ Fig. 8

Version 13, 14: monitor the unregulated voltage and are ideal for programming of the V_{IN} voltage thresholds. Fixed resistor values can be used for programming.



Note: internal threshold levels: 2.25/2.00/1.75V at V_{DD} = 5V (thresholds relative to V_{DD}, see table 4 and fig. 4) R_{VIN} = ~100MΩ Fig. 9

Version 15, 16: monitor the regulated voltage. They are suited to applications where the unregulated voltage is not available. (The tolerance is ± 10%, see table 4. For tighter tolerances, trimming can be used, see fig. 10).



Note: internal threshold levels: 2.00/1.95/1.90V (thresholds relative to internal bandgap reference) R_{VIN} = ~100MΩ Fig. 10

6

Monitoring of the unregulated voltage requires versions 11, 12, 13 and 14. These versions are based on the principle that V_{DD} rises with V_{IN} on power-up and V_{DD} holds up for a certain time after V_{IN} starts dropping on power-down. The versions 11 and 12 have a 100kΩ nominal resistance from V_{IN} to V_{SS} (internal voltage divider). The versions 13, 14, 15 and 16 have high impedance V_{IN} inputs (see fig. 7 and table 4) for external threshold voltage programming by a voltage divider on pin V_{IN}. The levels obtained are proportional to the internal levels V_{SH}, V_{SL} and V_{RL} on the chip itself (see Electrical Specifications).

Timer Programming

With pin RC unconnected, the on-chip RC oscillator together with its divider chain give a timeout T_{TO} of typically 100ms. To program different T_{TO}, an approximation for calculating component values is given by the formula:

$$T_{TO} = \left[0.75 + \frac{(32 + C_1) \cdot 2}{5.5 + \frac{V_{DD} - 1}{R_1}} \right] \cdot 8.192$$

$R_{1\,min.} = 10\,k\Omega$, $C_{1\,max.} = 1\,\mu F$

If R_1 is in MΩ and C_1 in pF, T_{TO} will be in ms.

A resistor decreases and a capacitor increases the interval to timeout. Excellent temperature stability of T_{TO} can be achieved by using external components. A precise square wave of period 2 x T_{TO} is generated at the outputs $\overline{RES}$ and RES when $\overline{TCL}$ is tied to either V_{DD} or V_{SS}. The oscillator and watchdog timer start running when both V_{IN} is greater than V_{SH} (see fig. 6) and V_{DD} is greater than V_{ON} (see fig. 3).

They will remain running while both V_{IN} is greater than V_{RL} and V_{DD} is greater than V_{OFF} (see fig. 3).

Timer Clearing and $\overline{RES}$/RES Action

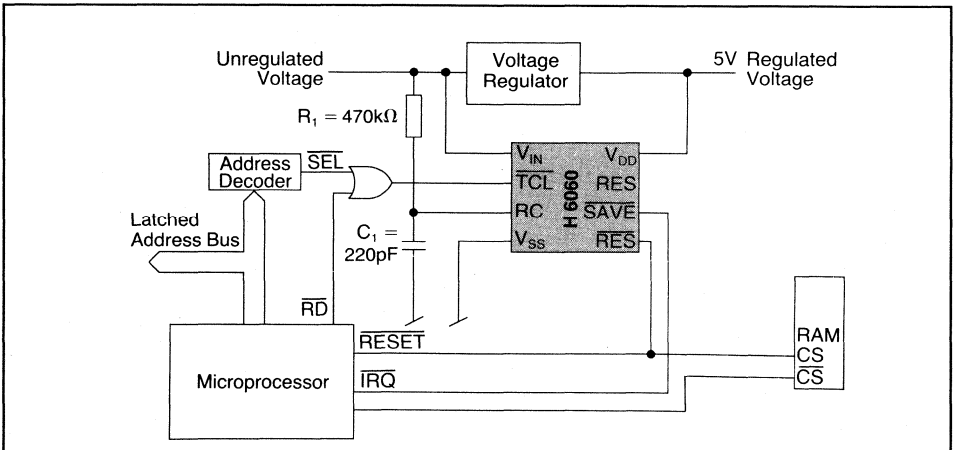
A negative edge or a negative pulse at the $\overline{TCL}$ input for longer than 150ns will reset the timer and set $\overline{RES}$ and RES inactive. If a further $\overline{TCL}$ signal edge or pulse is applied before T_{TO} timeout, $\overline{RES}$ and RES will remain inactive and the timer will again be reset to zero (see fig. 5). If no $\overline{TCL}$ signal is applied before the T_{TO} timeout, $\overline{RES}$ and RES will start to generate square waves of period 2 x T_{TO} starting with the inactive state. The watchdog will remain in this state until the next $\overline{TCL}$ signal appears, or until a fresh power-up sequence.

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in fig. 6. One timeout period after V_{IN} reaches V_{SH}, during power-up, $\overline{RES}$ and RES go inactive. A $\overline{TCL}$ pulse will have no effect until this power-on reset delay is completed. After completing the power-up sequence the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ and RES go active after one timeout period T_{TO}. After each subsequent timeout period, without a timer clear pulse at $\overline{TCL}$, $\overline{RES}$ and RES change polarity providing square wave signals. A $\overline{TCL}$ pulse clears the watchdog timer and causes $\overline{RES}$ and RES to go inactive. A voltage drop below the V_{RL} level overrides the timer and immediately forces $\overline{RES}$, RES and $\overline{SAVE}$ active. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence is completed.

Typical Applications

Microprocessor Watchdog with Power-On Reset and Voltage Monitor



$T_{TO} \times \sim 300$ ms

Fig. 11

Voltage Monitor with Spike Suppression

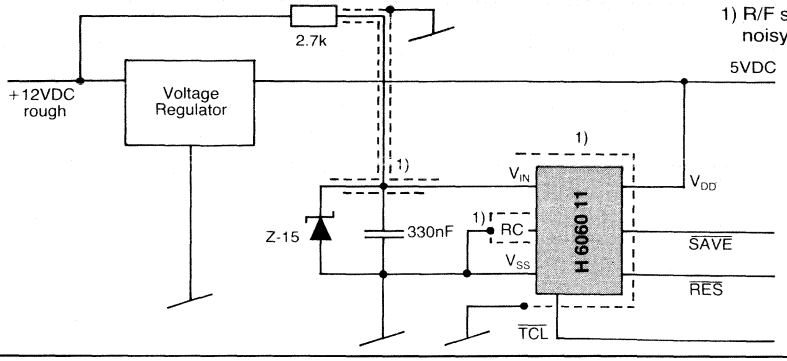
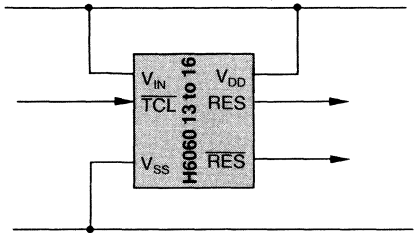


Fig. 12

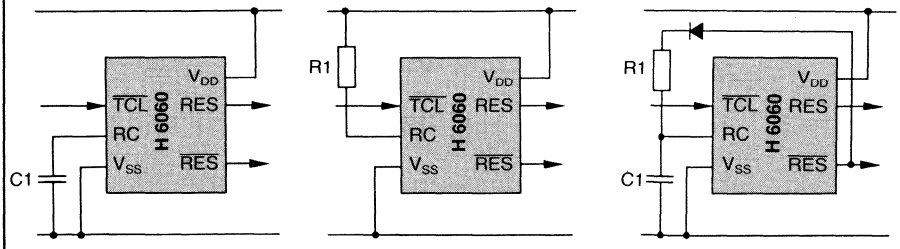
Watchdog and Power-On Reset



If precise thresholds are not required then V_{IN} monitoring on versions 13 to 16 can be disabled by tying V_{IN} to V_{DD}. The V_{DD} monitoring is still active and power-up reset occurs at V_{ON} and power-down reset at V_{OFF} threshold.

Fig. 13

External Programming of RC Oscillator



C1 increases T_{TO}

R1 shortens T_{TO}

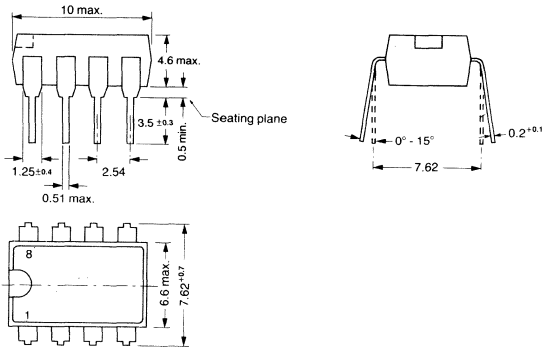
This circuit provides independent programming of both timeout period and power-on reset delay.

Note: if external components R1 and C1 are used, a tighter timeout period tolerance can be achieved.

Fig. 14

Package and Ordering Information

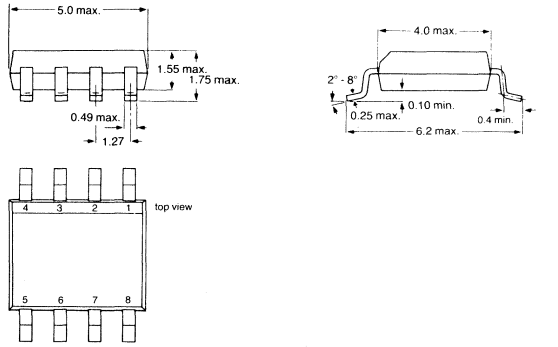
Dimensions of DIP8 Package



Dimensions in mm

Fig. 15

Dimensions of SO8 Package



Dimensions in mm

Fig. 16

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
H 6060 nn 8P	DIP8
H 6060 nn 8S	SO8

Extended temperature range (−40 to +125°C)

Type[1]	Package
H 6060 nnX 8P	DIP8*
H 6060 nnX 8S	SO8*

[1] nn stands for the versions 11*, 12*, 13*, 14, 15, 16
* and chip form, on request

The H 6060 standard versions are as shown in the electrical specifications:

	open-drain outputs	push-pull outputs
H 6060	11	12
H 6060	13	14
H 6060	15	16

When ordering please specify complete part number.

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3 V Self Recovering Watchdog

Features

- **Watchdog fully operational from 2.7 to 5.25 V**
- Regulated DC voltage monitor, internal voltage reference
- Self recovering watchdog function: reset goes active after 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- Standard timeout period and power-on reset time (100 ms), externally programmable from 3 ms to 3 mins if required
- Works down to 1.6 V supply voltage
- Low voltage alarm prior to reset on power-down
- Reset outputs of both polarities
- Open drain outputs
- Small footprint SO8 and DIP8 packages

Description

The H 6061 is a combined initialiser, watchdog and voltage monitor. The circuit is a low voltage low power monolithic CMOS device combining a series of voltage comparators and a programmable timer on the same chip. The device is specially suited to telecommunications applications where 3V working is expected, for functions such as supply voltage and microprocessor monitoring. The reset outputs are self recovering after a watchdog timeout, enabling the circuit to work with standalone systems without any external push-switch or control signal to restart after a watchdog timeout. The circuit provides a reset signal of both polarities. The state of the outputs is defined down to 1.6 V. An internal debouncer ensures power-up performance for fast-rise supply lines.

Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems
- Microcontroller 68HC05 applications

Typical Operating Configuration

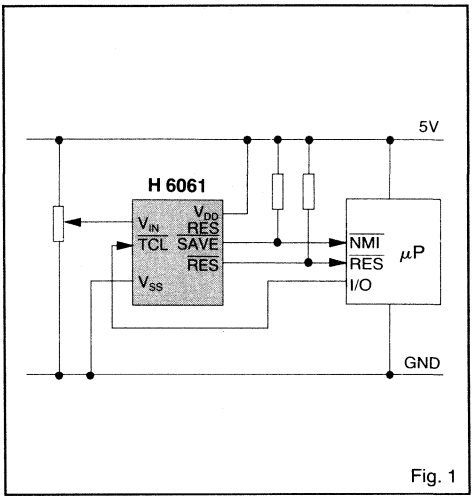


Fig. 1

Pin Assignment

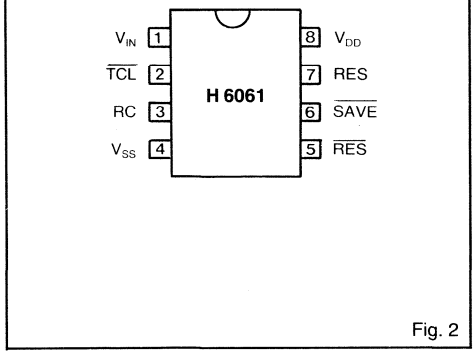


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{DD}	−0.3 to +5.6V
Voltage at any pin to V_{SS}	V_{MIN}	−0.3
Voltage at any pin to V_{DD}	V_{MAX}	+0.3
Voltage at V_{IN} to V_{SS}	V_{INMAX}	+12V
Current at any output	I_{MAX}	±10mA
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-833C method 3015	V_{Smax}	1000V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, it is advised that normal precautions be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unuwed inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature Industrial	T_A	−40		+85	°C
Supply voltage	V_{DD}	2.7		5.25	V
Monitored input voltage	V_{IN}	0		12	V
RC-oscillator programming (see Fig. 15)					
External capacitance*	C1			1	μF
External resistance	R1	10			kΩ

* Leakage < 1μA

Table 2

Electrical Characteristics

V_{DD} = 5V, T_A = −40°C to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD} activation threshold	V_{ON}	T_A = 25°C	2.3		2.7	V
V_{DD} deactivation threshold	V_{OFF}	T_A = 25°C		V_{ON}−0.3		V
Supply current	I_{DD}	RC open, $\overline{TCL}$ at V_{DD} or V_{SS}		80	140	μA
Input V_{IN}, $\overline{TCL}$						
Leakage current	I_P	$V_{SS} < V_{IP} < V_{DD}$;				
		T_A = 80°C		0.005	1	μA
$\overline{TCL}$ input low level	V_{IL}				0.8	V
$\overline{TCL}$ input high level	V_{IH}		2.4			V
Leakage on pins $\overline{SAVE}$, $\overline{RES}$, RES	I_{OLK}	$V_{OUT} = V_{DD}$		0.050	1	μA
O/P drive logic low	I_{OL}	V_{OL} = 0.4V	4	8		mA
	I_{OL}	V_{DD} = 3.5 V; V_{OL} = 0.4 V	2			mA
	I_{OL}	V_{DD} = 1.6 V; V_{OL} = 0.4 V	80			μA

Table 3

V_{IN} Surveillance

Voltage thresholds at T_A = 25°C

Version No.	Thresholds V_{SH}	V_{SL}	V_{RL}	at V_{DD}	Threshold Voltage Tolerance	Threshold Ratio*	Pin V_{IN} Input
25	1.54	1.50	1.46	2.7 - 5.0V	±10%	±2%	~100MΩ

* Threshold ratio defined as V_{SH} / V_{SL} or V_{SL} / V_{RL}

Table 4

Timing Characteristics

V_{DD} = 5.0 V, T_A = −40°C to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{TCL}$ to output pins	T_{DIDO}			250	500	ns
V_{IN} to output pins	T_{AIDO}	Excluding debounce time T_{DB}		4	10	µs
Logic transition times on all output pins	T_{TR}	Load 10kΩ, 100pF		30	100	ns
Timeout period	T_{TO}	RC open, unshielded, T_A = 25°C	60	100	160	ms
T_{TCL} input pulse width	T_{TCL}		150			ns
Power-on reset debounce	T_{DB}			T_{TO}/64		ms
Fastest pulse V_{IN} with debounce	T_{VINL}	−40° to +85°C	10			µs

Table 5

Timing Waveforms

Voltage reaction: V_{DD} Monitoring

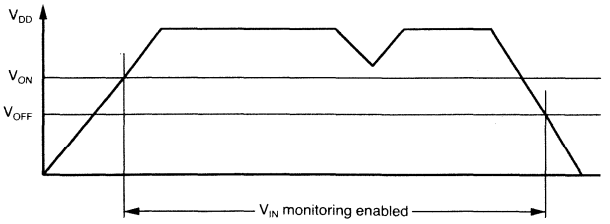
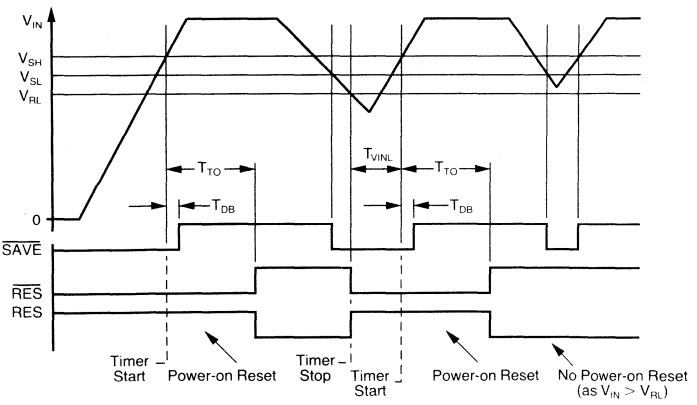


Fig. 3

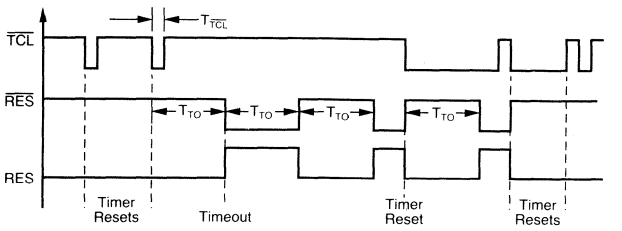
Voltage Reaction: V_{IN} Monitoring



Conditions:
$V_{DD} > V_{ON}$.
No timeout.
sequence.

Fig. 4

Timer Reaction



Conditions:
$V_{IN} > V_{RL}$ after power-up sequence

Fig. 5

Combined Voltage and Timer Reaction

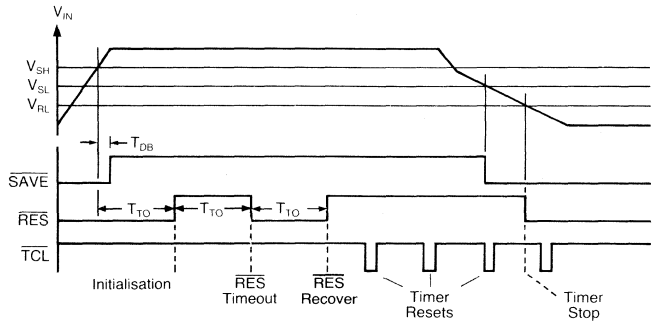


Fig. 6

Block Diagram

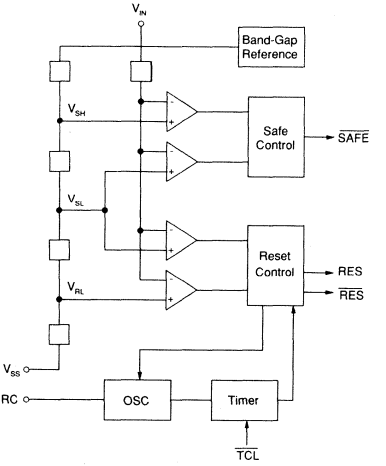


Fig. 7

Pin Description

Pin	Name	Function
1	V_{IN}	Voltage monitoring input
2	$\overline{TCL}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V_{SS}	GND terminal
5	RES	Reset output, open drain
6	$\overline{SAVE}$	Save output, open drain
7	$\overline{RES}$	Positive reset output, open drain
8	V_{DD}	Positive supply voltage

Table 6

Functional Description

Thresholds and outputs

The H 6061 has open-drain outputs and voltage thresholds on pin V_{IN} of typically 1.5V.

Internal voltage comparators

The voltage comparators detect the voltage applied to pin V_{IN} and compare it with thresholds V_{SH}, V_{SL} and V_{RL}. The H 6061 is designed for monitoring regulated DC voltages and has bandgap thresholds independent of V_{DD}. The reaction of the H 6061 to voltage changes on pin V_{IN} is given in Fig. 4. During powering-up, the outputs are active. After V_{IN} reaches the V_{SH} level, pin $\overline{SAVE}$ deactivates after a short debounce time T_{DB} to allow for fast ramp-ups. The initialisation time T_{TO} then passes before the two reset outputs go inactive. Thereafter, when the voltage on pin V_{IN} falls below the V_{SL} level, pin $\overline{SAVE}$ goes active low as a first warning. If V_{IN} then drops below the V_{RL} level, the reset signals go active and are guaranteed down to 1.6 V. The reset outputs react also to timeouts (see "Timer clearing"). Note that when the supply voltage V_{DD} is below the level V_{OFF} (about 2.2V), all outputs are in the active state for any allowed voltage of V_{IN}.

Voltage programming

The H 6061 was designed to give the best compromise in normal usage (see Table 3). Its voltage threshold can be programmed by an external resistor divider or a potentiometer to react at proportionally higher voltage levels (see Fig. 8 below).

Voltage Programming

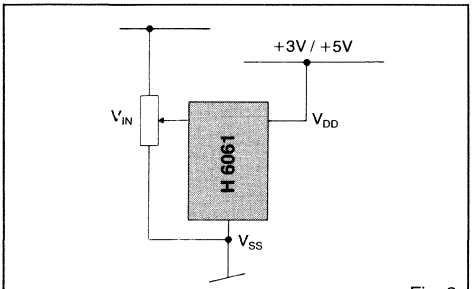


Fig. 8

Timer programming

A single timeout period T_{TO} is used for the initialisation reset duration and the watchdog timeout. With pin RC unconnected, the on-chip RC oscillator and divider chain give a timeout period T_{TO} of typically 100ms. A resistor to V_{DD} will shorten this time, and a capacitor to V_{SS} will lengthen it (see Fig. 11). An approximation for calculating trial values is given in milliseconds by the formula:

$$T_{TO} = \left[0.75 + \frac{(32 + C_1) \cdot 1.6}{4.8 + \frac{V_{DD} - 0.8}{R_1}} \right] \cdot 8.192$$

$R_{1\,min.} = 10\,k\Omega$, $C_{1\,max.} = 1\,\mu F$

If R_1 is in MΩ and C_1 in pF, T_{TO} will be in ms.

Choice of component values must be determined in practice. To have a square wave of period $2T_{TO}$, simply connect pin $\overline{TCL}$ to V_{DD} or V_{SS} and take the signal output from a reset pin.

Timer clearing

A negative edge or pulse at the $\overline{TCL}$ input longer than 150ns will clear the timer and deactivate the reset outputs under normal running conditions (see Fig. 3). $\overline{TCL}$ will however have no effect either when $V_{DD} < V_{OFF}$ or during the initialisation period before the deactivation of the reset pins.

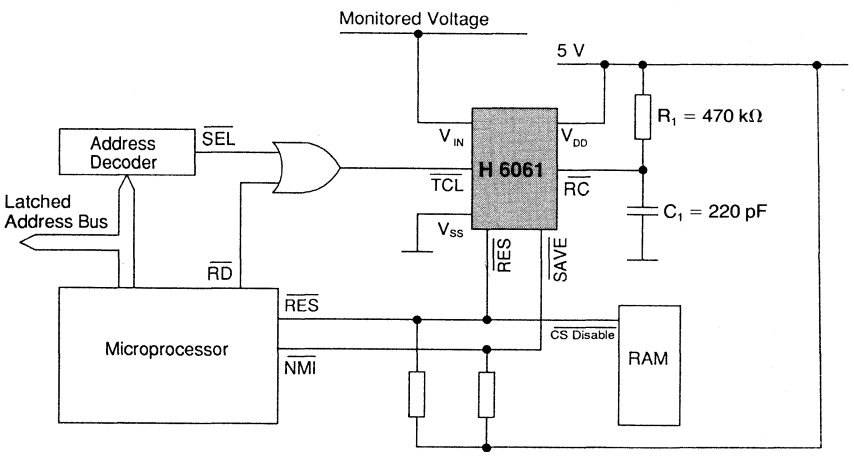
Combined voltage and timer action

In Fig. 6 is a typical sequence of power-up, watchdog run, and power-down. During initialisation the $\overline{SAVE}$ pin deactivates one debounce delay time T_{DB} after V_{IN} rises above V_{SH}, or when the power line V_{DD} rises above V_{ON}, whichever happens last. The reset pins only deactivate one timeout period T_{TO} afterwards to free the watchdog timer and end the initialisation. Note that either V_{IN} falling below V_{RL} threshold or V_{DD} below V_{ON} will cause an initialisation upon recovery. Following initialisation, the watchdog timer will time out after time T_{TO} unless at least one $\overline{TCL}$ pulse clears it. On timeout the reset pins reactivate for a further T_{TO} period before deactivating again for another try. A TCL pulse will deactivate any timeout reset, and another $\overline{TCL}$ pulse must follow within a time T_{TO} to keep reset inactive. If no $\overline{TCL}$ pulses come at all, the reset pins go square-wave. Power-down overrides all this however. A falling voltage on V_{IN} gives a warning $\overline{SAVE}$ = 0 signal at $V_{IN} = V_{SL}$ before activating the reset pins as soon as V_{IN} drops below V_{RL}. The H 6061 has fixed thresholds and low hysteresis for monitoring regulated DC lines. Additional protection is provided in case V_{DD} supply falls over about 10% below V_{ON} which thereupon activates all outputs at once.

6

Typical Applications

Microprocessor Watchdog with Voltage Monitor



$T_{TO} = \sim 250$ ms

Fig. 9

Selection of Watchdogs for Each Application

The H 6061 is designed for monitoring regulated DC voltages anywhere between 2.7 and 5.25V. Typically, it is used to monitor V_{DD} with pin V_{IN} tied to the midpoint of a voltage divider (see Fig. 8). This arrangement has the advantage of being able to trigger at selectable voltage limits, i.e. it can be used where the regulated voltage is below 5VDC.

Industrial Heavy-Duty utilisation

The H 6061 debounce protects against reactions due to fast-rise power lines, but absolute maximum ratings must be respected. With its flexibility of voltage programming and supply voltage the H 6061 can allow for voltage drops along supply lines, so it can be placed remotely, like on plug-in boards (see Fig. 9). The H 6061 is suitable for supply voltages down to 2.7VDC. As the H 6061 is designed to be sensitive to voltage changes, fast switching lines, like address/data bus lines should not be run between the V_{DD} and V_{SS} supply lines near the H 6061 without ground-plane shielding. Tracks from components to pin RC must be kept very short. Pin RC if left free should be shielded with a ground ring in noisy environments.

The H 6061 has only 40mV hysteresis specially for monitoring regulated DC. Pin V_{IN} must be protected from any significant mains ripple or RFI (see Fig. 10). It should be placed as near as possible to the point where voltage is to be monitored. Pin V_{IN} is protected by an internal resistor (nominal 15kΩ) against voltages in excess of V_{DD}. In some environments this may however pick up enough mains ripple or RFI to distort the voltage detection thresholds or even cause unwanted sporadic resets in the absence of adequate shielding or filtering on V_{IN}.

The H 6061 has sufficient immunity to ripple and interference on the V_{DD} supply line, but if it is important that a system meet severe criteria for injected spikes and RFI, then care must be taken to also decouple V_{DD} from these influences, as system protection must continue even under these conditions. With normal series voltage regulators, the regulated 5VDC output voltage follows the DC rough voltage within 1.5V on powering up. If the application has pin V_{IN} monitoring the DC rough, the internal inputs to the on-chip comparators will not rise above V_{DD} if the H 6061 is correctly programmed. With switched-mode power supplies however, the DC-rough voltage on power-up rises almost to its working level before the 5VDC line starts to ramp up. The H 6061 has been specially designed to work under these extreme conditions but care must be taken not to exceed absolute maximum ratings. In addition to the voltage monitoring on pin V_{IN}, a final protection is given by the H 6061 monitoring its own V_{DD} supply. If a system malfunction causes V_{DD} to fall below V_{OFF} even though pin V_{IN} stays high, then all outputs go active at once.

Combined Supply Monitor, Initialiser and Watchdog

V_{IN} shield [1] or decoupling [2] optional against interference

Nominal thresholds:
V_{SH} 2.84
V_{SL} 2.77
V_{RL} 2.70

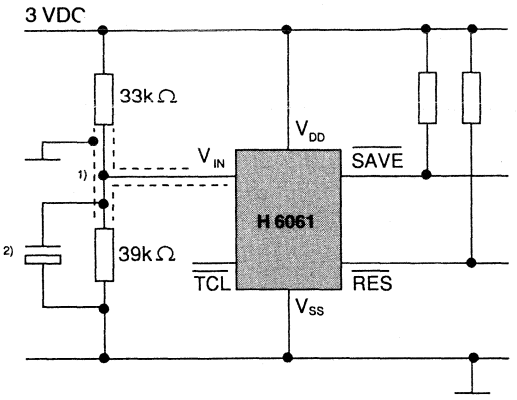
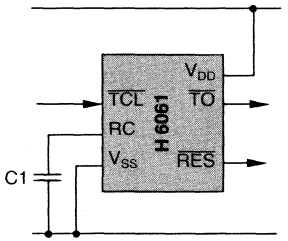
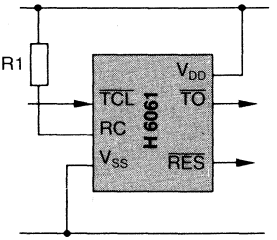


Fig. 10

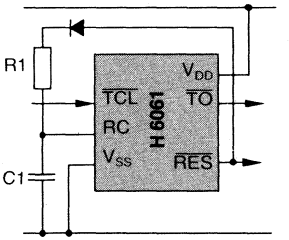
External Programming of RC Oscillator



C1 increases T_{TO}



R1 shortens T_{TO}



This circuit provides independent programming of both timeout period and power-on reset delay.

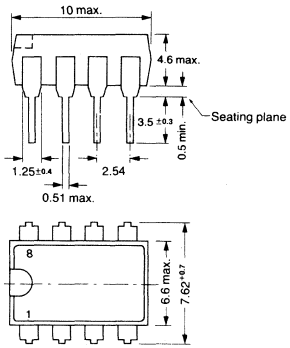
Note: if external components R1 and C1 are used, a tighter timeout period tolerance can be achieved.

Fig. 11

6

Package and Ordering Information

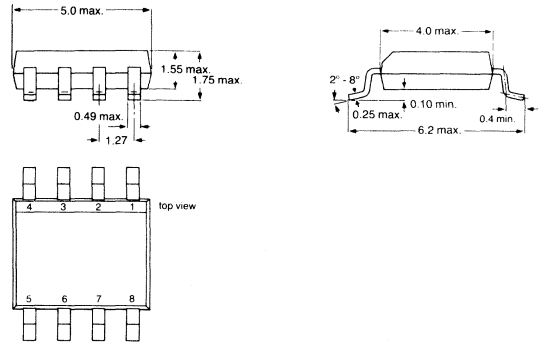
Dimensions of DIP8 Package



Dimensions in mm

Fig. 12

Dimensions of SO8 Package



Dimensions in mm

Fig. 13

Ordering Information

Industrial temperature range (−40 to +85°C)

Type	Package
H 6061 25 8P	DIP8
H 6061 25 8S	SO8

Extended temperature range (−40 to +125°C)

Type	Package
H 6061 25X 8P	DIP8*
H 6061 25X 8S	SO8*

* and chip form, on request

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Watchdog

Features

- Standby mode, maximum current 35 μA
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, reset threshold 1.17 V
- $\pm$ 1.5% threshold tolerance at 25°C
  $\pm$ 3% threshold tolerance for -40 to $+70$°C
- Programmable reset voltage monitoring
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy $\pm$ 10%
- System enable ($\overline{EN}$) output offers added security
- TTL / CMOS compatible
- -40 to $+70$°C temperature range
- DIP8 and SO8 packages

Description

The V 6130 offers a high level of integration by voltage monitoring and software monitoring in an 8 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products

Typical Operating Configuration

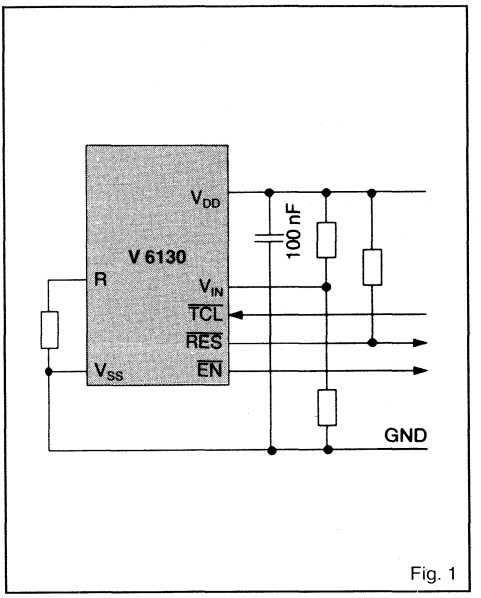


Fig. 1

Pin Assignment

DIP8 / SO8

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS} +7 V
Minimum voltage at V_{DD}	V_{DDmin}	V_{SS} −0.3 V
Max. voltage at any signal pin	V_{MAX}	V_{DD} +0.3 V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3 V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+70	°C
Supply voltage[1]	V_{DD}	3		5.5	V
$\overline{RES}$ & $\overline{EN}$ guaranteed[2]	V_{DD}	1.2			V
Comparator input voltage	V_{IN}	0		V_{DD}	V
RC-oscillator programming	R	10		1000	kΩ

Table 2

[1] A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

[2] $\overline{RES}$ must be pulled up externally to V_{DD} event if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

Electrical Characteristics

$3.0 \leq V_{DD} \leq 5.5$ V, C = 100 nF, $T_A = -40$ to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{DD}, V_{IN} = 0 V		22	35	μA
Supply current	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{DD}, O/Ps 1 MΩ to V_{DD}		55	100	μA
$\overline{RES}$ and $\overline{EN}$						
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$						
Output High Voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{DD} = 2.0 V, I_{OH} = −100 μA	1.8	1.9		V
	V_{OH}	V_{DD} = 1.2 V, I_{OH} = −30 μA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}		2.0		V_{DD}	V
Leakage current $\overline{TCL}$ input	I_{LI}	$V_{SS} \leq V_{TCL} \leq V_{DD}$		0.05	1	μA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference[1]	V_{REF}	T_A = 25°C	1.148	1.170	1.200	V
	V_{REF}	T_A = −20 to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis[1]	V_{HY}			2		mV

Table 3

[1] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

I_{SS} Standby versus Temperature at V_{DD} = 5.5 V

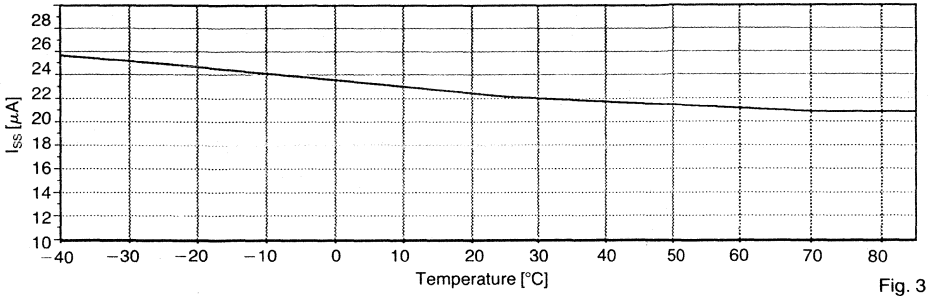


Fig. 3

Timing Characteristics

V_{DD} = 5.0 V ± 3%, C = 100 nF, T_A = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

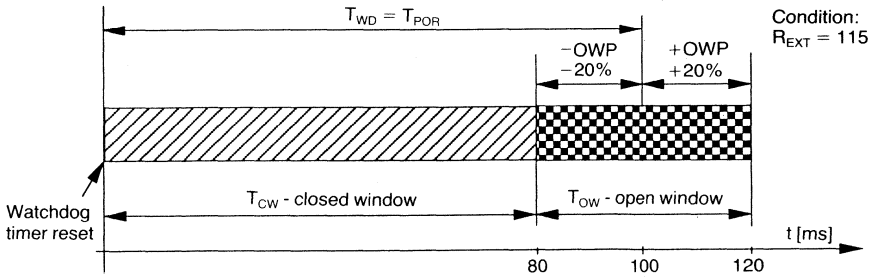


Fig. 4

Voltage Monitoring

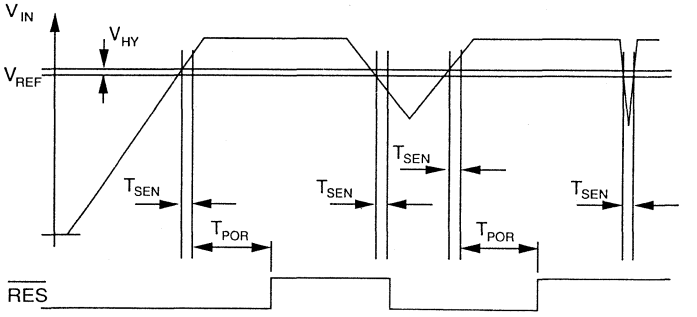


Fig. 5

Timer Reaction

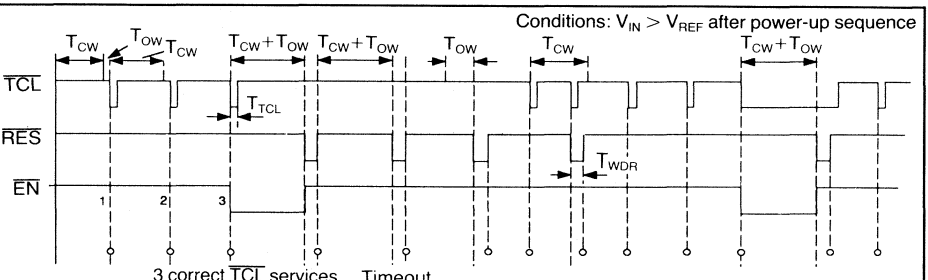


Fig. 6

Combined Voltage and Timer Reaction

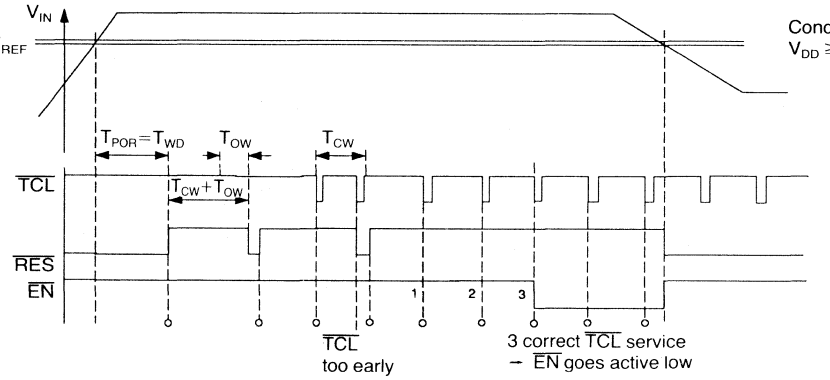


Fig. 7

Block Diagram

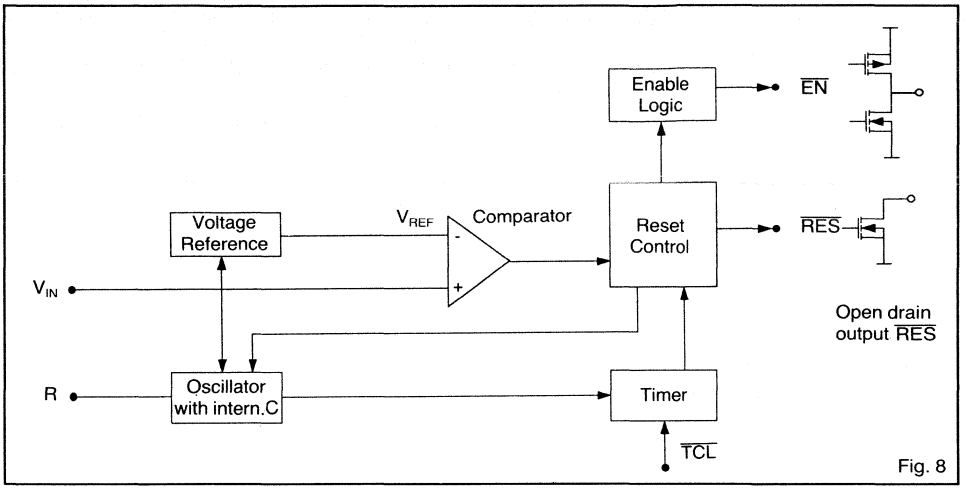


Fig. 8

Pin Description

Pin	Name	Function
1	$\overline{EN}$	Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{DD} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	NC	No connection
6	V_{DD}	Voltage supply
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 9. The user defines an external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5). When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Timer Programming

The on-chip oscillator needs an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9). It allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width (T_{WD}/40).

With R_{EXT} = 115 kΩ, the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP\ (T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP\ (T_{WD})$. The open window time is defined by $T_{CW} = 2 \times OWP\ (T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP =

± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms (T_{OW} = 2 x 0.2 (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically R_{EXT} x 0.8/ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 115 kΩ, then T_{WD} = 100 ms ± 10% and the useful open window limits for software are 90 to 100 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period, a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 6).

With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. If the software is stuck in a loop which includes the routine to clear the watchdog, a conventional watchdog will not reset the system even though the software is malfunctioning; the V 6130 will generate a system reset because the watchdog is cleared too quickly.

If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period (T_{CW} + T_{OW} + T_{WDR}). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 9).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 µs, overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable − $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V 6130 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

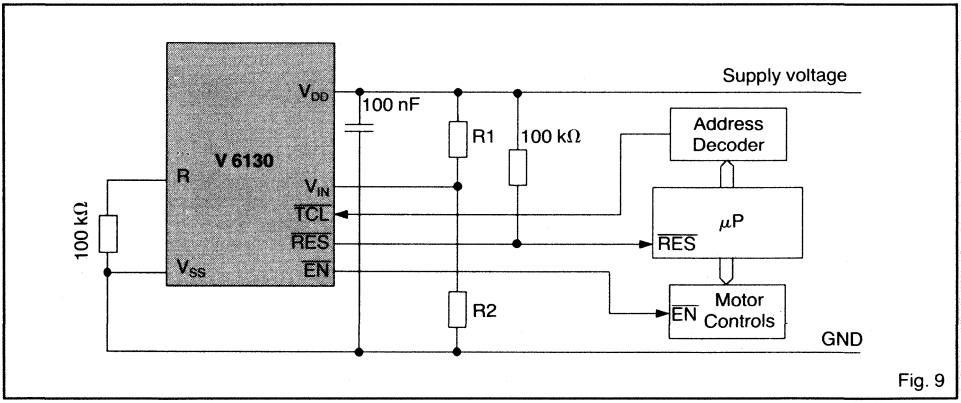


Fig. 9

T_{WD} versus Temperature at 5 V

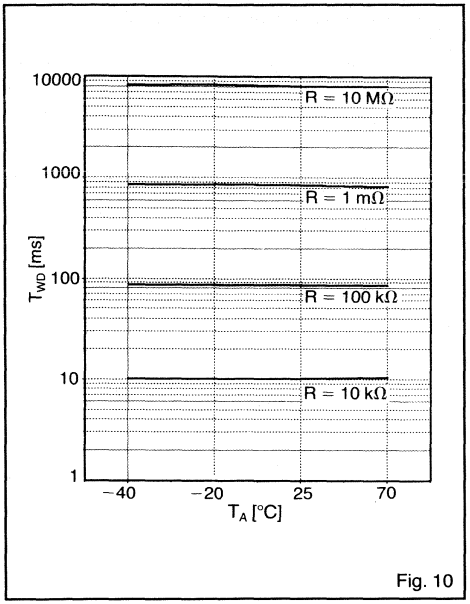


Fig. 10

T_{WD} versus R at 5 V

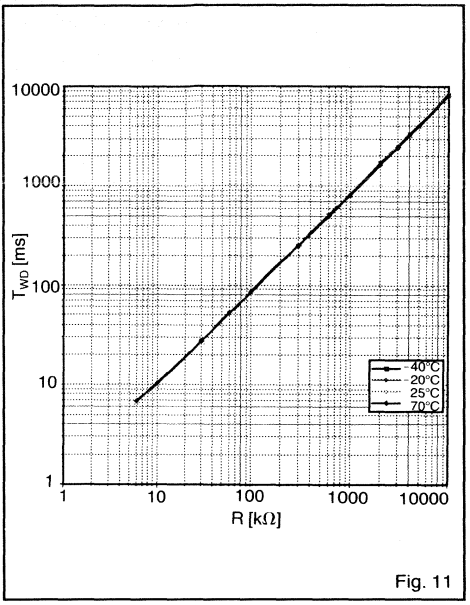


Fig. 11

T_{WD} versus V_{DD} at T_A = +25°C

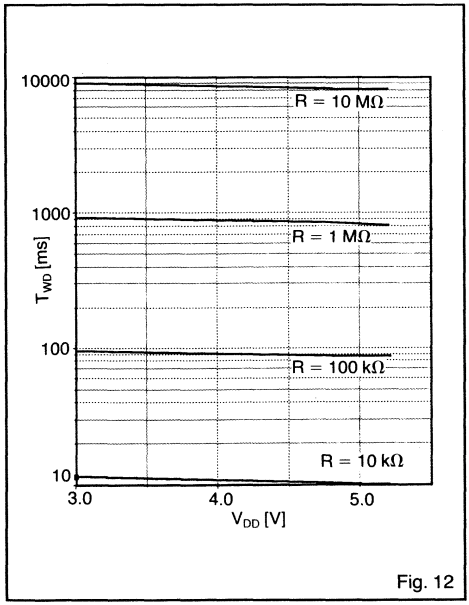


Fig. 12

T_{WD} versus R at T_A = +25°C

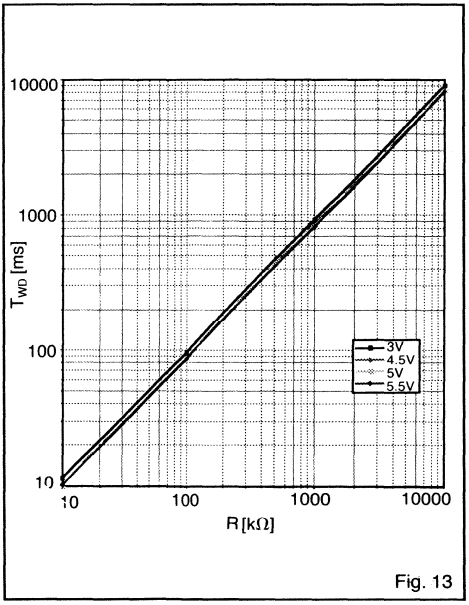


Fig. 13

T_{WD} versus R at $T_A = +25°C$

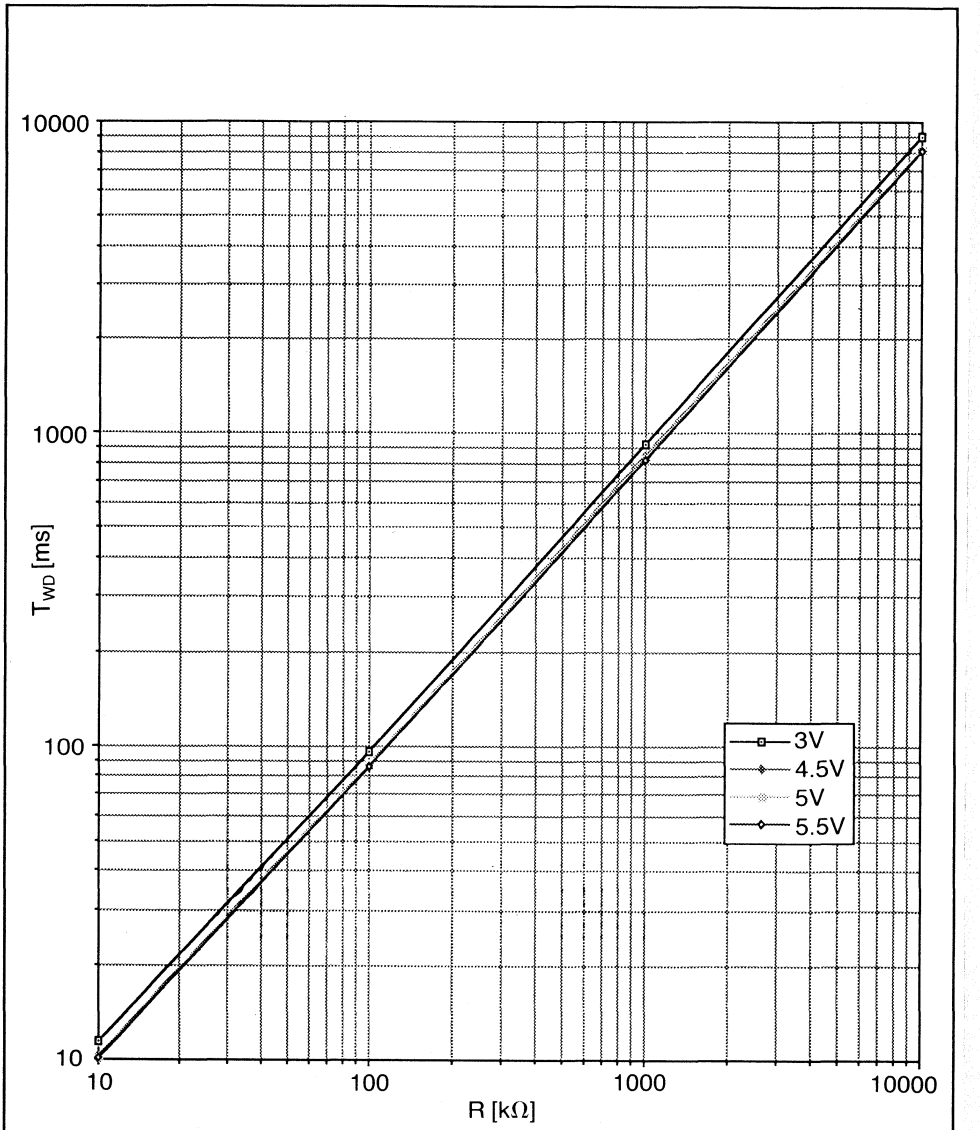


Fig. 14

T_{WD} versus V_{DD} at $T_A = +70°C$

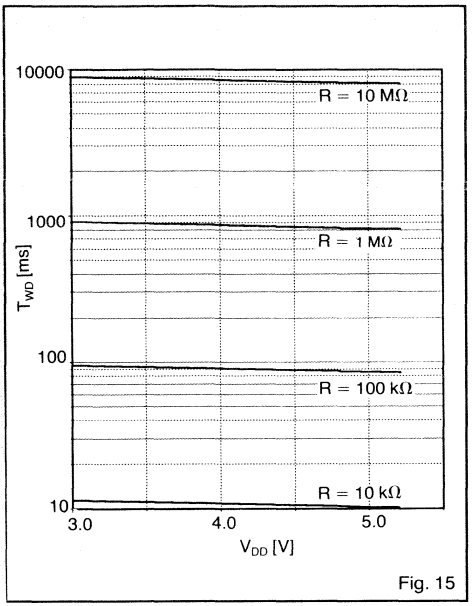


Fig. 15

T_{WD} versus R at $T_A = +70°C$

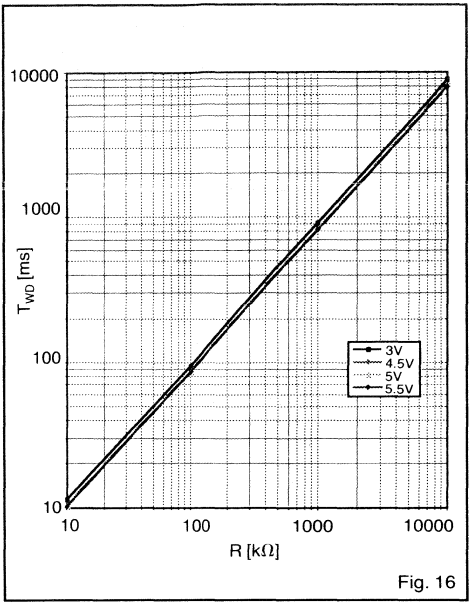


Fig. 16

T_{WD} versus V_{DD} at $T_A = -40°C$

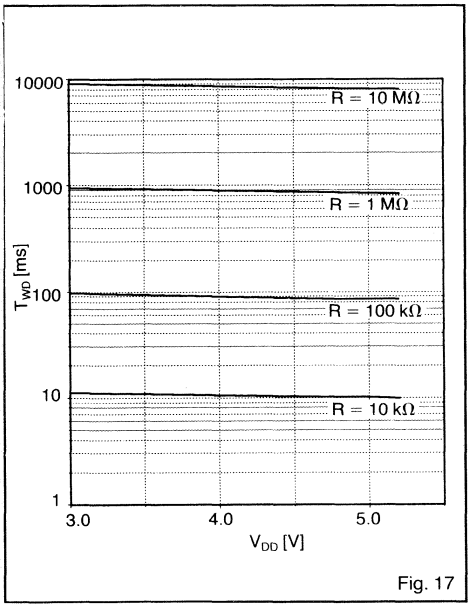


Fig. 17

T_{WD} versus R at $T_A = -40°C$

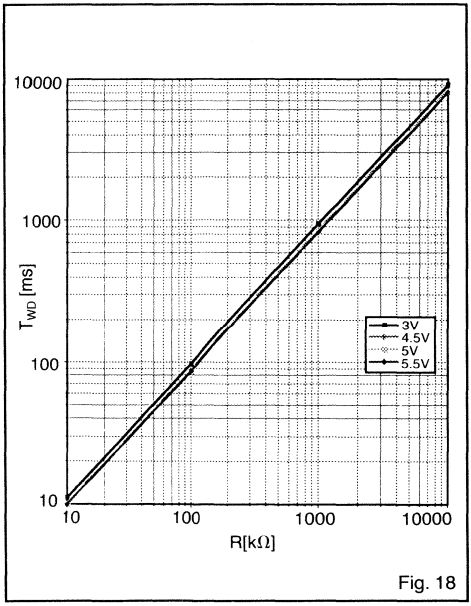
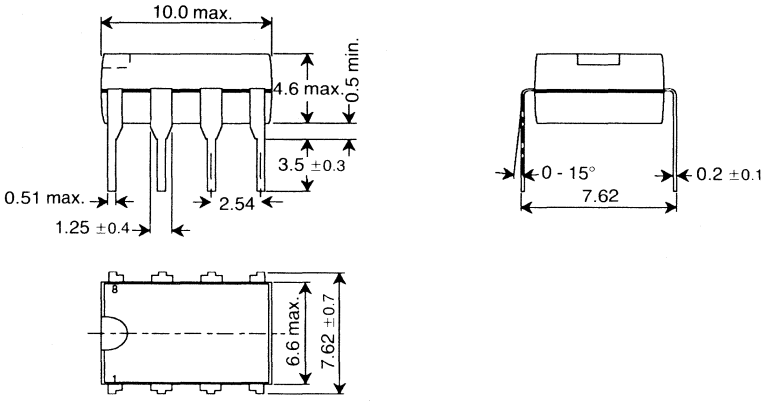


Fig. 18

Package and Ordering Information

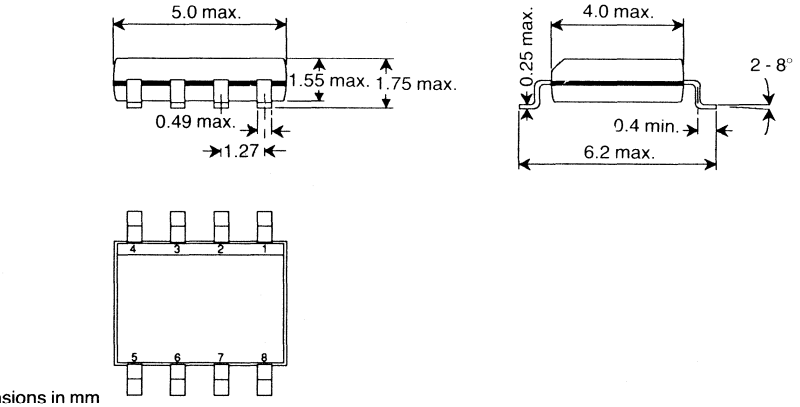
Dimensions of DIP8 Package



Dimensions in mm

Fig. 19

Dimensions of SO8 Package



Dimensions in mm

Fig. 20

Ordering Information

The V 6130 is available in the following packages:

Type	Package
V 6130 8P	DIP8
V 6130 8S	SO8

When ordering please specify complete part number.

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Watchdog

Features

- Standby mode, maximum current 35 μA
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, reset threshold 1.17 V
- $\pm$ 1.5% threshold tolerance at 25°C
  $\pm$ 3% threshold tolerance for -40 to $+70$°C
- Programmable reset voltage monitoring
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy $\pm$ 10%
- System enable ($\overline{EN}$) output offers added security
- 3 chip select feed-thru circuit controlled by $\overline{EN}$
- TTL / CMOS compatible
- -40 to $+70$°C temperature range
- DIP14 and SO14 packages

Description

The V 6133 offers a high level of integration by voltage monitoring and software monitoring in a 14 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products

Typical Operating Configuration

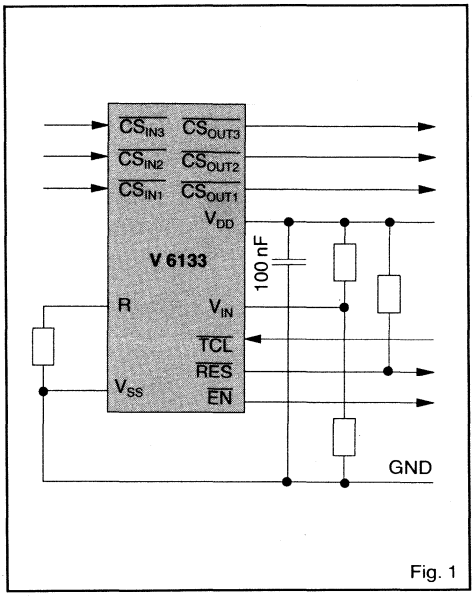


Fig. 1

Pin Assignment

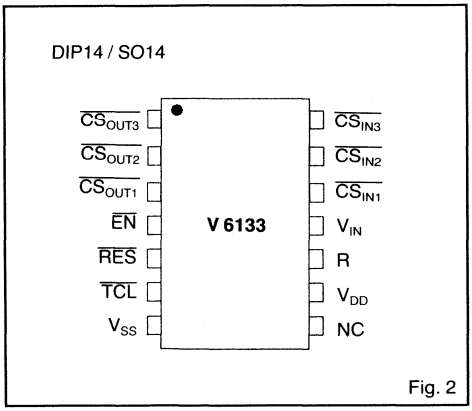


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	$V_{SS}+7$ V
Minimum voltage at V_{DD}	V_{DDmin}	$V_{SS}-0.3$ V
Max. voltage at any signal pin	V_{MAX}	$V_{DD}+0.3$ V
Min. voltage at any signal pin	V_{MIN}	$V_{SS}-0.3$ V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+70	°C
Supply voltage[1]	V_{DD}	3		5.5	V
$\overline{RES}$ & $\overline{EN}$ guaranteed[2]	V_{DD}	1.2			V
Comparator input voltage	V_{IN}	0		V_{DD}	V
RC-oscillator programming	R	10		1000	kΩ

Table 2

[1] A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

[2] $\overline{RES}$ must be pulled up externally to V_{DD} event if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

Electrical Characteristics

$3.0 \le V_{DD} \le 5.5$ V, C = 100 nF, $T_A = -40$ to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{DD}, V_{IN} = 0 V		22	35	μA
Supply current	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{DD} O/Ps 1 MΩ to V_{DD}		55	100	μA
$\overline{RES}$, $\overline{EN}$ and $\overline{CS_{OUT1/2/3}}$						
Output Low Voltage	V_{OL}	$V_{DD}=4.5$ V, $I_{OL}=20$ mA		0.4		V
	V_{OL}	$V_{DD}=4.5$ V, $I_{OL}=8$ mA		0.2	0.4	V
	V_{OL}	$V_{DD}=2.0$ V, $I_{OL}=4$ mA		0.2	0.4	V
	V_{OL}	$V_{DD}=1.2$ V, $I_{OL}=0.5$ mA		0.06	0.2	V
$\overline{EN}$ and $\overline{CS_{OUT1/2/3}}$						
Output High Voltage	V_{OH}	$V_{DD}=4.5$ V, $I_{OH}=-1$ mA	3.5	4.1		V
	V_{OH}	$V_{DD}=2.0$ V, $I_{OH}=-100$ μA	1.8	1.9		V
	V_{OH}	$V_{DD}=1.2$ V, $I_{OH}=-30$ μA	1.0	1.1		V
$\overline{TCL}$, V_{IN} and $\overline{CS_{IN1/2/3}}$						
$\overline{TCL}$ and $\overline{CS_{IN1/2/3}}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ and $\overline{CS_{IN1/2/3}}$ Input High Level	V_{IH}		2.0		V_{DD}	V
Leakage current TCL input	I_{LI}	$V_{SS} \le V_{TCL} \le V_{DD}$		0.05	1	μA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference[1]	V_{REF}	$T_A = 25$°C	1.148	1.170	1.200	V
	V_{REF}	$T_A = -20$ to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis[1]	V_{HY}			2		mV

Table 3

[1] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 6).

I_{SS} Standby versus Temperature at V_{DD} = 5.5 V

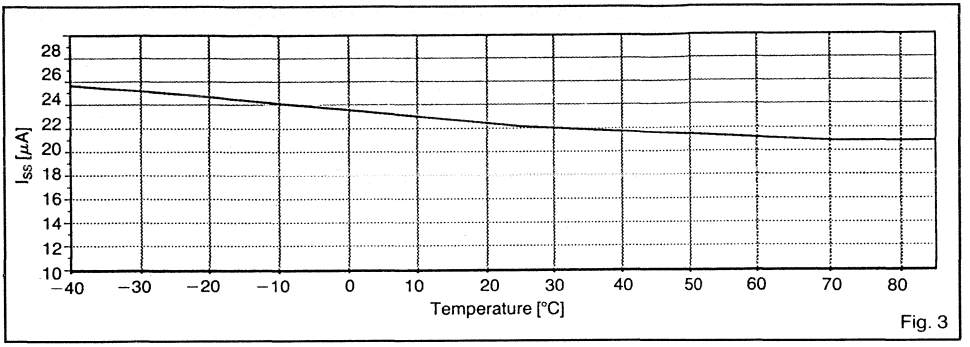


Fig. 3

Timing Characteristics

V_{DD} = 5.0 V ± 3%, C = 100 nF, T_A = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at rising edge	T_{CSH}			125	200	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at falling edge	T_{CSL}			75	150	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

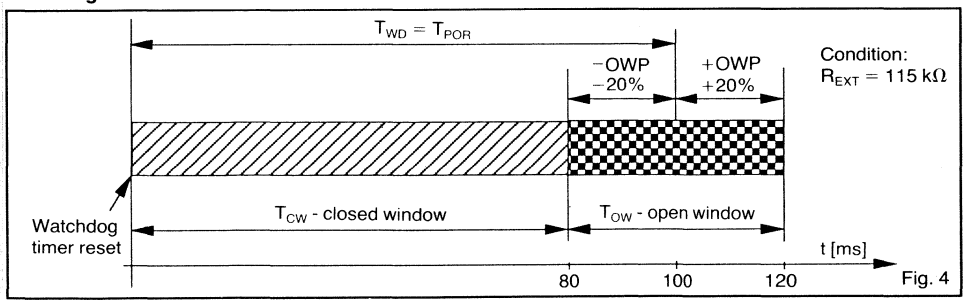


Fig. 4

Chip Select

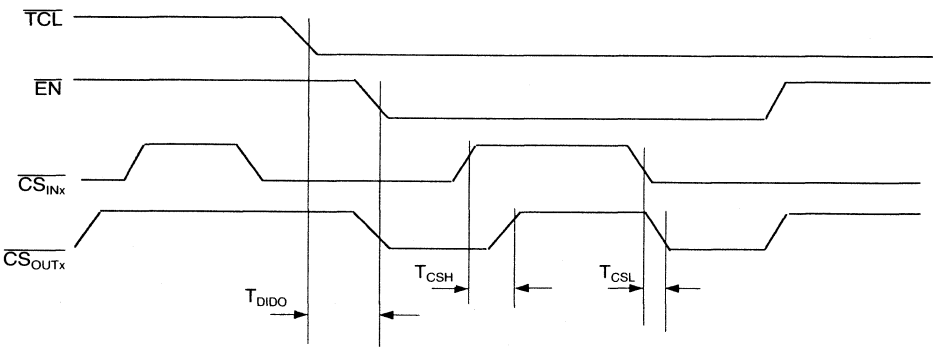


Fig. 5

Voltage Monitoring

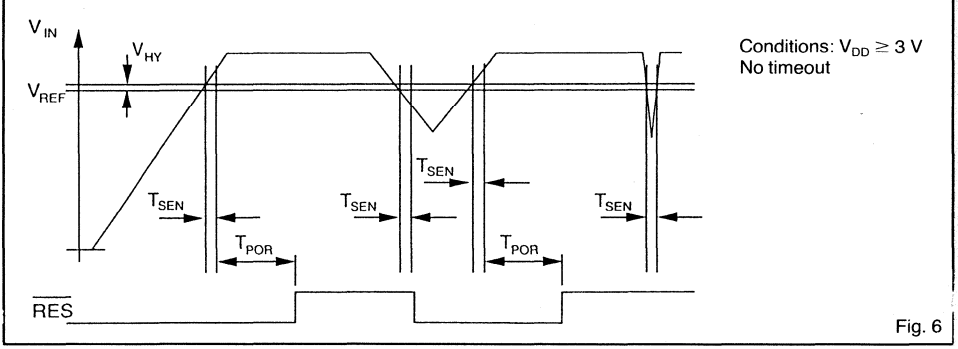


Fig. 6

Timer Reaction

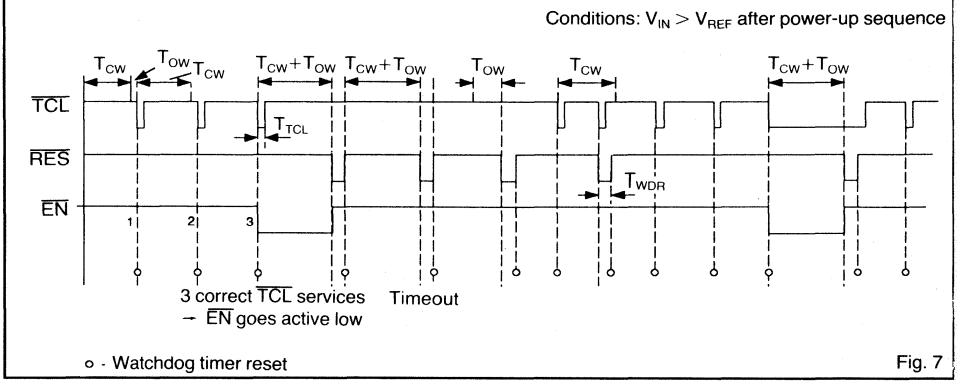


Fig. 7

Combined Voltage and Timer Reaction

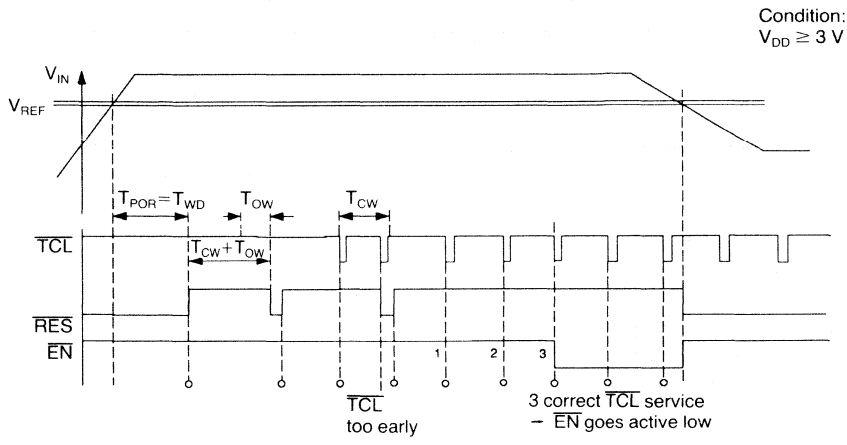


Fig. 8

Block Diagram

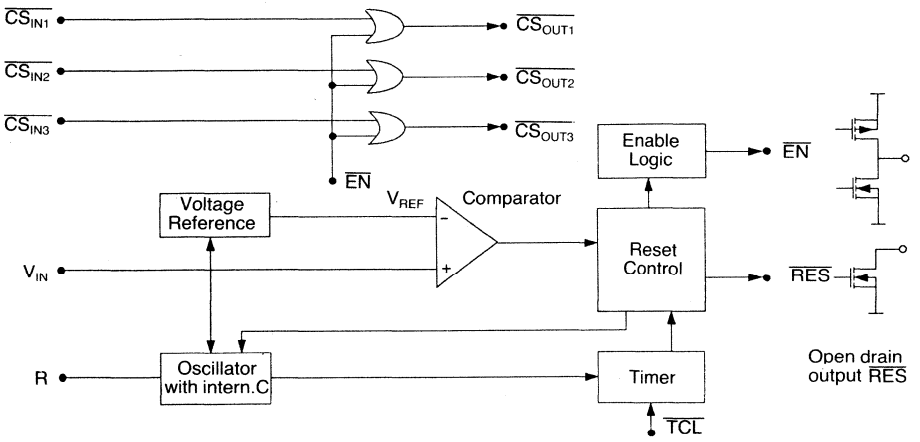


Fig. 9

Pin Description

Pin	Name	Function
1	$\overline{CS_{OUT3}}$	Push-pull active low chip select output 3
2	$\overline{CS_{OUT2}}$	Push-pull active low chip select output 2
3	$\overline{CS_{OUT1}}$	Push-pull active low chip select output 1
4	$\overline{EN}$	Push-pull active low enable output
5	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{DD} even if unused
6	$\overline{TCL}$	Watchdog timer clear input signal
7	V_{SS}	GND terminal
8	NC	No connection
9	V_{DD}	Voltage supply
10	R	R_{EXT} input for RC oscillator tuning
11	V_{IN}	Voltage comparator input
12	$\overline{CS_{IN1}}$	Chip select input 1
13	$\overline{CS_{IN2}}$	Chip select input 2
14	$\overline{CS_{IN3}}$	Chip select input 3

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 10. The user defines an external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 6). When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Timer Programming

The on-chip oscillator needs an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 10). It allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 115 kΩ, the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP\ (T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP\ (T_{WD})$. The open window time is defined by $T_{CW} = 2 \times OWP\ (T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms − 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically $R_{EXT} \times 0.87$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 115 kΩ, then T_{WD} = 100 ms ± 10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period, a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 7).

With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. If the software is stuck in a loop which includes the routine to clear the watchdog, conventional watchdog will not reset the system even though the software is malfunctioning; the V 6133 will generate a system reset because the watchdog is cleared too quickly.

If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 10).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 8. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs, overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable – $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V 6133 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly re-started after a reset condition).

Typical Application

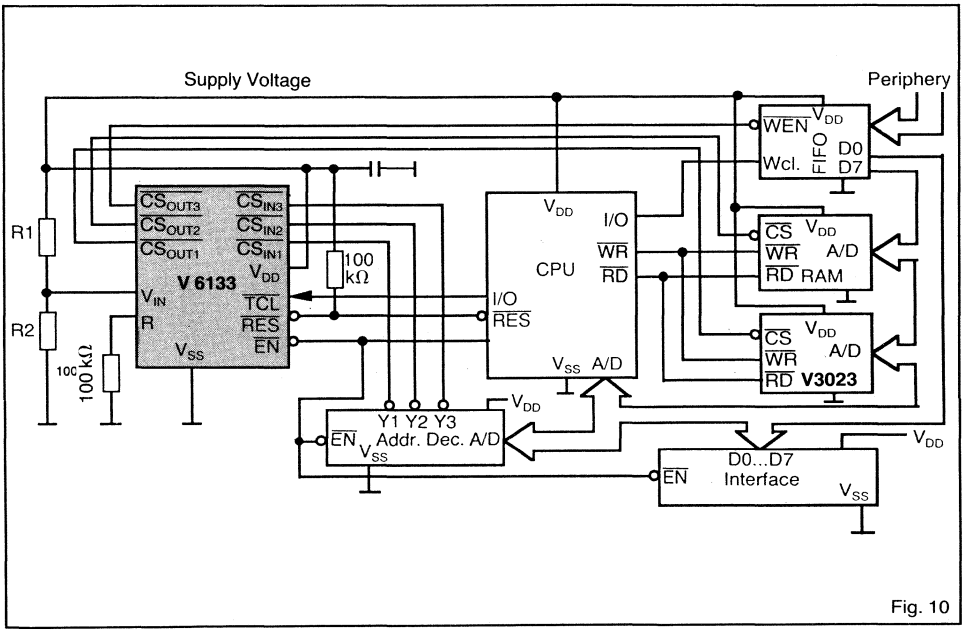


Fig. 10

T_{WD} versus Temperature at 5 V

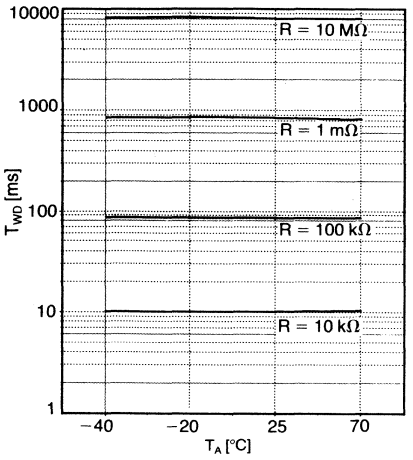


Fig. 11

T_{WD} versus R at 5 V

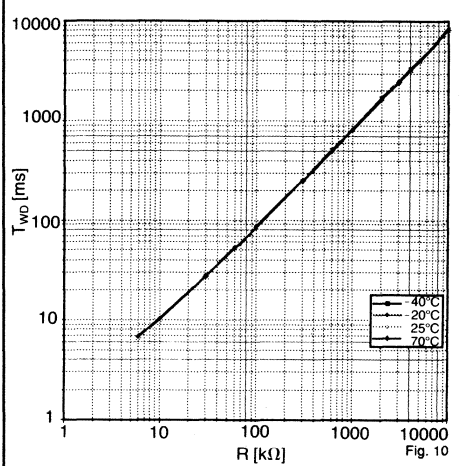


Fig. 10

Fig. 12

T_{WD} versus V_{DD} at T_A = +25°C

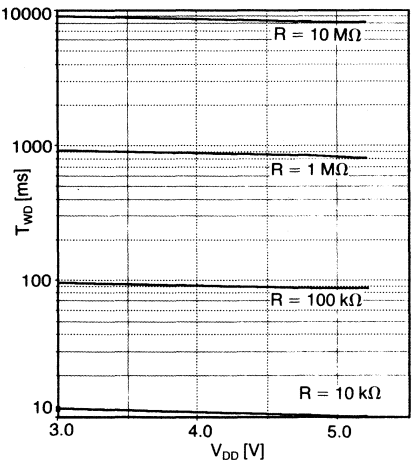


Fig. 13

T_{WD} versus R at T_A = +25°C

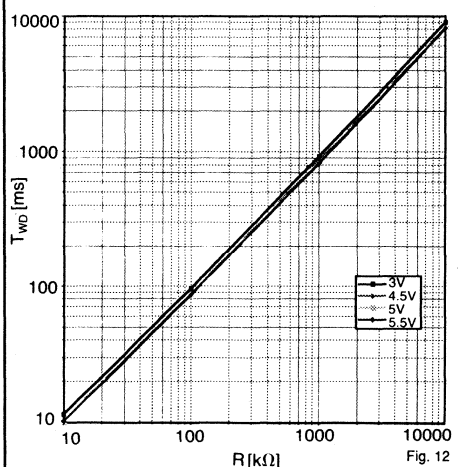


Fig. 12

Fig. 14

T_{WD} versus R at $T_A = +25°C$

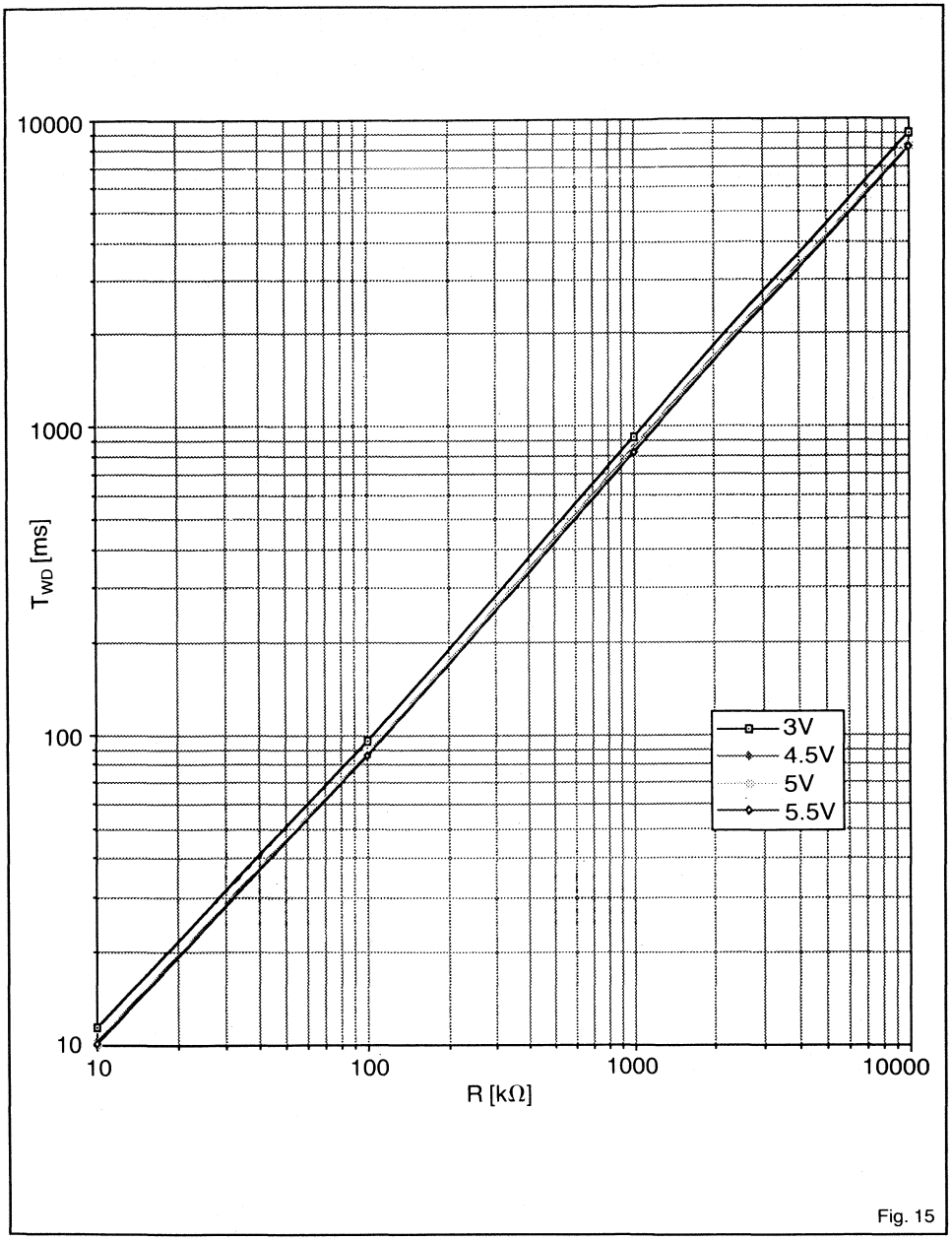


Fig. 15

T_{WD} versus V_{DD} at $T_A = +70°C$

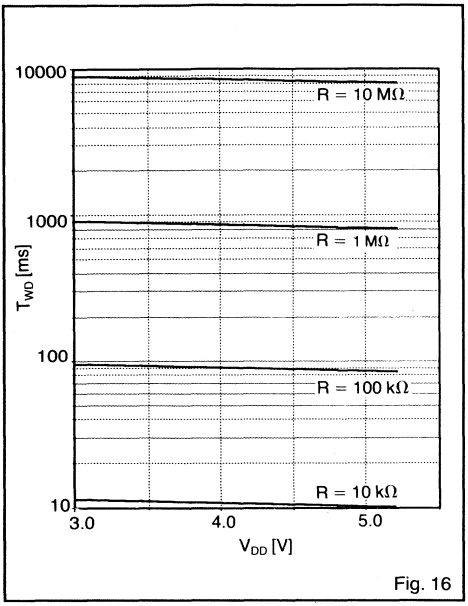


Fig. 16

T_{WD} versus R at $T_A = +70°C$

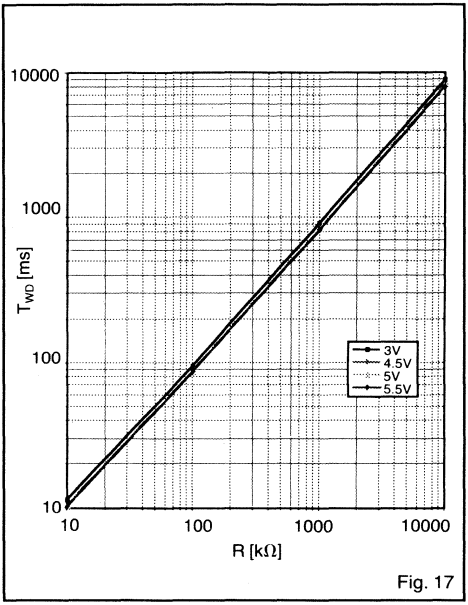


Fig. 17

T_{WD} versus V_{DD} at $T_A = -40°C$

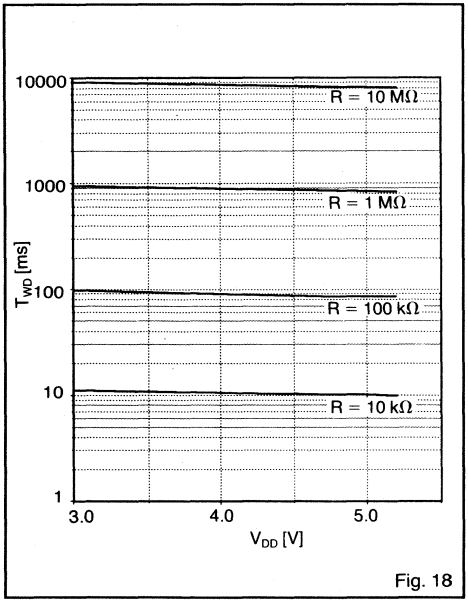


Fig. 18

T_{WD} versus R at $T_A = -40°C$

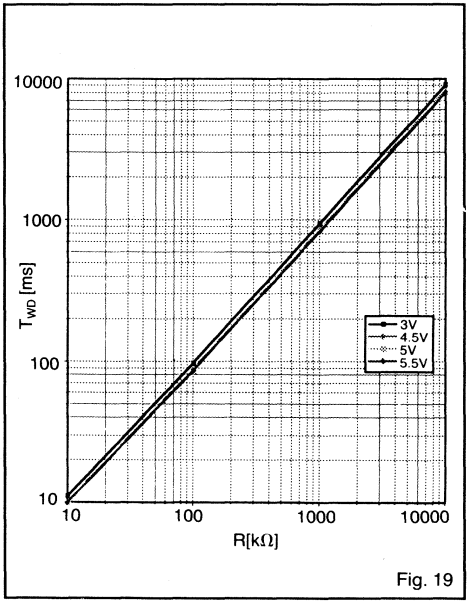
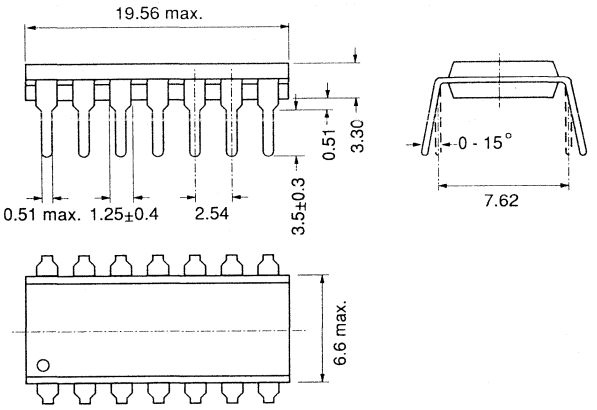


Fig. 19

Package and Ordering Information

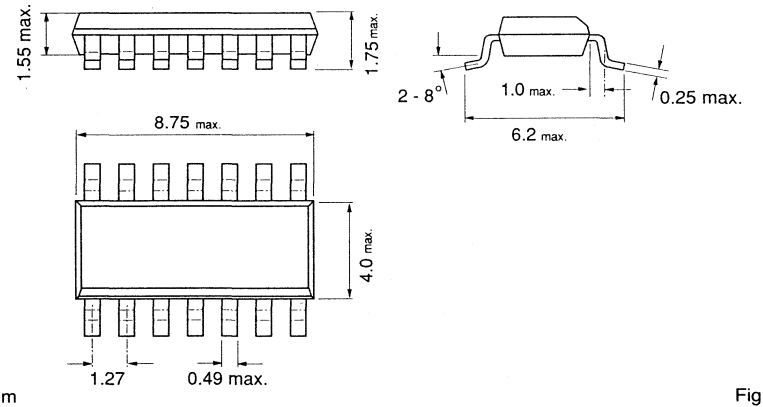
Dimensions of DIP14 Package



Dimensions in mm

Fig. 20

Dimensions of SO14 Package



Dimensions in mm

Fig. 21

Ordering Information

The V 6133 is available in the following packages:

Type	Package
V 6133 14P	DIP14
V 6133 14S	SO14

When ordering please specify complete part number.

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Watchdog

Features

- Standby mode, maximum current 45 μA
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, reset threshold 1.5 V
- Programmable reset voltage monitoring
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ± 10%
- System enable ($\overline{EN}$) output offers added security
- TTL / CMOS compatible
- −40 to +85°C temperature range
- On request, extended temperature range −40 to +125°C
- DIP8 and SO8 packages

Description

The V 6150 offers a high level of integration by voltage monitoring and software monitoring in an 8 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.5 V reference. The power-on reset function is initialized after V_{IN} reaches 1.5 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.5 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Automotive systems
- Cellular telephones
- Security systems
- Battery powered products

Typical Operating Configuration

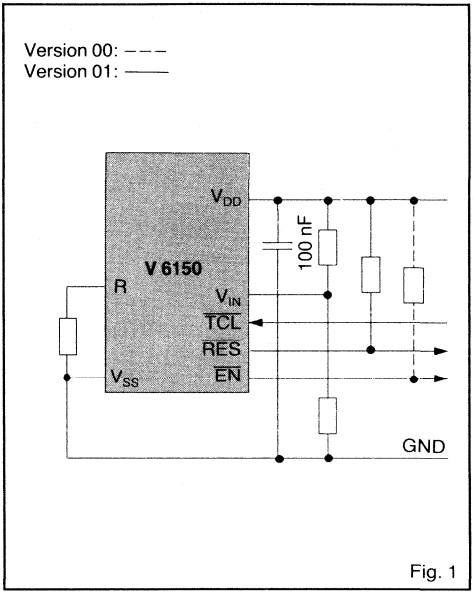


Fig. 1

Pin Assignment

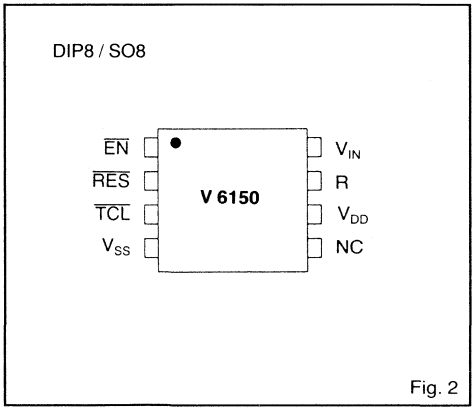


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	$V_{SS}+7$ V
Minimum voltage at V_{DD}	V_{DDmin}	$V_{SS}-0.3$ V
Max. voltage at any signal pin	V_{MAX}	$V_{DD}+0.3$ V
Min. voltage at any signal pin	V_{MIN}	$V_{SS}-0.3$ V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+125	°C
Supply voltage[1]	V_{DD}	3		5.5	V
$\overline{RES}$ & $\overline{EN}$ guaranteed[2]	V_{DD}	1.2			V
Comparator input voltage	V_{IN}	0		V_{DD}	V
RC-oscillator programming	R	10		1000	kΩ

Table 2

[1] A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

[2] $\overline{RES}$ and $\overline{EN}$ ($\overline{EN}$ only for version 00) must be pulled up externally to V_{DD} event if they are unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

Electrical Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$, C = 100 nF, $T_A = -40$ to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{DD}, $V_{IN} = 0$ V		23	45	µA
Supply current	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{DD}, O/Ps 1 MΩ to V_{DD}		75	120	µA
$\overline{RES}$ (vers. 00,01) **and $\overline{EN}$** (vers. 00)						
Output Low Voltage	V_{OL}	$V_{DD} = 4.5$ V, $I_{OL} = 20$ mA		0.4		V
	V_{OL}	$V_{DD} = 4.5$ V, $I_{OL} = 8$ mA		0.2	0.4	V
	V_{OL}	$V_{DD} = 2.0$ V, $I_{OL} = 4$ mA		0.2	0.4	V
	V_{OL}	$V_{DD} = 1.2$ V, $I_{OL} = 0.5$ mA		0.06	0.2	V
$\overline{EN}$ (vers. 01)						
Output High Voltage	V_{OH}	$V_{DD} = 4.5$ V, $I_{OH} = -1$ mA	3.5	4.1		V
	V_{OH}	$V_{DD} = 2.0$ V, $I_{OH} = -100$ µA	1.8	1.9		V
	V_{OH}	$V_{DD} = 1.2$ V, $I_{OH} = -30$ µA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}		2.0		V_{DD}	V
Leakage current $\overline{TCL}$ input	I_{LI}	$V_{SS} \le V_{TCL} \le V_{DD}$		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference[1]	V_{REF}	$V_{DD} = 5$ V, $T_A = 25$°C	1.474	1.52	1.566	V
	V_{REF}	$V_{DD} = 5$ V	1.436		1.620	V
	V_{REF}	$V_{DD} = 5$ V, $-40°C \le T_A \le 125°C$	1.420		1.620	V
Comparator hysteresis[1]	V_{HY}			2		mV

Table 3

[1] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

I_{SS} Standby versus Temperature at V_{DD} = 5 V

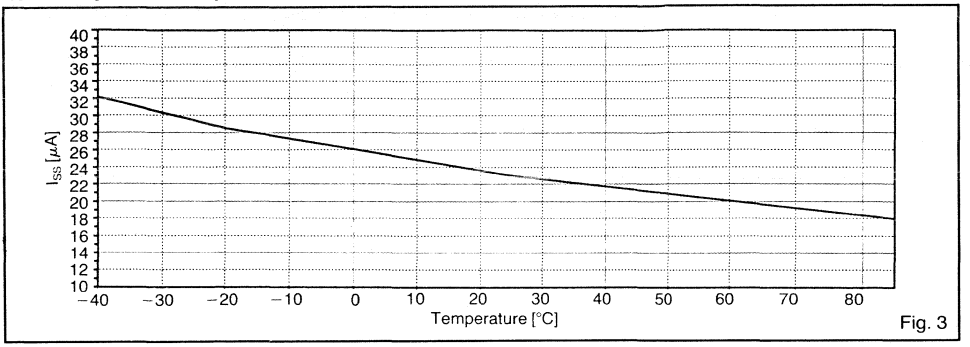


Fig. 3

Timing Characteristics

V_{DD} = 5.0 V ± 3%, C = 100 nF, T_A = −40 to +125°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 123 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 123 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 123 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 123 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 123 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

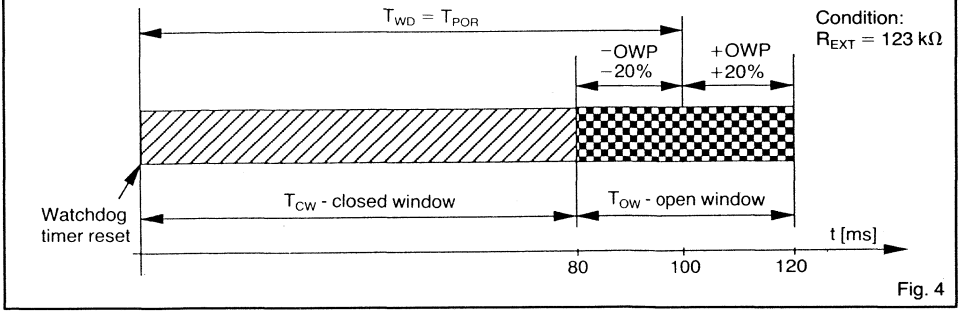


Fig. 4

Voltage Monitoring

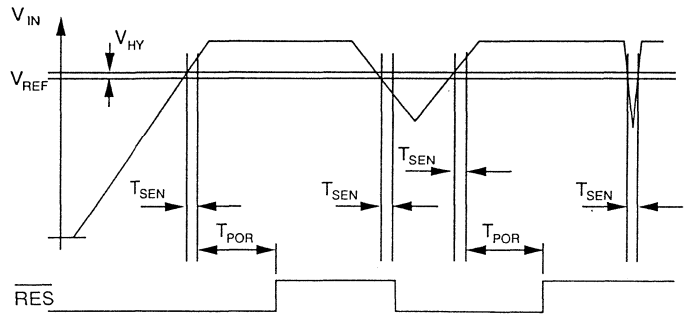


Fig. 5

Timer Reaction

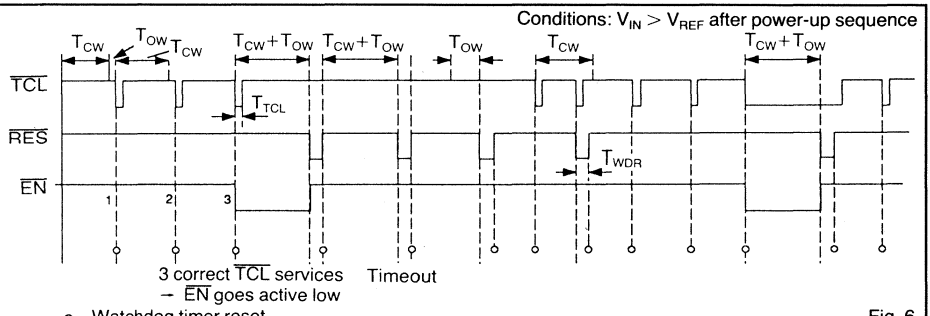


Fig. 6

Combined Voltage and Timer Reaction

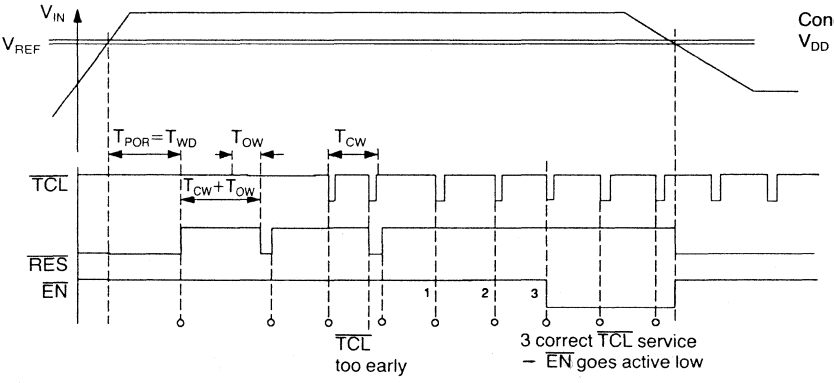


Fig. 7

Block Diagram

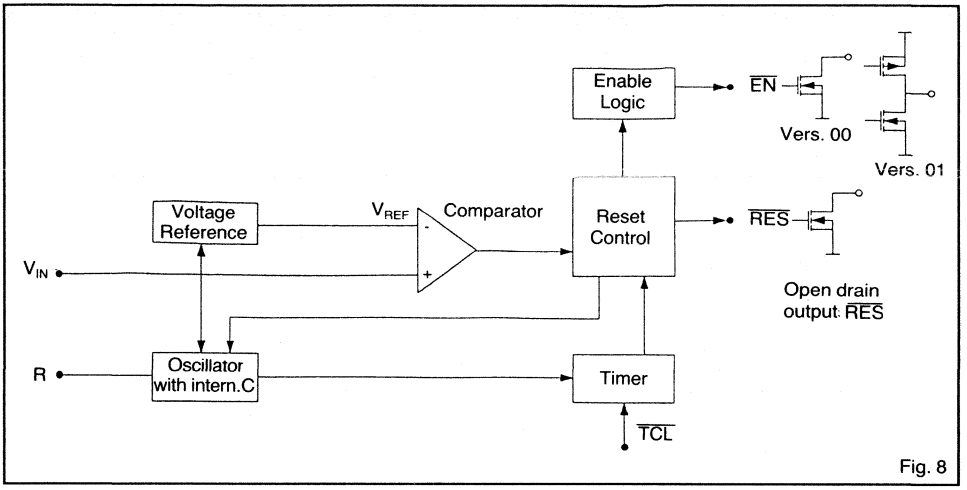


Fig. 8

6

Pin Description

Pin	Name	Function
1	$\overline{EN}$	**Vers. 00:** Open drain active low enable output. EN must be pulled up to V_{DD} even if unused. **Vers. 01:** Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{DD} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	NC	No connection
6	V_{DD}	Voltage supply
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 9. The user defines the external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.52 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5). When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 123 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 µs.

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 123 kΩ, the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP\ (T_{WD})$.

The open window starts after the closed time window finishes and lasts till T_{WD} + OWP (T_{WD}). The open window time is defined by T_{OW} = 2 x OWP (T_{WD}).
For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms (T_{OW} = 2 x 0.2 (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: R_{EXT} x 0.75 to R_{EXT} x 0.85 where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 123 kΩ, then T_{WD} = 100 ms ± 10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period, a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 6).
With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. If the software is stuck in a loop which includes the routine to clear the watchdog, then a conventional watchdog would not make a system reset even though the software is malfunctioning; the V 6150 would make a system reset because the watchdog would be cleared too quickly.
If no $\overline{TCL}$ pulse is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period (T_{CW} + T_{OW} + T_{WDR}). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 9).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 µs, overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable − $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.
A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V 6150 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).
For the version 00 the $\overline{EN}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 9).

Typical Application

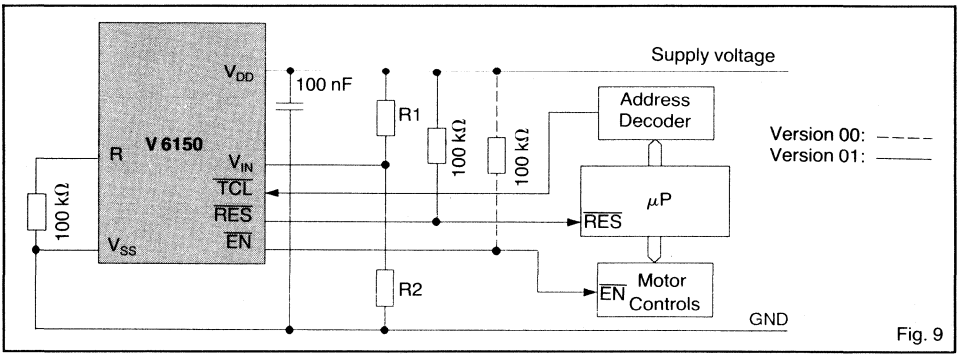


Fig. 9

T_{WD} versus Temperature at 5 V

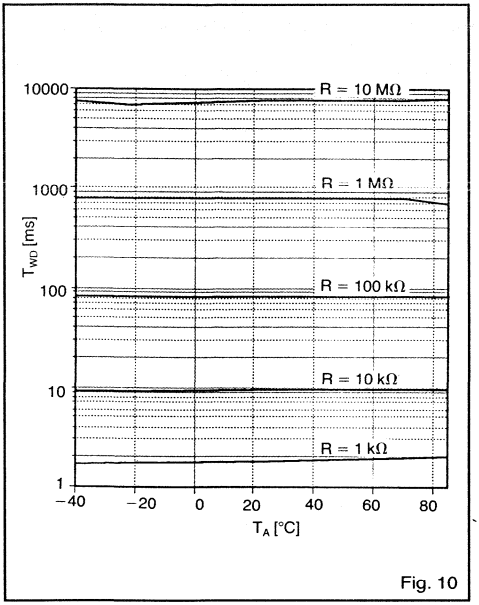


Fig. 10

T_{WD} versus R at 5 V

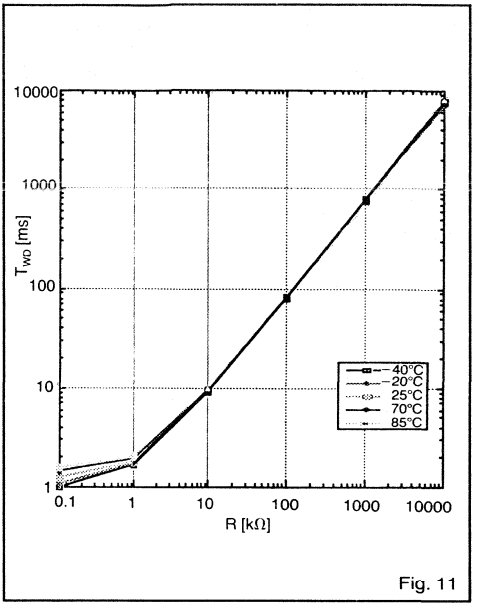


Fig. 11

T_{WD} versus V_{DD} at T_A = +25°C

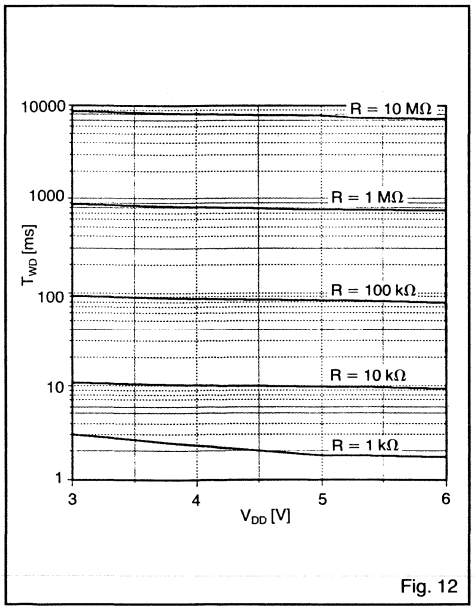


Fig. 12

T_{WD} versus R at T_A = +25°C

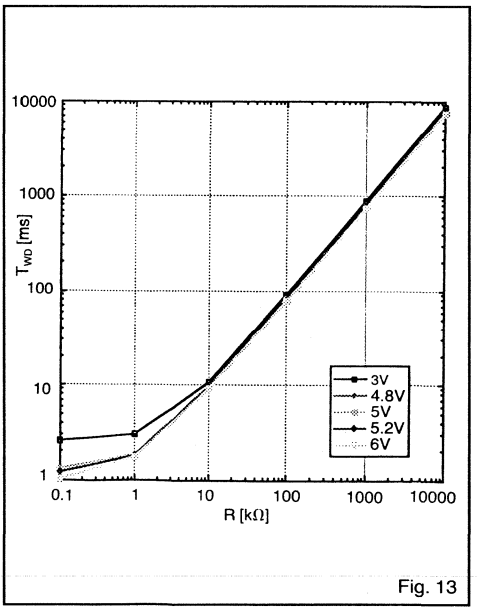


Fig. 13

6

T_{WD} versus R at $T_A = +25°C$

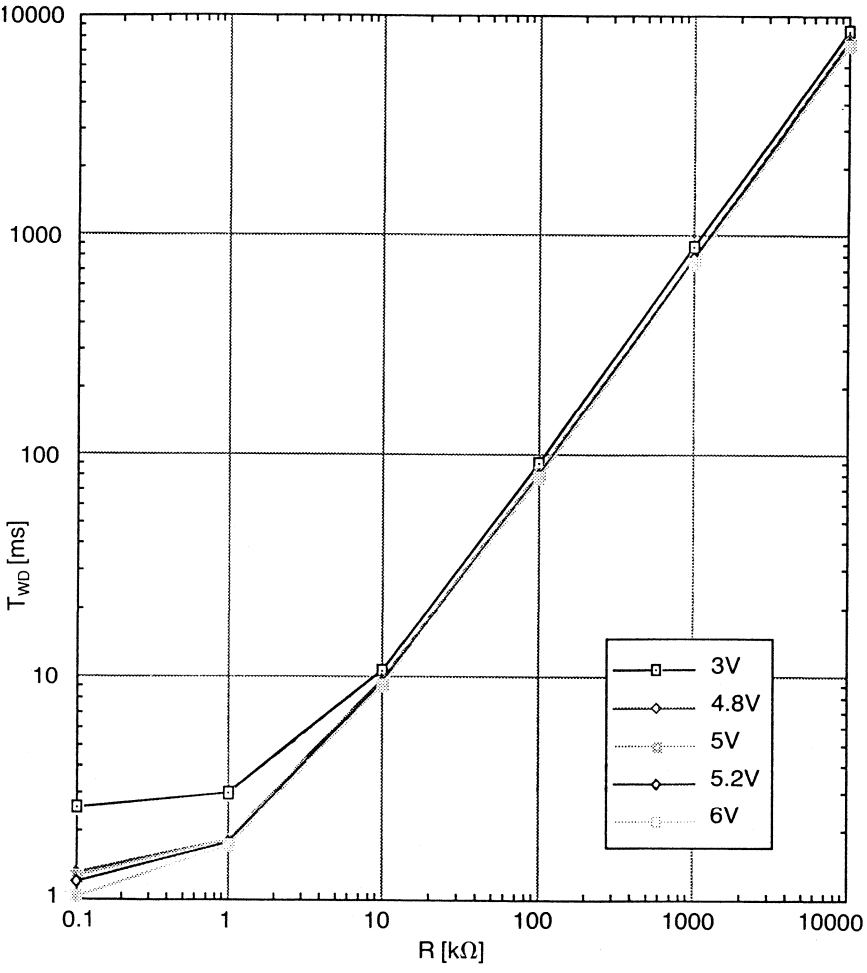


Fig. 14

T_{WD} versus V_{DD} at $T_A = +85°C$

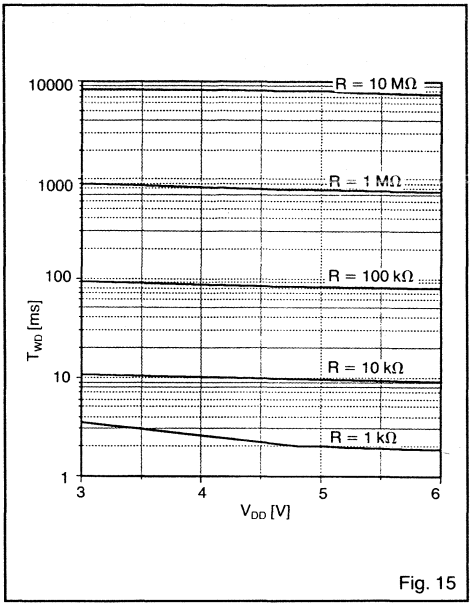


Fig. 15

T_{WD} versus R at $T_A = +85°C$

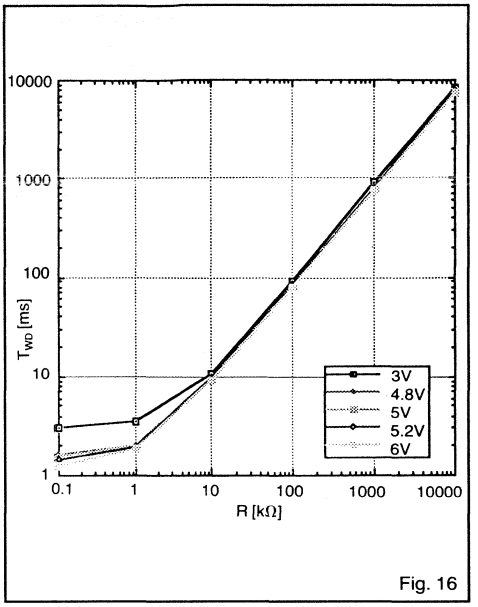


Fig. 16

T_{WD} versus V_{DD} at $T_A = -40°C$

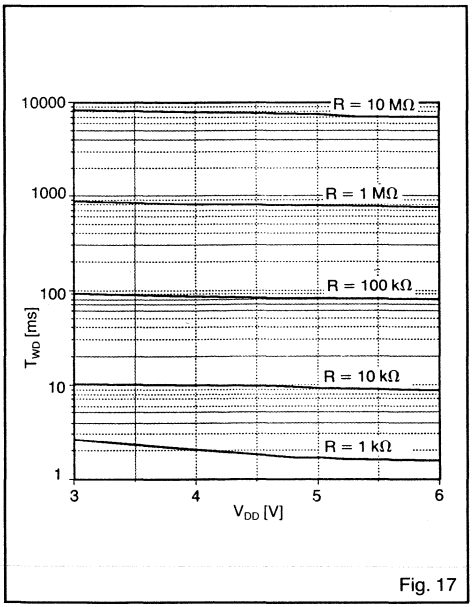


Fig. 17

T_{WD} versus R at $T_A = -40°C$

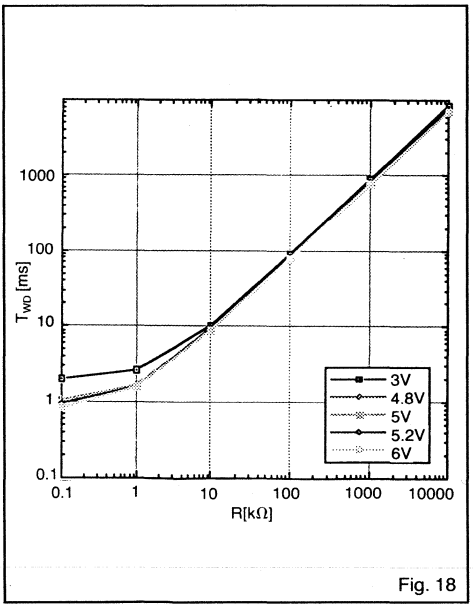
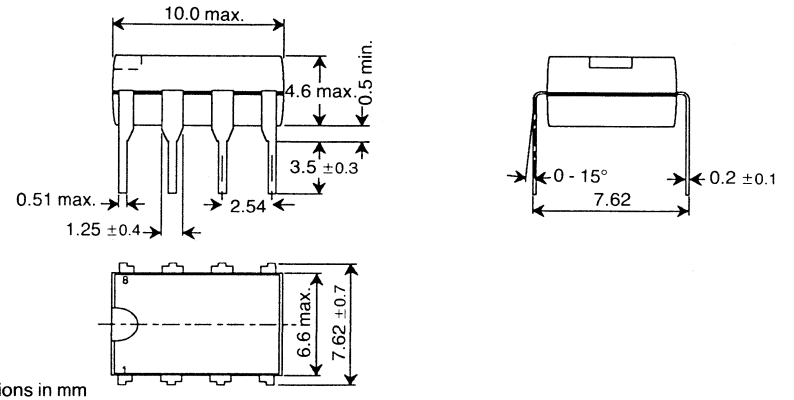


Fig. 18

6

Package and Ordering Information

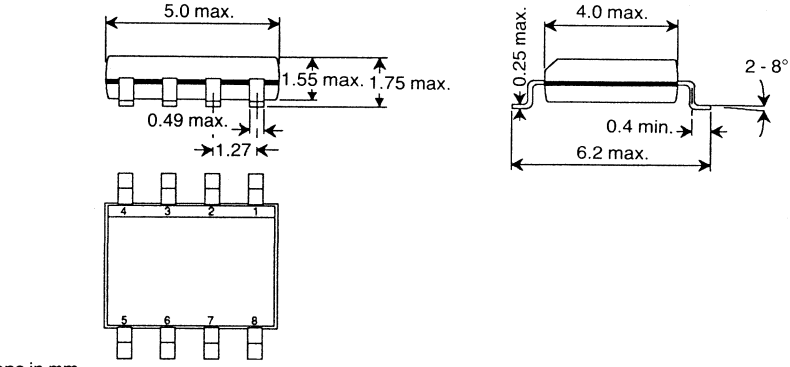
Dimensions of DIP8 Package



Dimensions in mm

Fig. 19

Dimensions of SO8 Package



Dimensions in mm

Fig. 20

Ordering Information

The V 6150 is available in the following packages:

Industrial temperature range (−40°C to +85°C)

Type[1]	Package
V 6150 nn 8P	DIP8
V 6150 nn 8S	SO8

Extended temperature range (−40°C to +125°C)

Type[1]	Package
V 6150 nn X 8P	DIP8*
V 6150 nn X 8S	SO8*

When ordering please specify complete part number.

Marking on package:

Package	Marking[1]
DIP8	V 6150 nn
SO8	6150 nn

[1] nn stands for the versions 00*, 01

* on request

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Watchdog

Features

- Standby mode, maximum current 35 μA
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, reset threshold 1.17 V
- $\pm$ 1.5% threshold tolerance at 25°C $\pm$ 3% threshold tolerance for -40 to $+70$°C
- Programmable reset voltage monitoring
- Voltage window, high threshold 5.9 V
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy $\pm$ 10%
- System enable ($\overline{EN}$) output offers added security
- TTL / CMOS compatible
- -40 to $+70$°C temperature range
- DIP8 and SO8 packages

Description

The V 6170 offers a high level of integration by voltage monitoring and software monitoring in an 8 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V or when V_{DD} is higher than 5.9 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products

Typical Operating Configuration

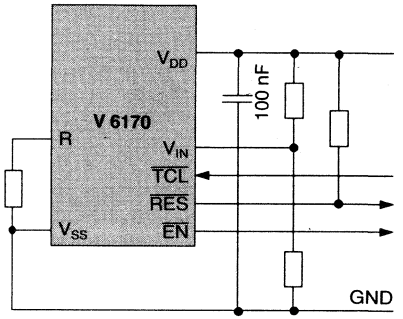


Fig. 1

Pin Assignment

DIP8 / SO8

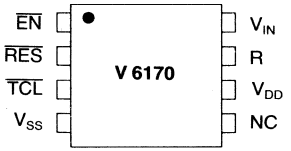


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS} +7 V
Minimum voltage at V_{DD}	V_{DDmin}	V_{SS} −0.3 V
Max. voltage at any signal pin	V_{MAX}	V_{DD} +0.3 V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3 V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+70	°C
Supply voltage[1]	V_{DD}	3		5.5	V
$\overline{RES}$ & $\overline{EN}$ guaranteed[2]	V_{DD}	1.2			V
Comparator input voltage	V_{IN}	0		V_{DD}	V
RC-oscillator programming	R	10		1000	kΩ

Table 2

[1] A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

[2] $\overline{RES}$ must be pulled up externally to V_{DD} event if it is unused.
(Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

Electrical Characteristics

$3.0 \leq V_{DD} \leq 5.5$ V, C = 100 nF, $T_A = -40$ to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{DD}, V_{IN} = 0 V		24	35	μA
Supply current	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{DD}, O/Ps 1 MΩ to V_{DD}		55	100	μA
$\overline{RES}$ and $\overline{EN}$						
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$						
Output High Voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{DD} = 2.0 V, I_{OH} = −100 μA	1.8	1.9		V
	V_{OH}	V_{DD} = 1.2 V, I_{OH} = −30 μA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}	$3 V \leq V_{DD} \pm 5.5 V$	V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}	$3 V \leq V_{DD} \leq 5.5 V$	2.0		V_{DD}	V
Leakage current $\overline{TCL}$ input	I_{LI}	$V_{SS} \leq V_{TCL} \leq V_{DD}$		0.05	1	μA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference[1]	V_{REF}	T_A = 25°C	1.148	1.170	1.200	V
	V_{REF}	T_A = −20 to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis[1]	V_{HY1}			2		mV
Level detector of V_{DD}[2]	V_{HIGH}	T_A = 25°C	5.78	5.95	6.12	V
	V_{HIGH}		5.60		6.30	V
Hysteresis[2]	V_{HY2}			50		mV

Table 3

[1] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

[2] The level detector of V_{DD} (V_{HIGH}) is the level when V_{DD} is rising. The level detector when V_{DD} is falling equals V_{HIGH} minus the hysteresis (V_{HY2}) (see Fig. 5).

I_{SS} Standby versus Temperature at V_{DD} = 5.5 V

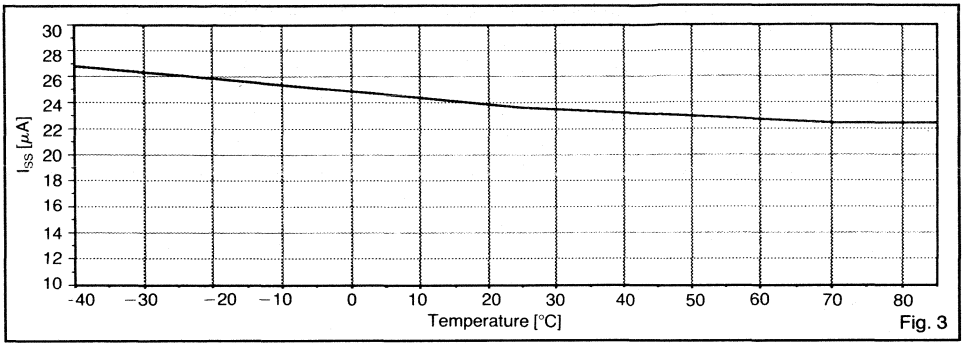


Fig. 3

Timing Characteristics

V_{DD} = 5.0 V ± 3%, C = 100 nF, T_A = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

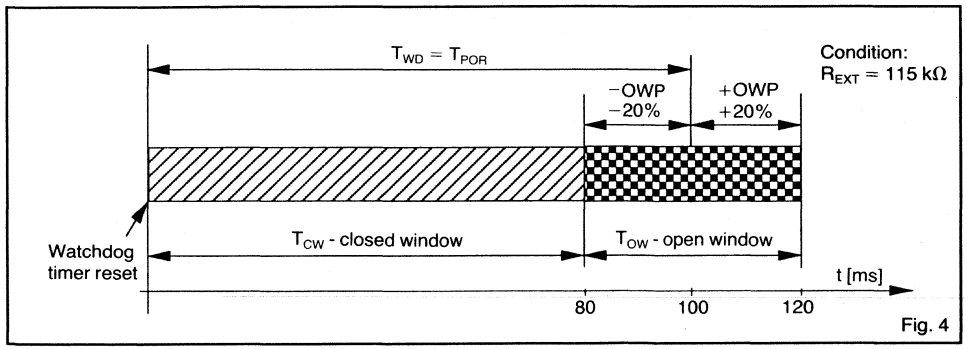


Fig. 4

Voltage Monitoring

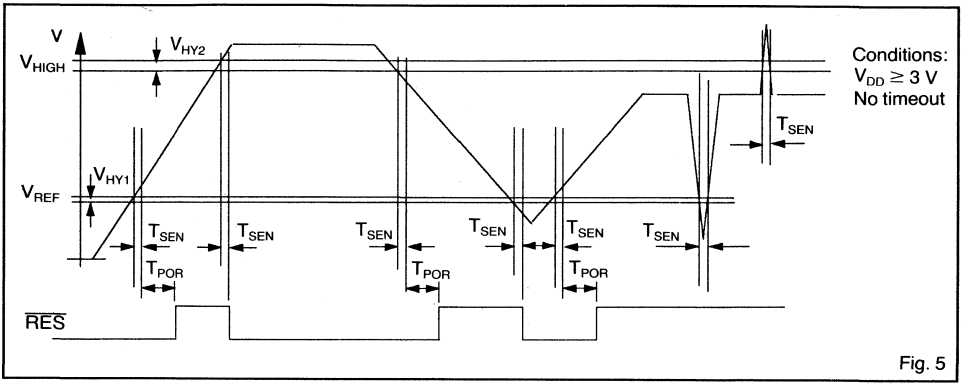


Fig. 5

Timer Reaction

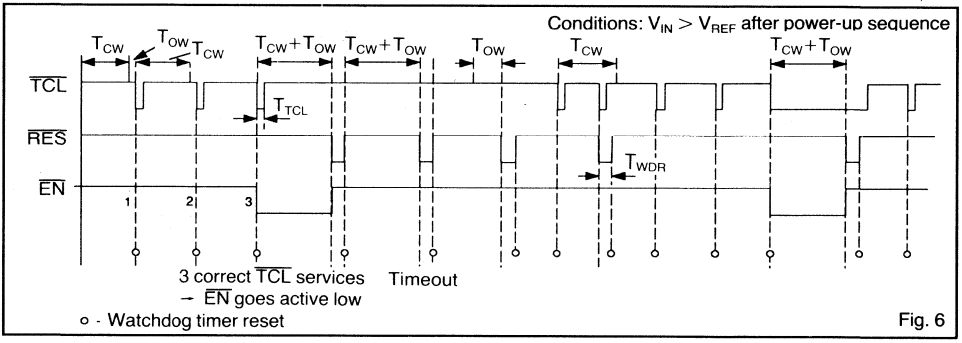


Fig. 6

Combined Voltage and Timer Reaction

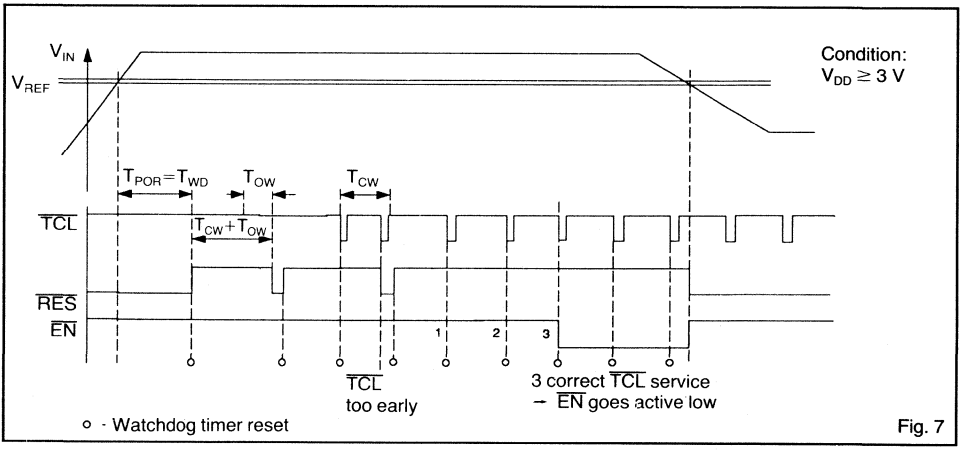


Fig. 7

Block Diagram

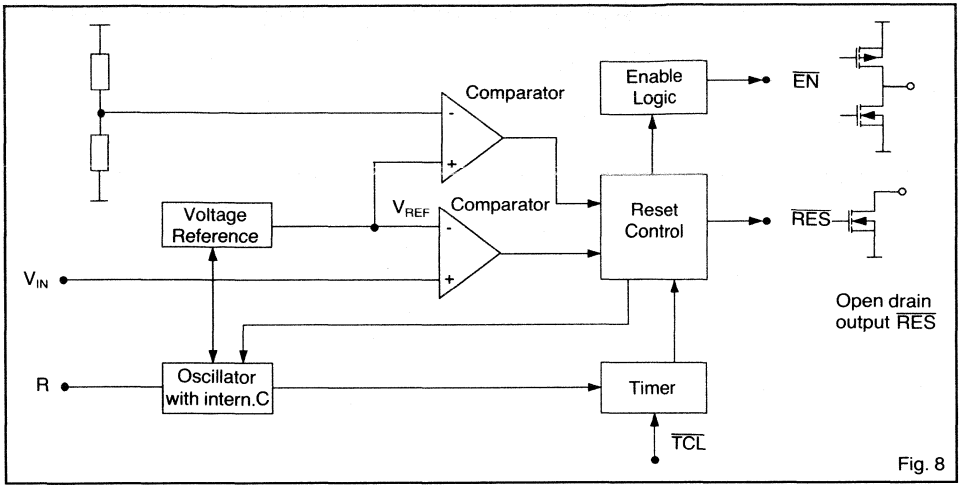


Fig. 8

Pin Description

Pin	Name	Function
1	$\overline{EN}$	Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{DD} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	NC	No connection
6	V_{DD}	Voltage supply
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 9. The user defines an external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5). When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Voltage Window

The reset output ($\overline{RES}$) is inactive when V_{IN} is higher than V_{REF} and when V_{DD} is lower than V_{HIGH}. If V_{IN} is less than V_{REF} or V_{DD} higher than V_{HIGH}, the reset output goes active low (see Fig. 5).

Timer Programming

The on-chip oscillator needs an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9). It allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 115 kΩ, the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer

resets and is defined by $T_{CW} = T_{WD} - OWP\ (T_{WD})$
The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP\ (T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP\ (T_{WD})$.
For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically $R_{EXT} \times 0.87$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 115 kΩ, then T_{WD} = 100 ms ± 10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period, a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 6).
With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset.
If the software is stuck in a loop which includes the routine to clear the watchdog, a conventional watchdog will not reset the system even though the software is malfunctioning; the V 6170 will generate a system reset because the watchdog is cleared too quickly.
If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").
The $\overline{RES}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 9).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 µs, overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable − $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.
A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V 6170 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

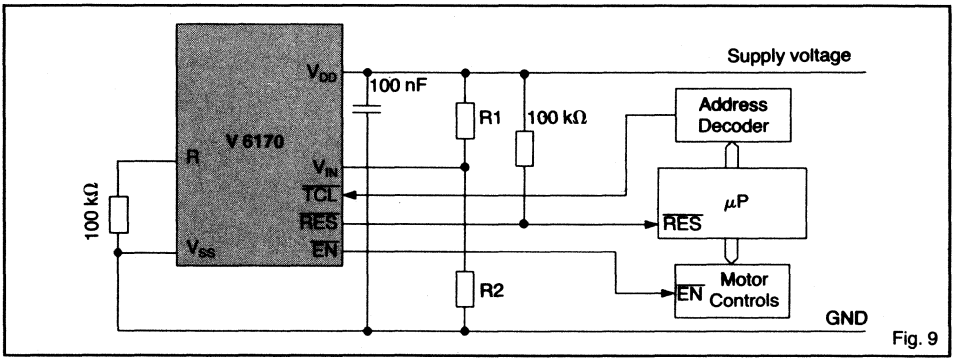


Fig. 9

T_{WD} versus Temperature at 5 V

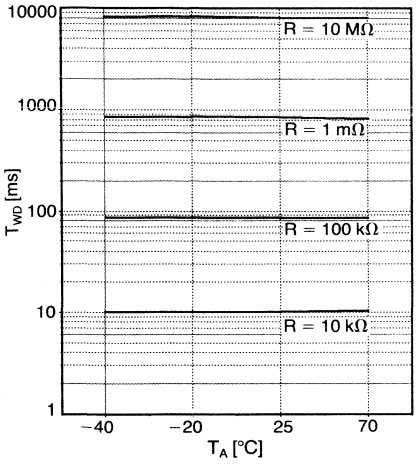


Fig. 10

T_{WD} versus R at 5 V

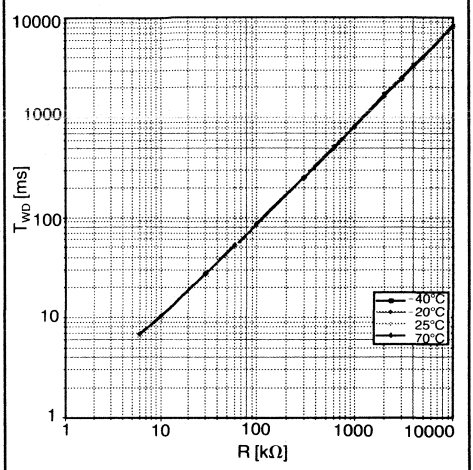


Fig. 11

T_{WD} versus V_{DD} at T_A = +25°C

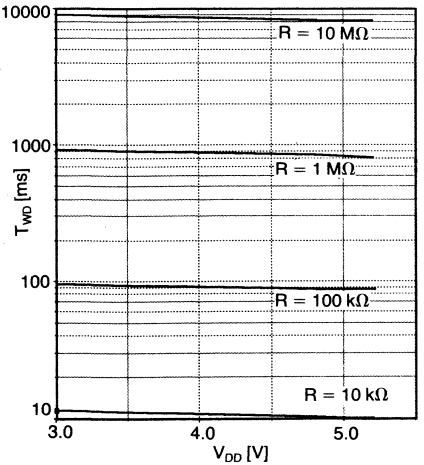


Fig. 12

T_{WD} versus R at T_A = +25°C

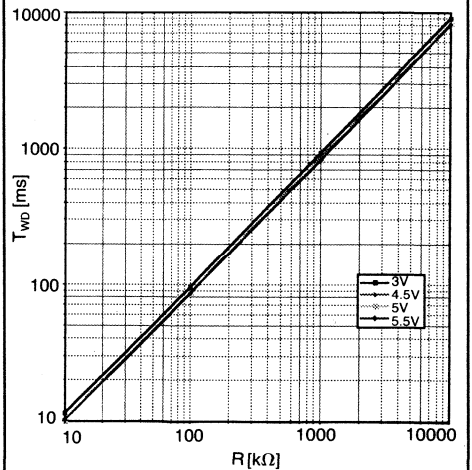


Fig. 13

6

T_{WD} versus R at T_A = +25°C

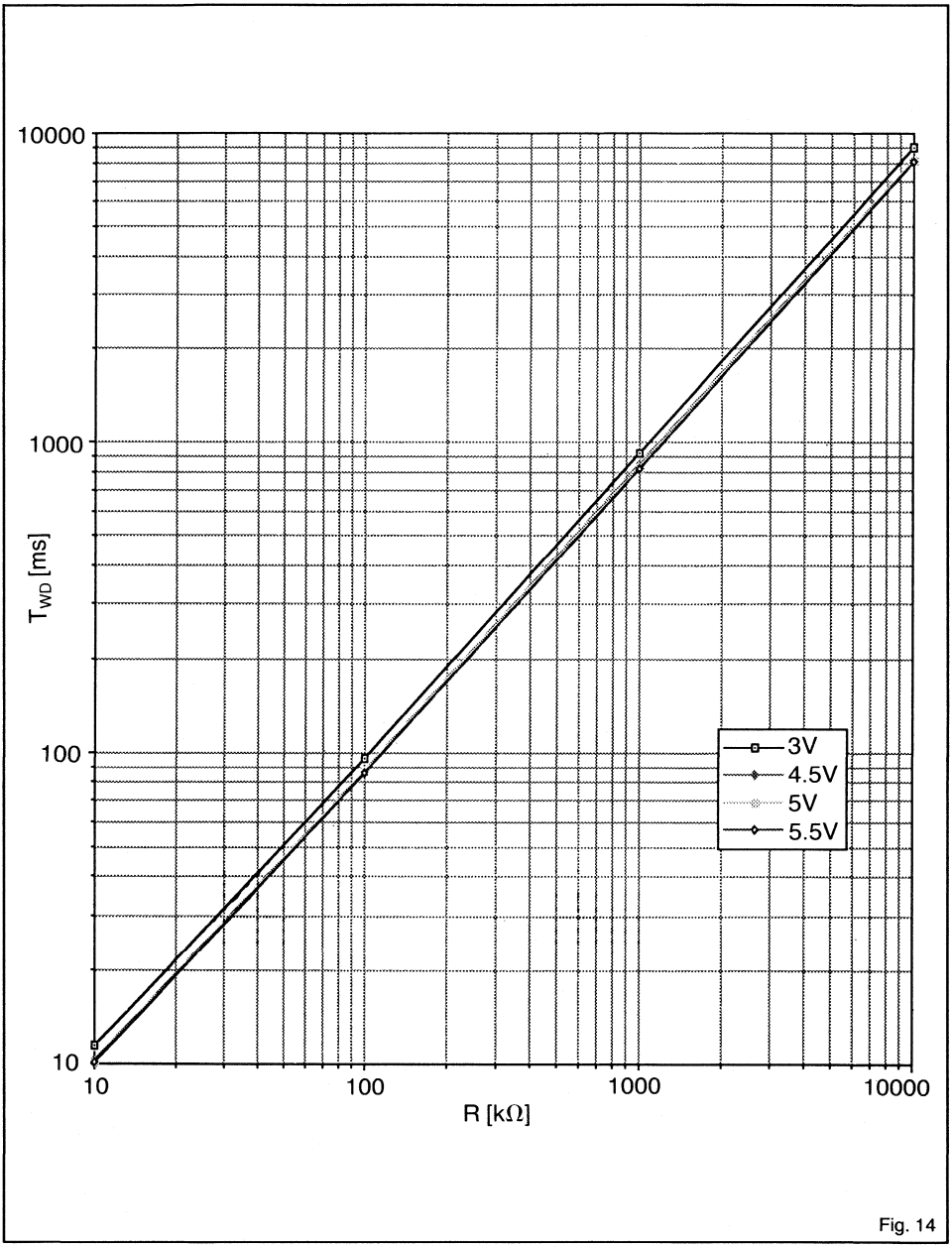


Fig. 14

T_{WD} versus V_{DD} at $T_A = +70°C$

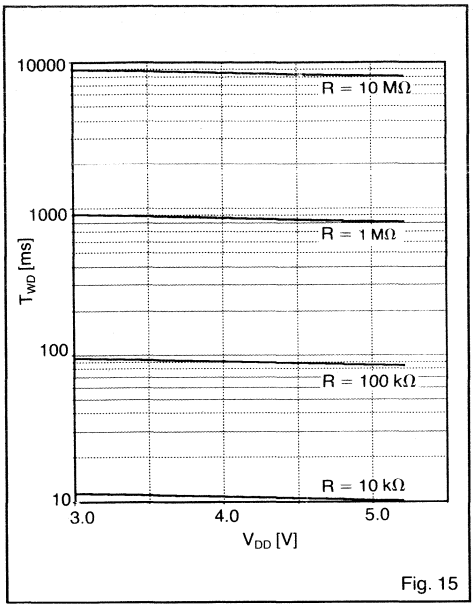


Fig. 15

T_{WD} versus R at $T_A = +70°C$

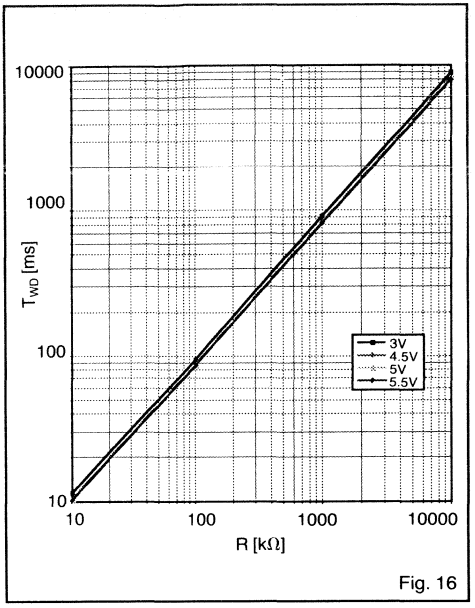


Fig. 16

T_{WD} versus V_{DD} at $T_A = -40°C$

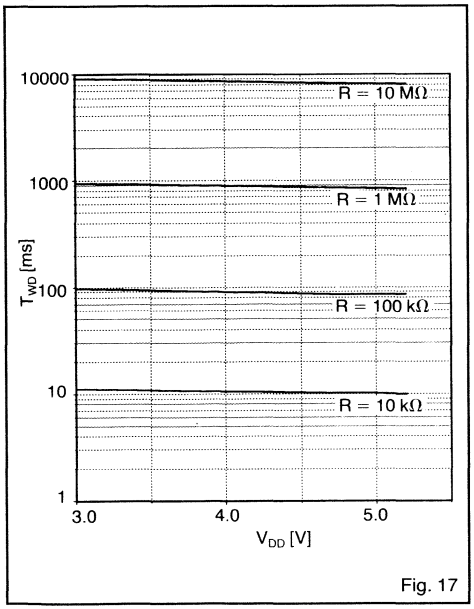


Fig. 17

T_{WD} versus R at $T_A = -40°C$

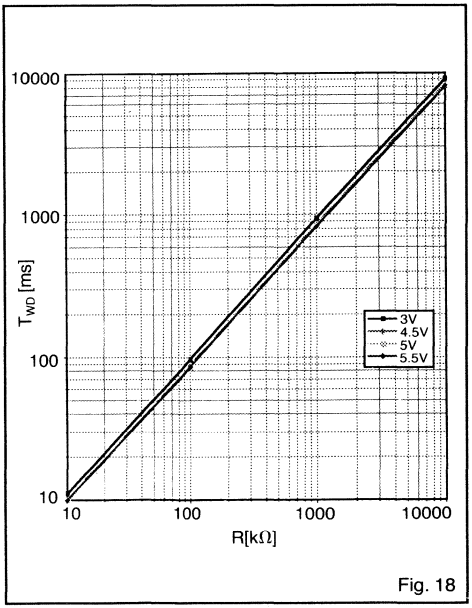
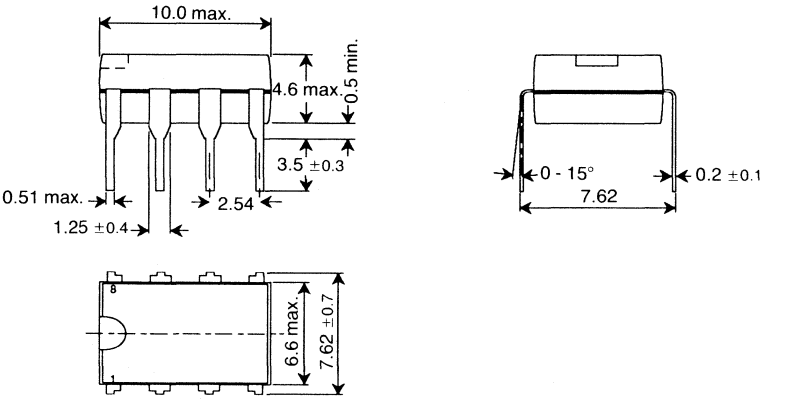


Fig. 18

Package and Ordering Information

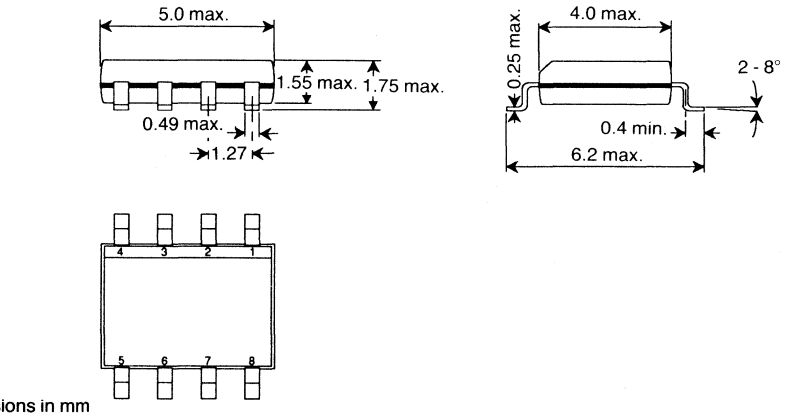
Dimensions of DIP8 Package



Dimensions in mm

Fig. 19

Dimensions of SO8 Package



Dimensions in mm

Fig. 20

Ordering Information

The V 6170 is available in the following packages:

Type	Package
V 6170 8P	DIP8
V 6170 8S	SO8

When ordering please specify complete part number.

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Watchdog

Features

- Standby mode, maximum current 35 μA
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, reset threshold 1.17 V
- $\pm$ 1.5% threshold tolerance at 25°C
  $\pm$ 3% threshold tolerance for -40 to $+70$°C
- Programmable reset voltage monitoring
- Voltage window, high threshold 5.9 V
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy $\pm$ 10%
- System enable ($\overline{EN}$) output offers added security
- 3 chip select feed-thru circuit controlled by $\overline{EN}$
- TTL / CMOS compatible
- -40 to $+70$°C temperature range
- DIP14 and SO14 packages

Description

The V 6173 offers a high level of integration by voltage monitoring and software monitoring in an 14 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V or when V_{DD} is higher than 5.9 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products

Typical Operating Configuration

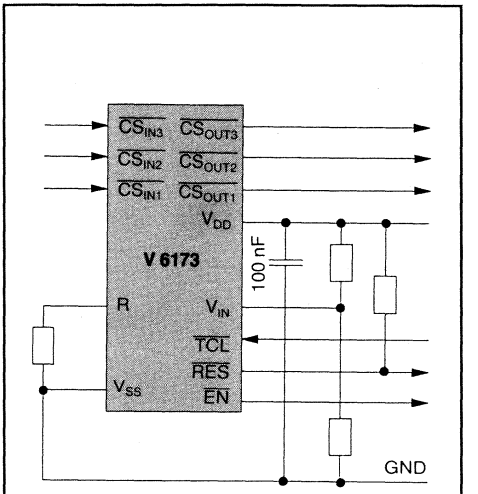


Fig. 1

Pin Assignment

DIP14 / SO14

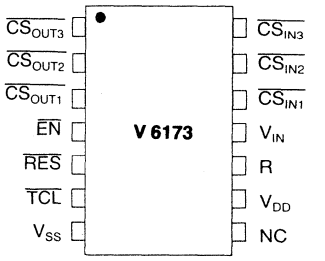


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	$V_{SS}+7$ V
Minimum voltage at V_{DD}	V_{DDmin}	$V_{SS}-0.3$ V
Max. voltage at any signal pin	V_{MAX}	$V_{DD}+0.3$ V
Min. voltage at any signal pin	V_{MIN}	$V_{SS}-0.3$ V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+70	°C
Supply voltage[1]	V_{DD}	3		5.5	V
$\overline{RES}$ & $\overline{EN}$ guaranteed[2]	V_{DD}	1.2			V
Comparator input voltage	V_{IN}	0		V_{DD}	V
RC-oscillator programming	R	10		1000	kΩ

Table 2

[1] A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

[2] $\overline{RES}$ must be pulled up externally to V_{DD} event if it is unused.
(Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

Electrical Characteristics

$3 \leq V_{DD} \leq 5.5$ V, C = 100 nF, $T_A = -40$ to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{DD}, V_{IN} = 0 V		24	35	μA
Supply current	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{DD}, O/Ps 1 MΩ to V_{DD}		55	100	μA
$\overline{RES}$, $\overline{EN}$ and $\overline{CS_{OUT1/2/3}}$						
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$ and $\overline{CS_{OUT1/2/3}}$						
Output High Voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{DD} = 2.0 V, I_{OH} = −100 μA	1.8	1.9		V
	V_{OH}	V_{DD} = 1.2 V, I_{OH} = −30 μA	1.0	1.1		V
$\overline{TCL}$, V_{IN} and $\overline{CS_{IN1/2/3}}$						
$\overline{TCL}$ and $\overline{CS_{IN1/2/3}}$ Input Low Level	V_{IL}	$3\,V \leq V_{DD} \pm 5.5$ V	V_{SS}		0.8	V
$\overline{TCL}$ and $\overline{CS_{IN1/2/3}}$ Input High Level	V_{IH}	$3\,V \leq V_{DD} \leq 5.5$ V	2.0		V_{DD}	V
Leakage current $\overline{TCL}$ input	I_{LI}	$V_{SS} \leq V_{TCL} \leq V_{DD}$		0.05	1	μA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference[1]	V_{REF}	T_A = 25°C	1.148	1.170	1.200	V
	V_{REF}	T_A = −20 to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis[1]	V_{HY1}			2		mV
Level detector of V_{DD}[2]	V_{HIGH}	T_A = 25°C	5.78	5.95	6.12	V
	V_{HIGH}		5.60		6.30	V
Hysteresis[2]	V_{HY2}			50		mV

Table 3

[1] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 6).

[2] The level detector of V_{DD} (V_{HIGH}) is the level when V_{DD} is rising. The level detector when V_{DD} is falling equals V_{HIGH} minus the hysteresis (V_{HY2}) (see Fig. 6).

I_{SS} Standby versus Temperature at V_{DD} = 5.5 V

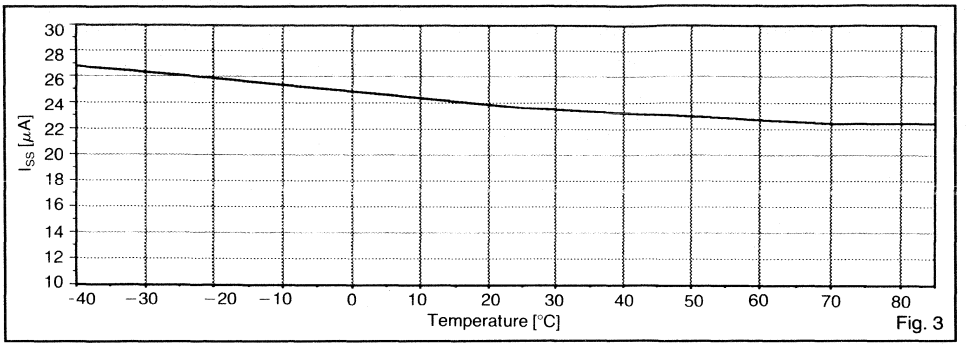


Fig. 3

Timing Characteristics

V_{DD} = 5.0 V ± 3%, C = 100 nF, T_A = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at rising edge	T_{CSH}			125	200	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at falling edge	T_{CSL}			75	150	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

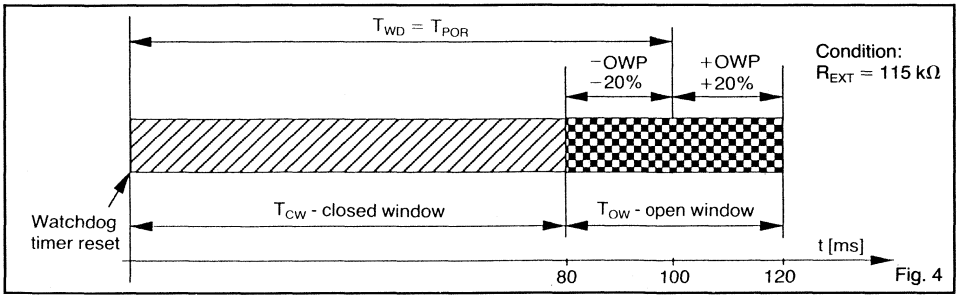


Fig. 4

Chip Select

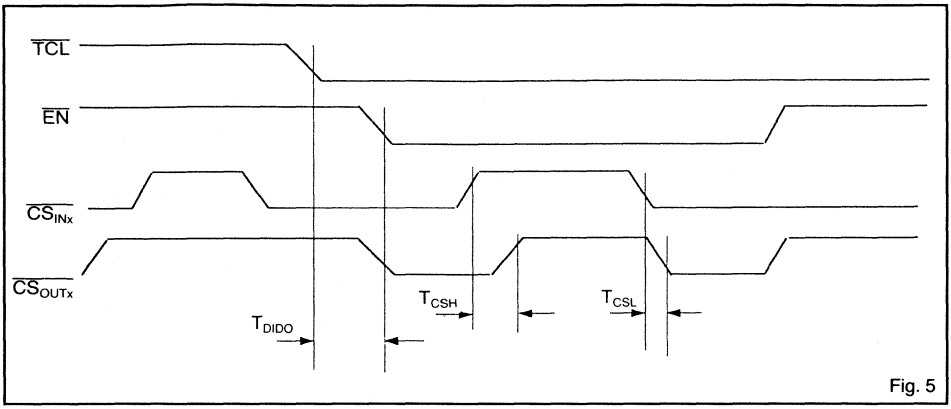


Fig. 5

Voltage Monitoring

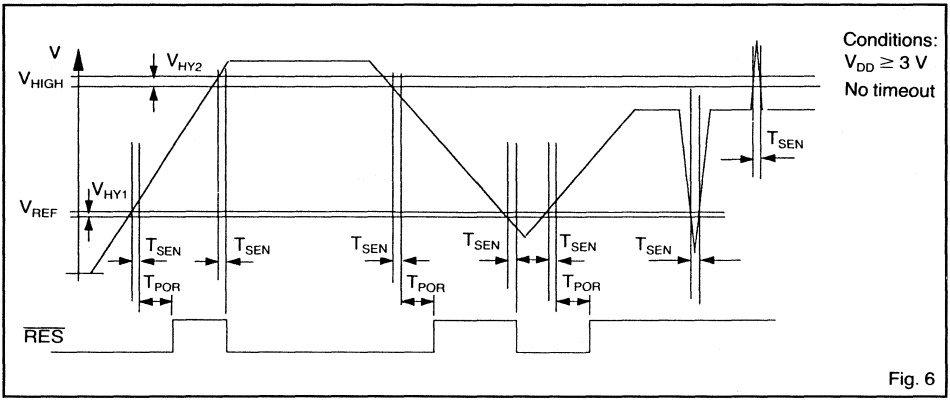


Fig. 6

Timer Reaction

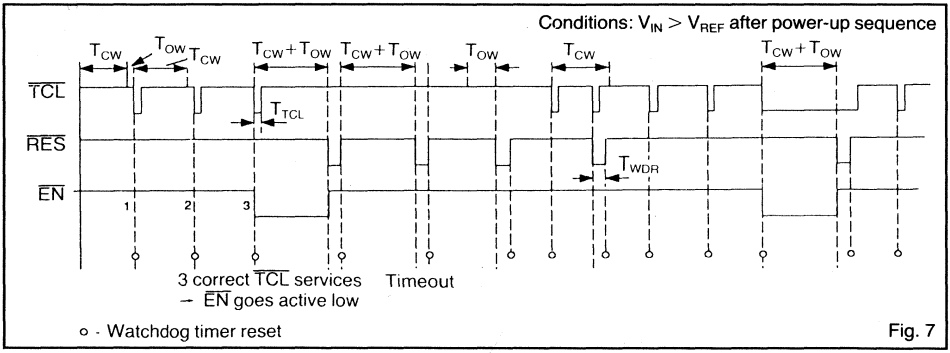


Fig. 7

Combined Voltage and Timer Reaction

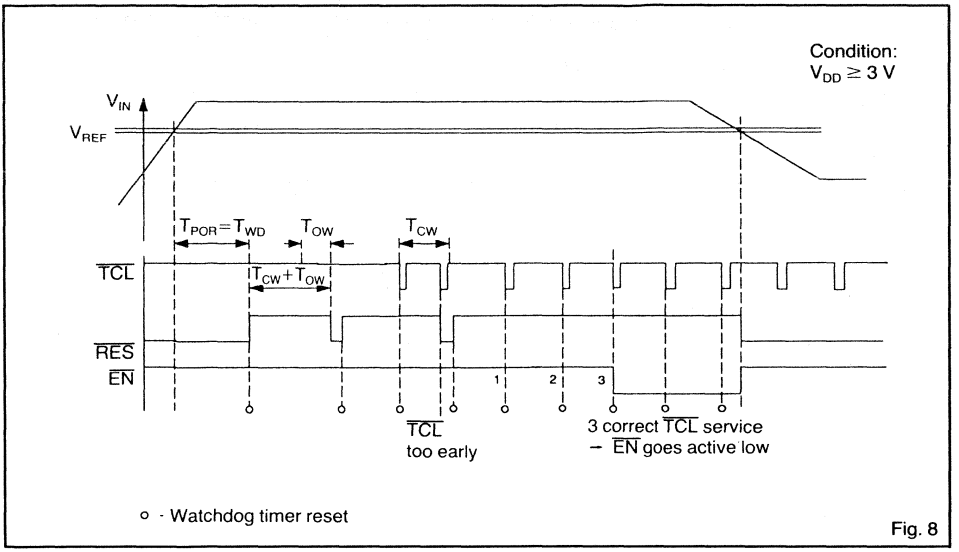


Fig. 8

Block Diagram

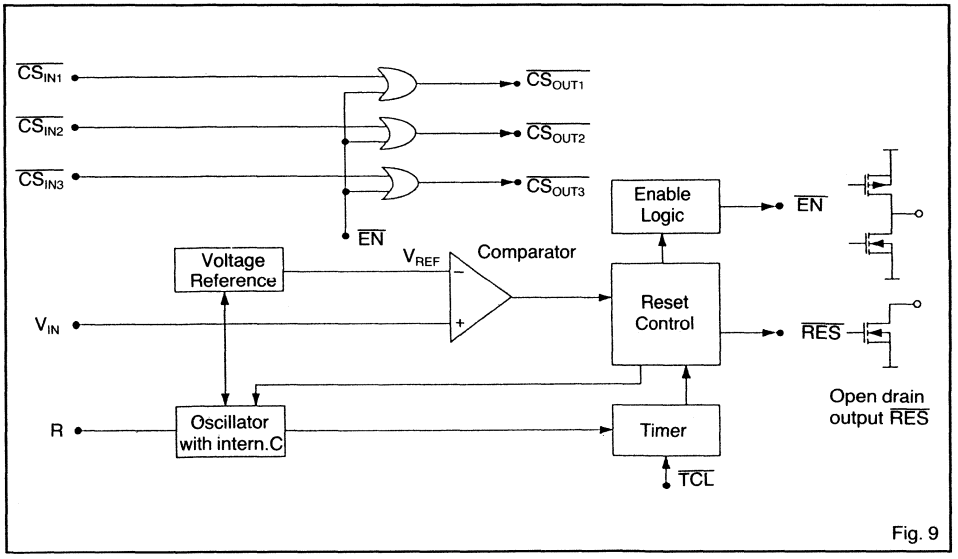


Fig. 9

Pin Description

Pin	Name	Function
1	$\overline{CS_{OUT3}}$	Push-pull active low chip select output 3
2	$\overline{CS_{OUT2}}$	Push-pull active low chip select output 2
3	$\overline{CS_{OUT1}}$	Push-pull active low chip select output 1
4	$\overline{EN}$	Push-pull active low enable output
5	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{DD} even if unused
6	$\overline{TCL}$	Watchdog timer clear input signal
7	V_{SS}	GND terminal
8	NC	No connection
9	V_{DD}	Voltage supply
10	R	R_{EXT} input for RC oscillator tuning
11	V_{IN}	Voltage comparator input
12	$\overline{CS_{IN1}}$	Chip select input 1
13	$\overline{CS_{IN2}}$	Chip select input 2
14	$\overline{CS_{IN3}}$	Chip select input 3

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 10. The user defines an external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 6). When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 µs.

Voltage Window

The reset output ($\overline{RES}$) is inactive when V_{IN} is higher than V_{REF} and when V_{DD} is lower than V_{HIGH}. If V_{IN} is less than V_{REF} or V_{DD} higher than V_{HIGH}, the reset output goes active low (see Fig. 6).

Timer Programming

The on-chip oscillator needs an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 10). It allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 115 kΩ, the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP\ (T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP\ (T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP\ (T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically $R_{EXT} \times 0.87$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 115 kΩ, then T_{WD} = 100 ms ± 10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period, a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 7).

With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. If the software is stuck in a loop which includes the routine to clear the watchdog, a conventional watchdog will not reset the system even though the software is malfunctioning; the V 6173 will generate a system reset because the watchdog is cleared too quickly.

If no $\overline{TCL}$ pulse is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 10).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 8. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs, overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable – $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.
A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V 6173 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

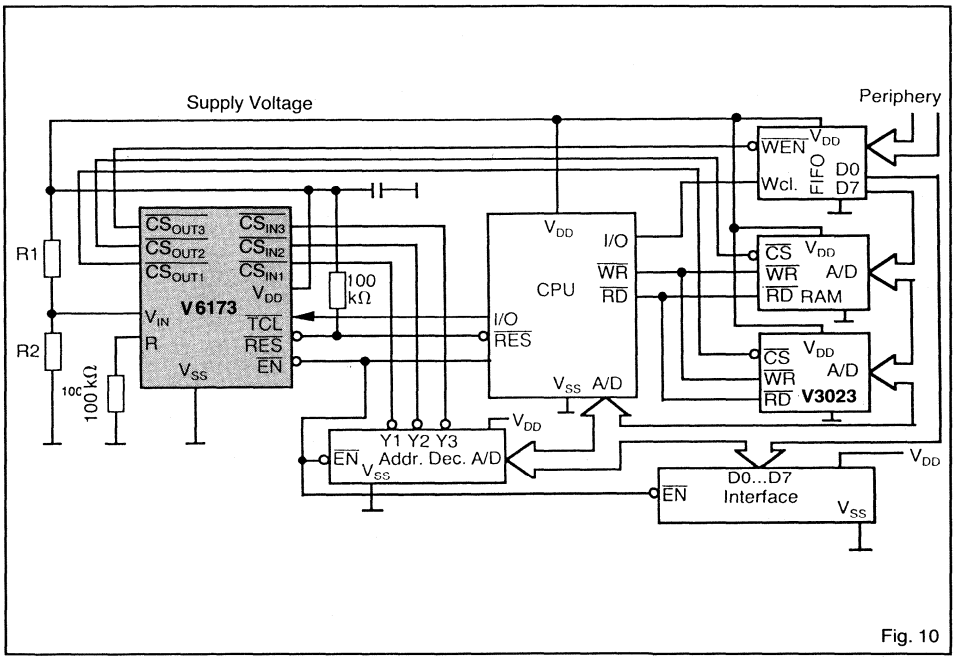


Fig. 10

T_{WD} versus Temperature at 5 V

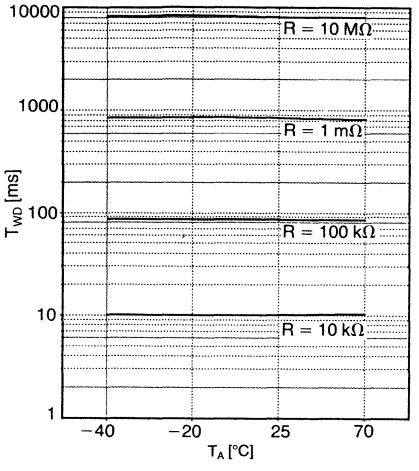


Fig. 11

T_{WD} versus R at 5 V

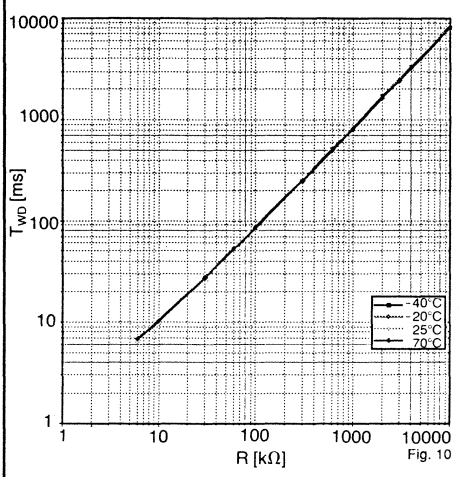


Fig. 10

Fig. 12

T_{WD} versus V_{DD} at T_A = +25°C

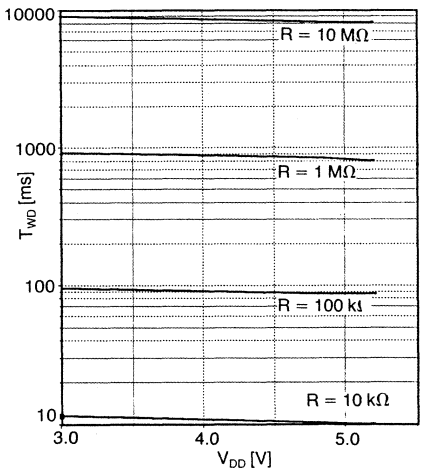


Fig. 13

T_{WD} versus R at T_A = +25°C

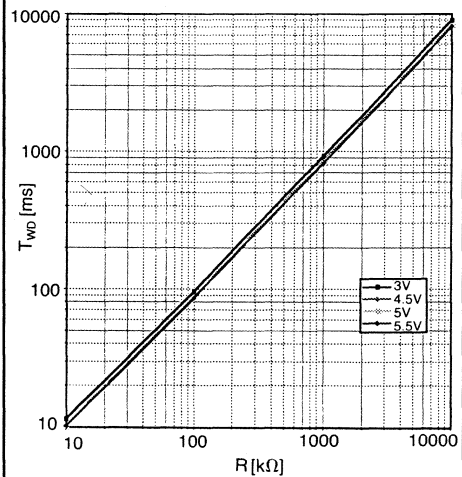


Fig. 14

T_{WD} versus R at $T_A = +25°C$

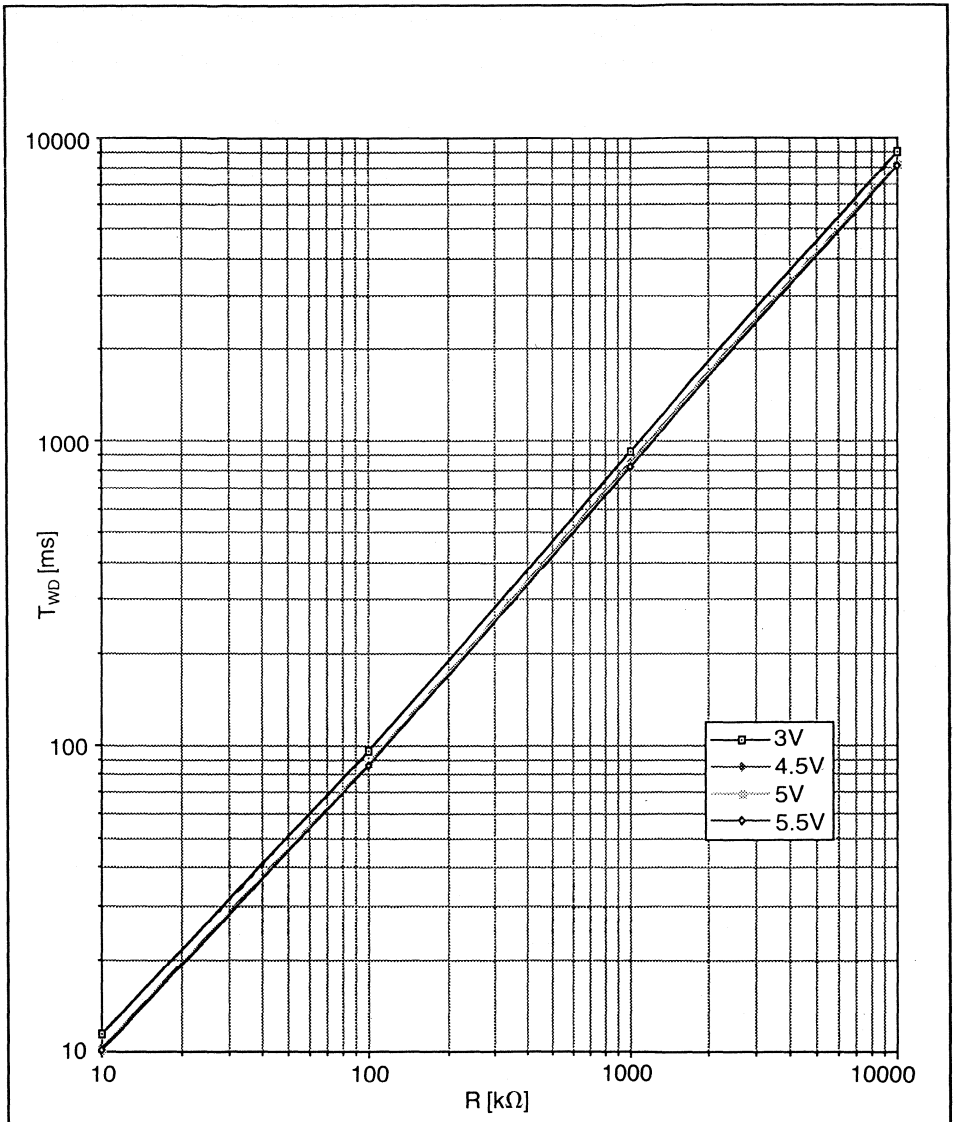


Fig. 15

T_{WD} versus V_{DD} at $T_A = +70°C$

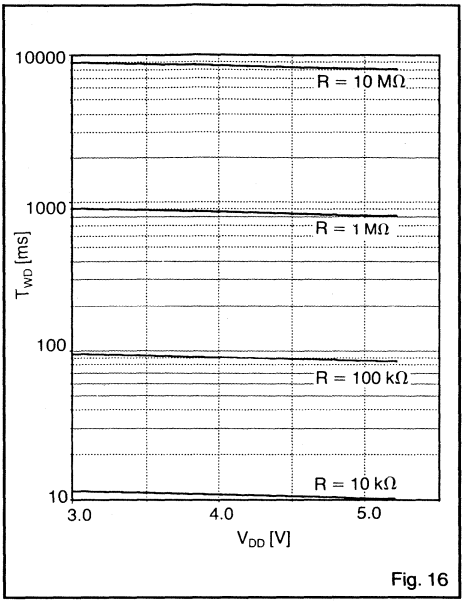


Fig. 16

T_{WD} versus R at $T_A = +70°C$

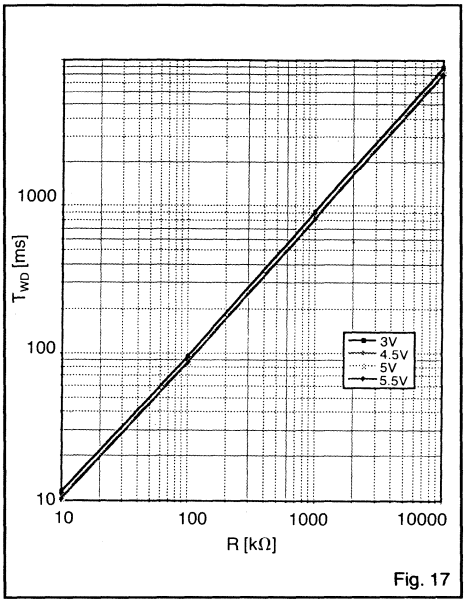


Fig. 17

T_{WD} versus V_{DD} at $T_A = -40°C$

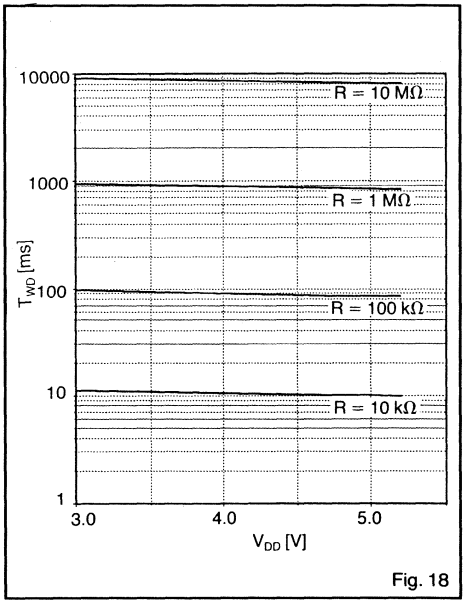


Fig. 18

T_{WD} versus R at $T_A = -40°C$

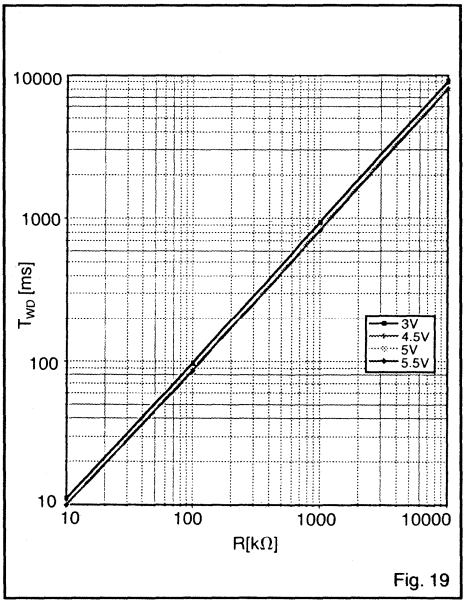
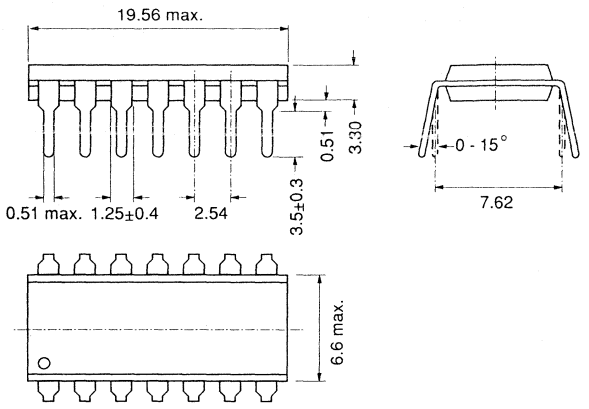


Fig. 19

Package and Ordering Information

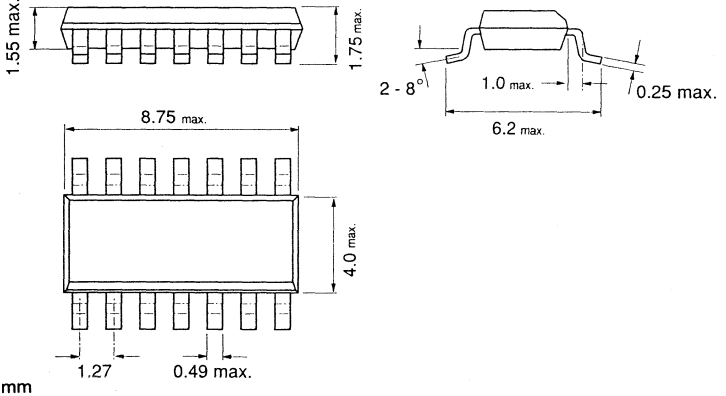
Dimensions of DIP14 Package



Dimensions in mm

Fig. 20

Dimensions of SO14 Package



Dimensions in mm

Fig. 21

Ordering Information

The V 6173 is available in the following packages:

Type	Package
V 6173 14P	DIP14
V 6173 14S	SO14

When ordering please specify complete part number.

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Table of Contents

H 6052

Smart Reset

Features

- Proper microprocessor restart after power up
- Processor reset at power down
- On-chip oscillator gives a typical POR of 160 ms
- Reset output working down to below 1.6 V
- No external components needed
- Very small mounting space
- TO-92 package
- SOT-223 package
- Sensitivity typically 10 μs

Description

The H 6052 is a CMOS device which monitors the supply voltage and controls the reset of the microprocessor. Upon the supply voltage rising above $V_{TH\ ON}$, the reset output, whether RES or $\overline{RES}$, will remain active (RES = 1, $\overline{RES}$ = 0) for an additional 160 ms. This allows the system voltage and the oscillator of the microprocessor system to stabilize before the system becomes fully active. When V_{DD} falls below $V_{TH\ OFF}$ the reset output goes active (RES = 1, $\overline{RES}$ = 0).

Applications

All microprocessor and microcontroller applications where an automatic restart of the microprocessor after power down is required:

- white goods
- brown goods
- automotive electronics
- industrial electronics

Typical Operating Configuration

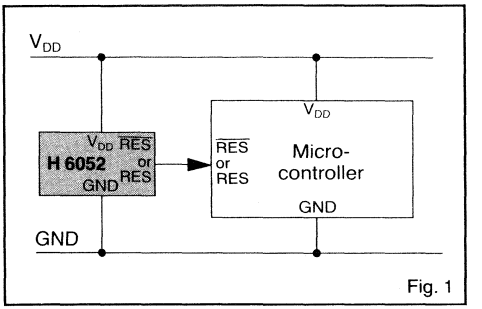
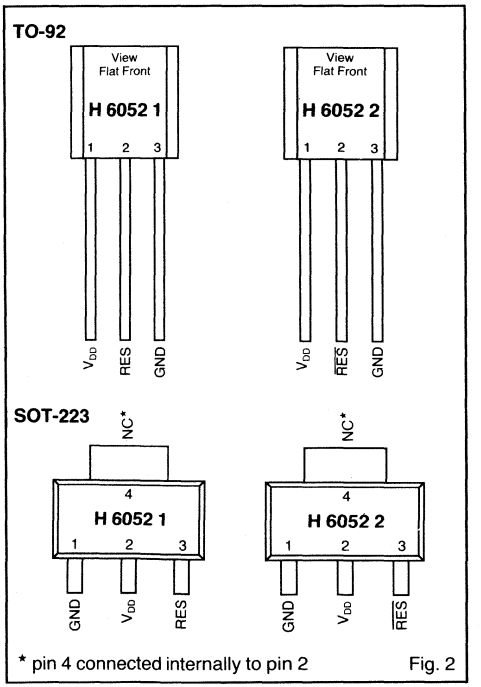


Fig. 1

Pin Assignment



* pin 4 connected internally to pin 2

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to GND	V_{DD}	−0.3 V to + 7 V
Voltage at RES or $\overline{RES}$	V_{min}	GND − 0.3 V
Voltage at RES or $\overline{RES}$	V_{max}	V_{DD} + 0.3 V
Storage temperature range	T_{STO}	−65° to +150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	1.6		5.5	V

Table 2

Electrical Characteristics

V_{DD} = 5.0 V ± 10%, T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply current	I_{DD}	RES or RES open		80	140	µA
Supply voltage:						
Power on threshold*	$V_{TH\,ON}$	T_A = +25°C	3.6	4	4.4	V
Power off threshold*	$V_{TH\,OFF}$	T_A = +25°C	2.8*	3.2*	3.6*	V
$\overline{RES}$ output high level	V_{OH}	I_{OH} = 2 mA	V_{DD} −0.4			V
$\overline{RES}$ output low level	V_{OL}	V_{DD} = 3.5 V, I_{OL} = 2 mA			0.4	V
$\overline{RES}$ output low level	V_{OL}	V_{DD} = 1.6 V, I_{OL} = 400 µA			0.4	V
RES output low level	V_{OL}	I_{OL} = 4 mA			0.4	V
RES output high level	V_{OH}	V_{DD} = 3.5 V, I_{OH} = 1.5 mA	V_{DD} −0.4			V
RES output high level	V_{OH}	V_{DD} = 1.6 V, I_{OH} = 80 µA	V_{DD} −0.4			V

* V_{THON} is related to $V_{TH\,OFF}$. Typically, $V_{TH\,OFF}$ = $V_{TH\,ON}$ − 0.8 V

Table 3

Timing Characteristics

V_{DD} = 5 V ± 10%, T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power on reset	t_{POR}		70		350	ms
Power on reset	t_{POR}	T_A = 25°C	100	160	250	ms

Table 4

Timing Waveforms

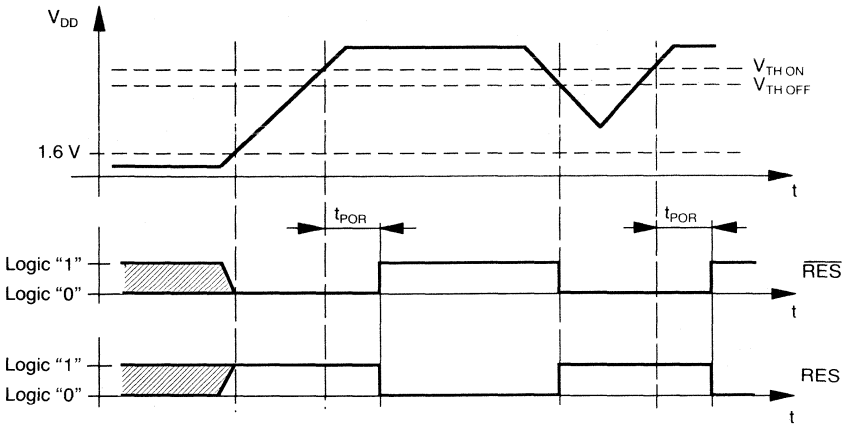


Fig. 3

Block Diagram

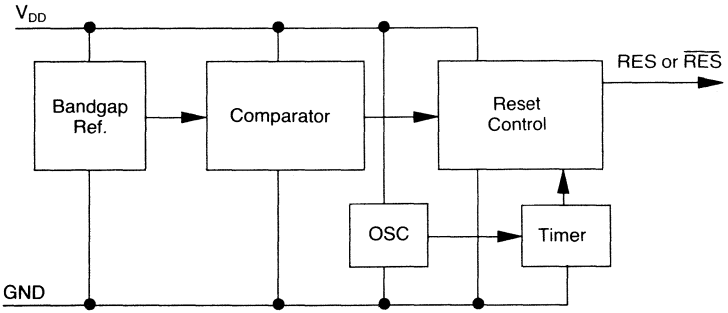


Fig. 4

Pin Description

TO-92

Pin	Name	Function
1	GND	Supply GND
2	RES or $\overline{RES}$	Reset output (H 6052 1) $\overline{Reset}$ output (H 6052 2)
3	V_{DD}	Positive supply

Table 5

SOT-223

Pin	Name	Function
1	GND	Supply ground
2	V_{DD}	Positive supply
3	RES or $\overline{RES}$	Reset output (H 6052 1) $\overline{Reset}$ output (H 6052 2)
4	NC	No connection (pin 4 connected internally to pin 2)

Table 6

Typical Applications

Power On Reset

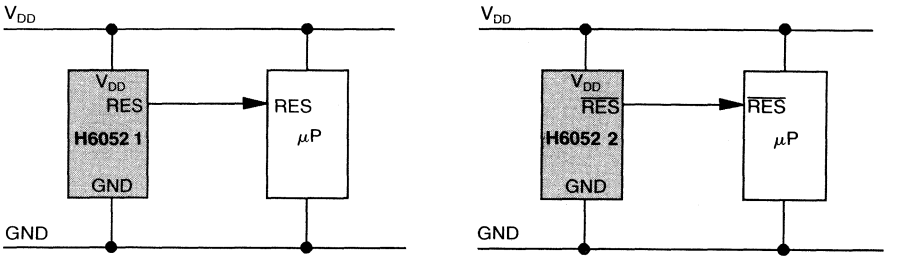
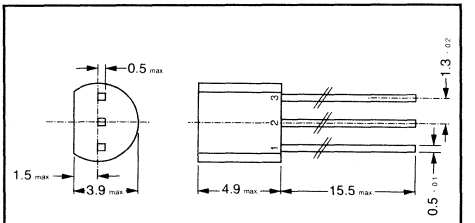


Fig. 5

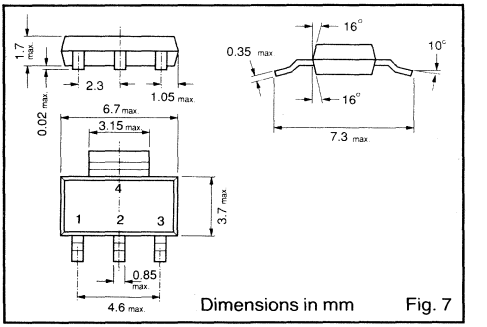
Package and Ordering Information

Dimensions of TO-92 Package



Dimensions in mm Fig. 6

Dimensions of SOT-223 Package



Dimensions in mm Fig. 7

Ordering Information

The H 6052 is available in the following packages:

Part number:	Package:	
H 6052 1	TO-92	Reset Output
H 6052 1	SOT-223	Reset Output
H 6052 2	TO-92	$\overline{\text{Reset}}$ Output
H 6052 2	SOT-223	$\overline{\text{Reset}}$ Output

When ordering please specify complete part number and package.

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Smart Reset

Features

- Clear microprocessor restart after power up
- Processor reset at power down
- Reset output guaranteed down to V_{DD} = 1 V
- Low power consumption: typ. 3 μA at V_{DD} = 5 V
- On-chip oscillator
- No external components required
- Push-pull or Open drain output
- TO-92 and SOT-223 packages
- Pin compatible with DS 1233 A in TO-92

Description

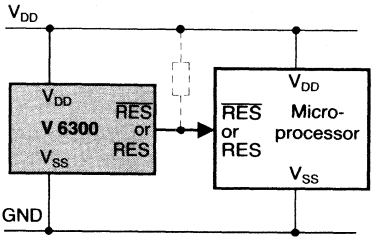
The V 6300 monitors the supply voltage of any electronic systems, and generates the appropriate Reset signal. The threshold defines the minimum allowed voltage which guarantees the good functionality of the system. As long as V_{DD} stays upside this voltage level, the output stays inactive. If V_{DD} drops below V_{TH}, the output gets active. When V_{DD} rises above V_{TH}, the output remains active for an additional 50 ms (typ.). This allows the system to stabilize before getting fully active. The threshold voltage may be obtained in different versions: 2 V, 2.4 V, 2.8 V, 3.5 V, 4 V, 4.5 V.

Applications

All microprocessor applications where an automatic restart is required:

- White / Brown goods
- Automotive electronics
- Industrial electronics
- Telecom systems
- Hand-held systems

Typical Operating Configuration



For Open drain version: – – – – –

Fig. 1

Pin Assignment

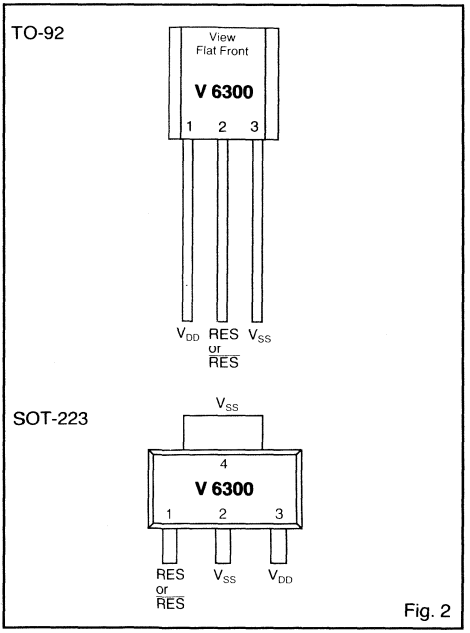


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to V_{SS}	V_{DD}	−0.3 V to +10 V
Min. voltage at RES or $\overline{RES}$	V_{min}	V_{SS} −0.3 V
Max. voltage at RES or $\overline{RES}$	V_{max}	V_{DD} +0.3 V
Storage temperature range	T_{STO}	−65° to +150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	1		8	V

Table 2

Electrical Characteristics

T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Min. at 25°C	Typ.	Max. at 25°C	Max.	Units
Supply current[1]	I_{DD}	V_{DD} = 2 V			1.5	2.1	3.1	µA
	I_{DD}	V_{DD} = 5 V			3	3.9	5.7	µA
	I_{DD}	V_{DD} = 8 V			5.2	6.8	10	µA
Threshold voltage	V_{TH}	Version: A, G, M	1.77	1.84	1.95	2.04	2.17	V
	V_{TH}	Version: B, H, N	2.09	2.18	2.32	2.41	2.55	V
	V_{TH}	Version: C, I, O	2.48	2.59	2.73	2.86	3.03	V
	V_{TH}	Version: D, J, P	3.11	3.23	3.42	3.59	3.80	V
	V_{TH}	Version: E, K, Q	3.55	3.70	3.88	4.08	4.32	V
	V_{TH}	Version: F, L, R	4.05	4.22	4.42	4.67	4.95	V
Threshold hysteresis	V_{HYS}				25			mV
RES Output Low Level	V_{OL}	V_{DD} = 5 V, I_{OL} = 8 mA			175		400	mV
	V_{OL}	V_{DD} = 3 V, I_{OL} = 4 mA			140		300	mV
	V_{OL}	V_{DD} = 1 V, I_{OL} = 50 µA			20		90	mV
RES Output High Level	V_{OH}	V_{DD} = 5 V, I_{OH} = −8 mA	4.3		4.5			V
	V_{OH}	V_{DD} = 3 V, I_{OH} = −4 mA	2.3		2.6			V
	V_{OH}	V_{DD} = 1 V, I_{OH} = −100 µA	850		950			mV
Output leakage current[2]	I_{LEAK}	V_{DD} = 8 V			0.05		1	µA

[1] RES or $\overline{RES}$ open
[2] Only for Open drain versions

Table 3

Timing Characteristics

V_{DD} = 5 V, T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power on Reset time	t_{POR}		25	50	75	ms
Sensitivity[3]	t_{SEN}	for V_{DD} = 5 V to 3 V in 5 µs	20	0.8 · t_R		µs
Reaction time[3]	t_R	for V_{DD} = 5 V to 3 V in 5 µs	22	75	150	µs

[3] Tested on versions with V_{TH} higher than 3 V

Table 4

Timing Waveforms

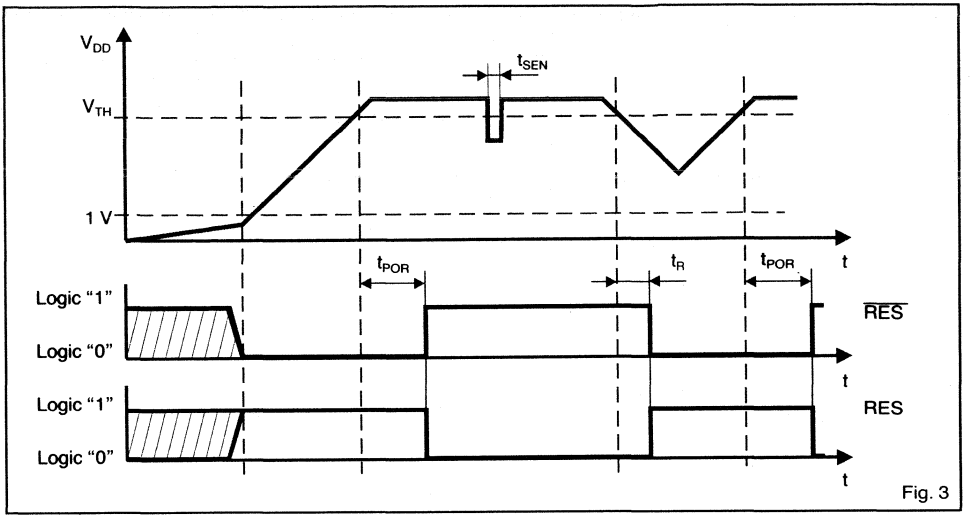


Fig. 3

Block Diagram

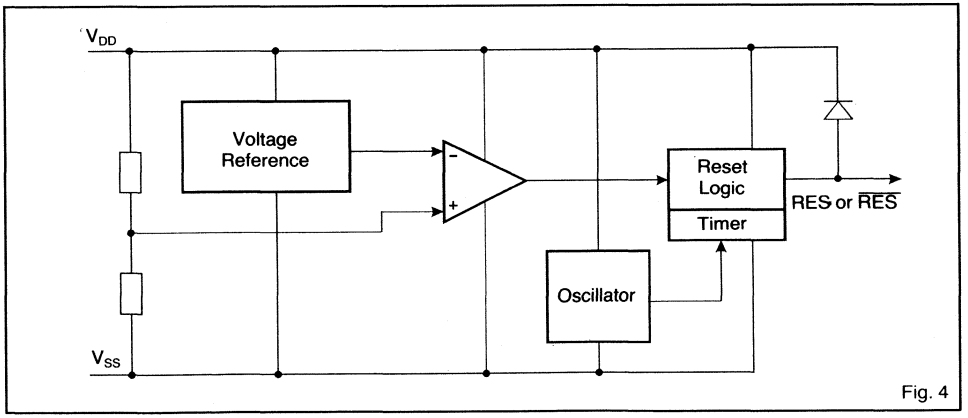


Fig. 4

Pin Description

TO-92

Pin	Name	Function
1	V_{DD}	Positive Supply
2	RES or $\overline{RES}$	Reset output
3	V_{SS}	Supply ground

Table 5

SOT-223

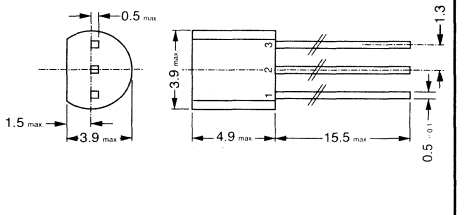
Pin	Name	Function
1	RES or $\overline{RES}$	Reset output
2	V_{SS}	Supply ground
3	V_{DD}	Positive Supply
4*	V_{SS}	Supply ground

* Internally connected to pin 2

Table 6

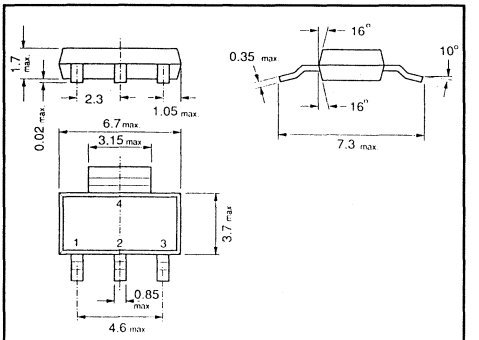
Package and Ordering Information

Dimensions of TO-92 Package



Dimensions in mm Fig. 6

Dimensions of SOT-223 Package



Dimensions in mm Fig. 7

Ordering Information

The V 6300 is available with Push-pull or Open drain output stage and Reset active low or high.

Ordering form: V 6300 <version letter> <packaging>

Example: Smart reset with: - Reset active low
- Open drain output
- 2.8 V threshold
- TO-92 package

V 6300 O TO-92

When ordering, please specify the complete part number.

Version letter definition

Output stage	Threshold Voltage [V]					
	2.0	2.4	2.8	3.5	4	4.5
Push-pull, Reset active low	A*	B*	C*	D*	E*	F*
Push-pull, Reset active high	G*	H*	I	J*	K*	L*
Open drain, Reset active low	M*	N*	O	P	Q*	R*

* and Chip form, on request Table 7

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Smart Reset

Features

- Voltage Window monitoring
- Clear microprocessor restart after power up
- Processor reset at power down
- Reset output guaranteed down to V_{DD} = 1 V
- Low power consumption: typ. 3 μA at V_{DD} = 5 V
- On-chip oscillator
- No external components required
- Push-pull or Open drain output
- TO-92 and SOT-223 packages
- Pin compatible with DS 1233 A in TO-92

Description

The V 6310 monitors the supply voltage of any electronic systems, and generates the appropriate Reset signal. The gap between the two thresholds defines the allowed voltage range. As long as V_{DD} stays inside this voltage window, the output stays inactive. If V_{DD} drops below V_{THlow} or rises above V_{THhigh}, the output gets active. When V_{DD} enters into the allowed range, the output remains active for an additional 50 ms (typ.). This allows the system to stabilize before getting fully active. The lower threshold voltage may be obtained in different versions:

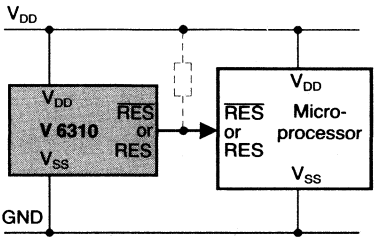
2.0 V to 6 V
2.4 V to 6 V
2.8 V to 6 V
3.5 V to 6 V
4.0 V to 6 V
4.5 V to 6 V

Applications

Any microprocessor application where an automatic restart is required:

- White / Brown goods
- Automotive electronics
- Industrial electronics
- Telecom systems
- Hand-held systems

Typical Operating Configuration



For Open drain version: – – – – –

Fig. 1

Pin Assignment

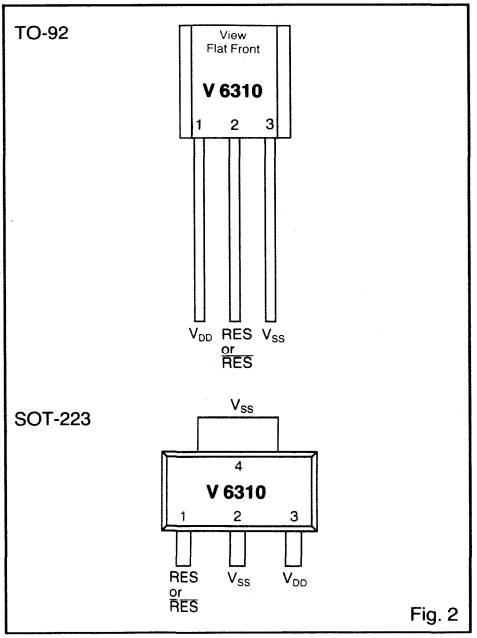


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to V_{SS}	V_{DD}	−0.3 V to +10 V
Min. voltage at RES or $\overline{RES}$	V_{min}	V_{SS} −0.3 V
Max. voltage at RES or $\overline{RES}$	V_{max}	V_{DD} +0.3 V
Storage temperature range	T_{STO}	−65° to +150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	1		8	V

Table 2

Electrical Characteristics

T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Min. at 25°C	Typ.	Max. at 25°C	Max.	Units
Supply current[1]	I_{DD}	V_{DD} = 2 V			1.5	2.1	3.1	µA
	I_{DD}	V_{DD} = 5 V			3	3.9	5.7	µA
	I_{DD}	V_{DD} = 8 V			5.2	6.8	10	µA
Threshold Low Voltage	V_{THlow}	Version: A, G, M	1.77	1.84	1.95	2.04	2.17	V
	V_{THlow}	Version: B, H, N	2.09	2.18	2.32	2.41	2.55	V
	V_{THlow}	Version: C, I, O	2.48	2.59	2.73	2.86	3.03	V
	V_{THlow}	Version: D, J, P	3.11	3.23	3.42	3.59	3.80	V
	V_{THlow}	Version: E, K, Q	3.55	3.70	3.88	4.08	4.32	V
	V_{THlow}	Version: F, L, R	4.05	4.22	4.42	4.67	4.95	V
Threshold High Voltage	V_{THhigh}		5.58	5.79	6.10	6.42	6.82	V
Threshold hysteresis	V_{HYS}				25			mV
RES Output Low Level	V_{OL}	V_{DD} = 5 V, I_{OL} = 8 mA			175		400	mV
	V_{OL}	V_{DD} = 3 V, I_{OL} = 4 mA			140		300	mV
	V_{OL}	V_{DD} = 1 V, I_{OL} = 50 µA			20		90	mV
RES Output High Level	V_{OH}	V_{DD} = 5 V, I_{OH} = −8 mA	4.3		4.5			V
	V_{OH}	V_{DD} = 3 V, I_{OH} = −4 mA	2.3		2.6			V
	V_{OH}	V_{DD} = 1 V, I_{OH} = −100 µA	850		950			mV
Output leakage current[2]	I_{LEAK}	V_{DD} = 8 V			0.05		1	µA

[1] RES or $\overline{RES}$ open

[2] Only for Open drain versions

Table 3

Timing Characteristics

V_{DD} = 5 V, T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power on Reset time	t_{POR}		25	50	75	ms
Sensitivity around V_{THhigh}	$t_{SENhigh}$	for V_{DD} = 5 V to 7 V in 5 µs	18	0.8 · t_{Rhigh}		µs
Sensitivity around V_{THlow}[3]	t_{SENlow}	for V_{DD} = 5 V to 3 V in 5 µs	20	0.8 · t_{Rlow}		µs
Reaction time around V_{THhigh}	t_{Rhigh}	for V_{DD} = 5 V to 7 V in 5 µs	20	55	90	µs
Reaction time around V_{THlow}[3]	t_{Rlow}	for V_{DD} = 5 V to 3 V in 5 µs	22	75	150	µs

[3] Tested on versions with V_{THlow} higher than 3 V

Table 4

Timing Waveforms

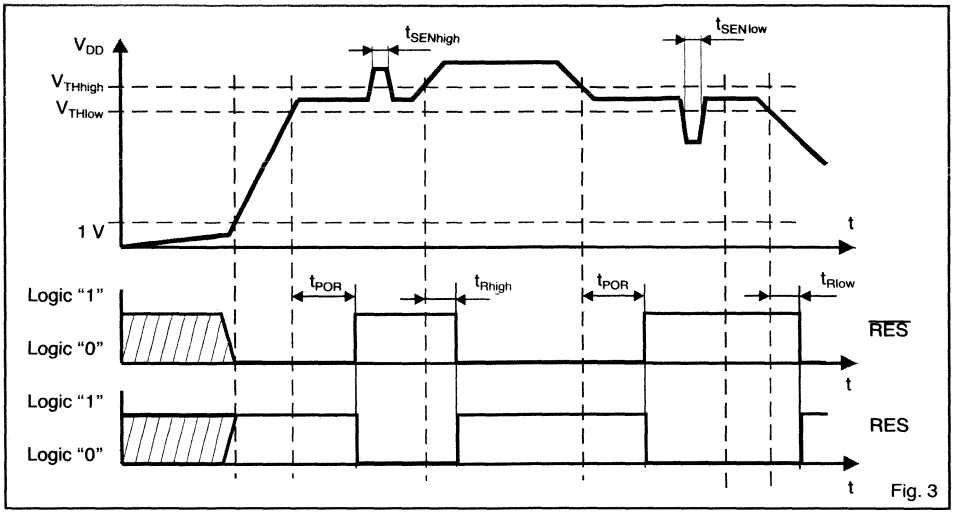


Fig. 3

Block Diagram

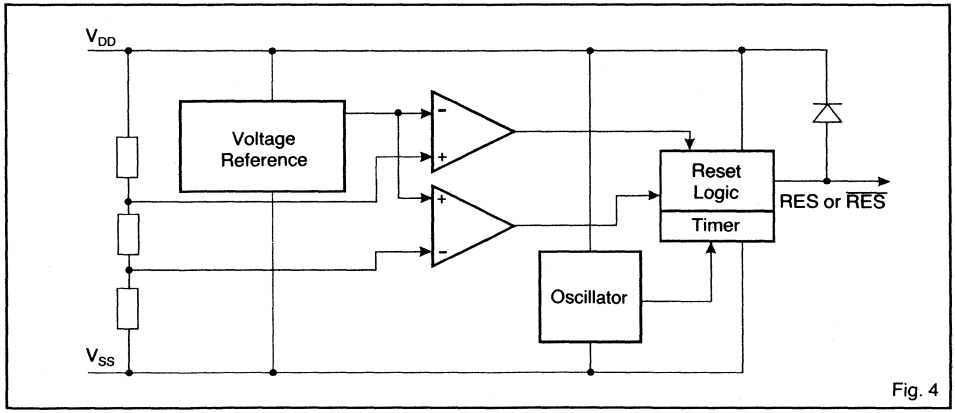


Fig. 4

Pin Description

TO-92

Pin	Name	Function
1	V_{DD}	Positive Supply
2	RES or $\overline{RES}$	Reset output
3	V_{SS}	Supply ground

Table 5

SOT-223

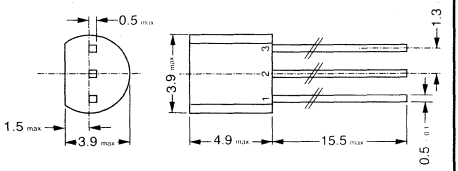
Pin	Name	Function
1	RES or $\overline{RES}$	Reset output
2	V_{SS}	Supply ground
3	V_{DD}	Positive Supply
4*	V_{SS}	Supply ground

* Internally connected to pin 2

Table 6

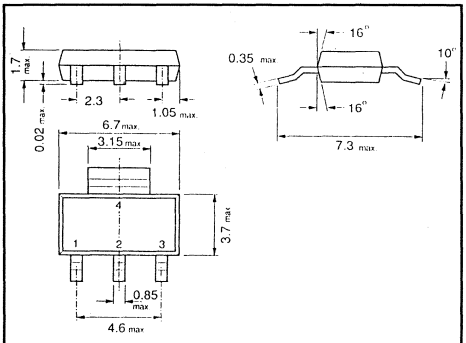
Package and Ordering Information

Dimensions of TO-92 Package



Dimensions in mm Fig. 6

Dimensions of SOT-223 Package



Dimensions in mm Fig. 7

Ordering Information

The V 6310 is available with Push-pull or Open drain output stage and Reset active low or high.

Ordering form: V 6310 <version letter> <packaging>

Example: Smart reset with:
- Reset active low
- Open drain output
- 2.8 V threshold
- TO-92 package

V 6310 O TO-92

When ordering, please specify the complete part number.

Version letter definition

Output stage	Threshold Voltage [V]					
	2.0	2.4	2.8	3.5	4	4.5
Push-pull, Reset active low	A*	B*	C*	D*	E*	F*
Push-pull, Reset active high	G*	H*	I*	J*	K*	L*
Open drain, Reset active low	M*	N*	O	P*	Q*	R*

* and Chip form, on request Table 7

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Smart Reset

Features

- Clear microprocessor restart after power up
- Processor reset at power down
- Reset output guaranteed down to V_{DD} = 1 V
- Low power consumption: typ. 3 μA at V_{DD} = 5 V
- On-chip oscillator
- No external components required
- Push-pull or Open drain output
- TO-92 package
- Pin compatible with MC 33064

Description

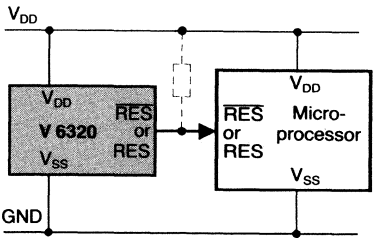
The V 6320 monitors the supply voltage of any electronic systems, and generates the appropriate Reset signal. The threshold defines the minimum allowed voltage which guarantees the good functionality of the system. As long as V_{DD} stays upside this voltage level, the output stays inactive. If V_{DD} drops below V_{TH}, the output gets active. When V_{DD} rises above V_{TH}, the output remains active for an additional 50 ms (typ.). This allows the system to stabilize before getting fully active. The threshold voltage may be obtained in different versions: 2 V, 2.4 V, 2.8 V, 3.5 V, 4 V, 4.5 V.

Applications

All microprocessor applications where an automatic restart is required:

- White / Brown goods
- Automotive electronics
- Industrial electronics
- Telecom systems
- Hand-held systems

Typical Operating Configuration



For Open drain version: – – – – – –

Fig. 1

Pin Assignment

TO-92

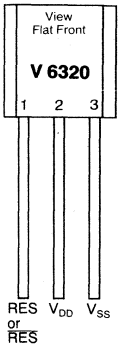


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to V_{SS}	V_{DD}	−0.3 V to +10 V
Min. voltage at RES or $\overline{RES}$	V_{min}	V_{SS} −0.3 V
Max. voltage at RES or $\overline{RES}$	V_{max}	V_{DD} +0.3 V
Storage temperature range	T_{STO}	−65°C to +150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	1		8	V

Table 2

Electrical Characteristics

T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Min. at 25°C	Typ.	Max. at 25°C	Max.	Units
Supply current[1]	I_{DD}	V_{DD} = 2 V			1.5	2.1	3.1	µA
	I_{DD}	V_{DD} = 5 V			3	3.9	5.7	µA
	I_{DD}	V_{DD} = 8 V			5.2	6.8	10	µA
Threshold voltage	V_{TH}	Version: A, G, M	1.77	1.84	1.95	2.04	2.17	V
	V_{TH}	Version: B, H, N	2.09	2.18	2.32	2.41	2.55	V
	V_{TH}	Version: C, I, O	2.48	2.59	2.73	2.86	3.03	V
	V_{TH}	Version: D, J, P	3.11	3.23	3.42	3.59	3.80	V
	V_{TH}	Version: E, K, Q	3.55	3.70	3.88	4.08	4.32	V
	V_{TH}	Version: F, L, R	4.05	4.22	4.42	4.67	4.95	V
Threshold hysteresis	V_{HYS}				25			mV
RES Output Low Level	V_{OL}	V_{DD} = 5 V, I_{OL} = 8 mA			175		400	mV
	V_{OL}	V_{DD} = 3 V, I_{OL} = 4 mA			140		300	mV
	V_{OL}	V_{DD} = 1 V, I_{OL} = 50 µA			20		90	mV
RES Output High Level	V_{OH}	V_{DD} = 5 V, I_{OH} = −8 mA	4.3		4.5			V
	V_{OH}	V_{DD} = 3 V, I_{OH} = −4 mA	2.3		2.6			V
	V_{OH}	V_{DD} = 1 V, I_{OH} = −100 µA	850		950			mV
Output leakage current[2]	I_{LEAK}	V_{DD} = 8 V			0.05		1	µA

[1] RES or $\overline{RES}$ open

[2] Only for Open drain versions

Table 3

Timing Characteristics

V_{DD} = 5 V, T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power on Reset time	t_{POR}		25	50	75	ms
Sensitivity[3]	t_{SEN}	for V_{DD} = 5 V to 3 V in 5 µs	20	0.8 · t_R		µs
Reaction time[3]	t_R	for V_{DD} = 5 V to 3 V in 5 µs	22	75	150	µs

[3] Tested on versions with V_{TH} higher than 3 V

Table 4

Timing Waveforms

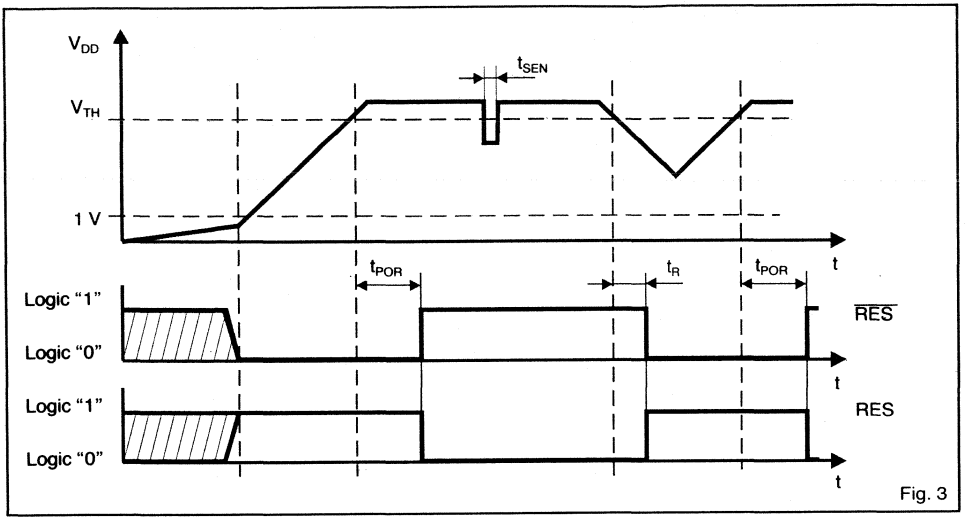


Fig. 3

Block Diagram

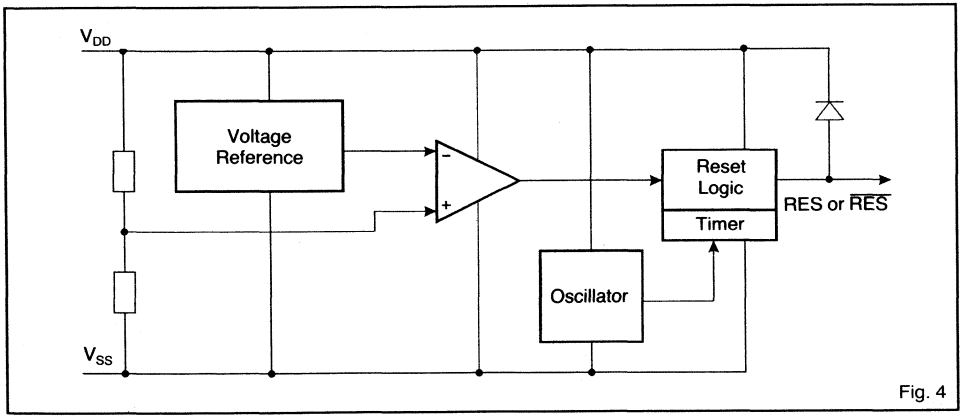


Fig. 4

Pin Description

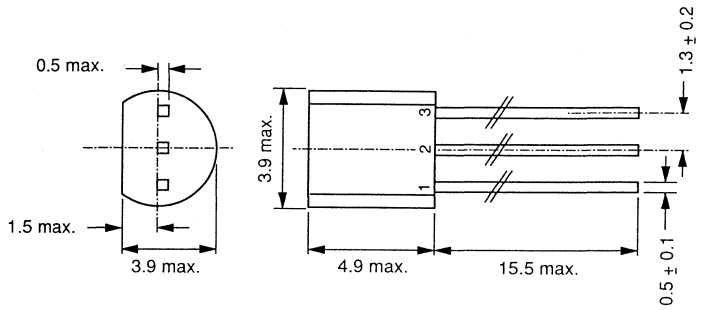
TO-92

Pin	Name	Function
1	RES or $\overline{RES}$	Reset output
2	V_{DD}	Positive Supply
3	V_{SS}	Supply ground

Table 5

Package and Ordering Information

Dimensions of TO-92 Package



Dimensions in mm

Fig. 6

Ordering Information

The V 6320 is available with Push-pull or Open drain output stage and Reset active low or high.

Ordering form: V 6320 <version letter> <packaging>

Example: Smart reset with:
- Reset active low
- Open drain output
- 4.5 V threshold
- TO-92 package

V 6320 R TO-92

When ordering, please specify the complete part number.

Version letter definition

Output stage	Threshold Voltage [V]					
	2.0	2.4	2.8	3.5	4	4.5
Push-pull, Reset active low	A*	B*	C*	D*	E*	F*
Push-pull, Reset active high	G*	H*	I*	J*	K*	L*
Open drain, Reset active low	M*	N*	O*	P	Q*	R

* and Chip form, on request

Table 6

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Smart Reset

Features

- Voltage Window monitoring
- Clear microprocessor restart after power up
- Processor reset at power down
- Reset output guaranteed down to V_{DD} = 1 V
- Low power consumption: typ. 3 μA at V_{DD} = 5 V
- On-chip oscillator
- No external components required
- Push-pull or Open drain output
- TO-92 package
- Pin compatible with MC 33064

Description

The V 6330 monitors the supply voltage of any electronic systems, and generates the appropriate Reset signal. The gap between the two thresholds defines the allowed voltage range. As long as V_{DD} stays inside this voltage window, the output stays inactive. If V_{DD} drops below V_{THlow} or rises above V_{THhigh}, the output gets active. When V_{DD} enters into the allowed range, the output remains active for an additional 50 ms (typ.). This allows the system to stabilize before getting fully active. The lower threshold voltage may be obtained in different versions:

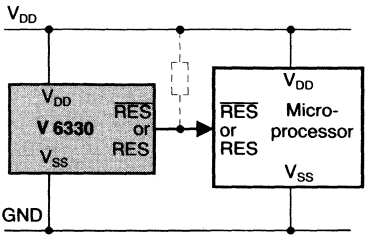
2.0 V to 6 V
2.4 V to 6 V
2.8 V to 6 V
3.5 V to 6 V
4.0 V to 6 V
4.5 V to 6 V

Applications

Any microprocessor application where an automatic restart is required:

- White / Brown goods
- Automotive electronics
- Industrial electronics
- Telecom systems
- Hand-held systems

Typical Operating Configuration



For Open drain version: – – – – –

Fig. 1

Pin Assignment

TO-92

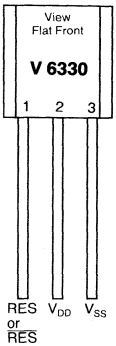


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to V_{SS}	V_{DD}	−0.3 V to +10 V
Min. voltage at RES or $\overline{RES}$	V_{min}	V_{SS} −0.3 V
Max. voltage at RES or $\overline{RES}$	V_{max}	V_{DD} +0.3 V
Storage temperature range	T_{STO}	−65° to +150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	1		8	V

Table 2

Electrical Characteristics

T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Min. at 25°C	Typ.	Max. at 25°C	Max.	Units
Supply current[1]	I_{DD}	V_{DD} = 2 V			1.5	2.1	3.1	µA
	I_{DD}	V_{DD} = 5 V			3	3.9	5.7	µA
	I_{DD}	V_{DD} = 8 V			5.2	6.8	10	µA
Threshold Low Voltage	V_{THlow}	Version: A, G, M	1.77	1.84	1.95	2.04	2.17	V
	V_{THlow}	Version: B, H, N	2.09	2.18	2.32	2.41	2.55	V
	V_{THlow}	Version: C, I, O	2.48	2.59	2.73	2.86	3.03	V
	V_{THlow}	Version: D, J, P	3.11	3.23	3.42	3.59	3.80	V
	V_{THlow}	Version: E, K, Q	3.55	3.70	3.88	4.08	4.32	V
	V_{THlow}	Version: F, L, R	4.05	4.22	4.42	4.67	4.95	V
Threshold High Voltage	V_{THhigh}		5.58	5.79	6.10	6.42	6.82	V
Threshold hysteresis	V_{HYS}				25			mV
RES Output Low Level	V_{OL}	V_{DD} = 5 V, I_{OL} = 8 mA			175		400	mV
	V_{OL}	V_{DD} = 3 V, I_{OL} = 4 mA			140		300	mV
	V_{OL}	V_{DD} = 1 V, I_{OL} = 50 µA			20		90	mV
RES Output High Level	V_{OH}	V_{DD} = 5 V, I_{OH} = −8 mA	4.3		4.5			V
	V_{OH}	V_{DD} = 3 V, I_{OH} = −4 mA	2.3		2.6			V
	V_{OH}	V_{DD} = 1 V, I_{OH} = −100 µA	850		950			mV
Output leakage current[2]	I_{LEAK}	V_{DD} = 8 V			0.05		1	µA

[1] RES or $\overline{RES}$ open

[2] Only for Open drain versions

Table 3

Timing Characteristics

V_{DD} = 5 V, T_A = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power on Reset time	t_{POR}		25	50	75	ms
Sensitivity around V_{THhigh}	$t_{SENhigh}$	for V_{DD} = 5 V to 7 V in 5 µs	18	0.8 · t_{Rhigh}		µs
Sensitivity around V_{THlow}[3]	t_{SENlow}	for V_{DD} = 5 V to 3 V in 5 µs	20	0.8 · t_{Rlow}		µs
Reaction time around V_{THhigh}	t_{Rhigh}	for V_{DD} = 5 V to 7 V in 5 µs	20	55	90	µs
Reaction time around V_{THlow}[3]	t_{Rlow}	for V_{DD} = 5 V to 3 V in 5 µs	22	75	150	µs

[3] Tested on versions with V_{THlow} higher than 3 V

Table 4

Timing Waveforms

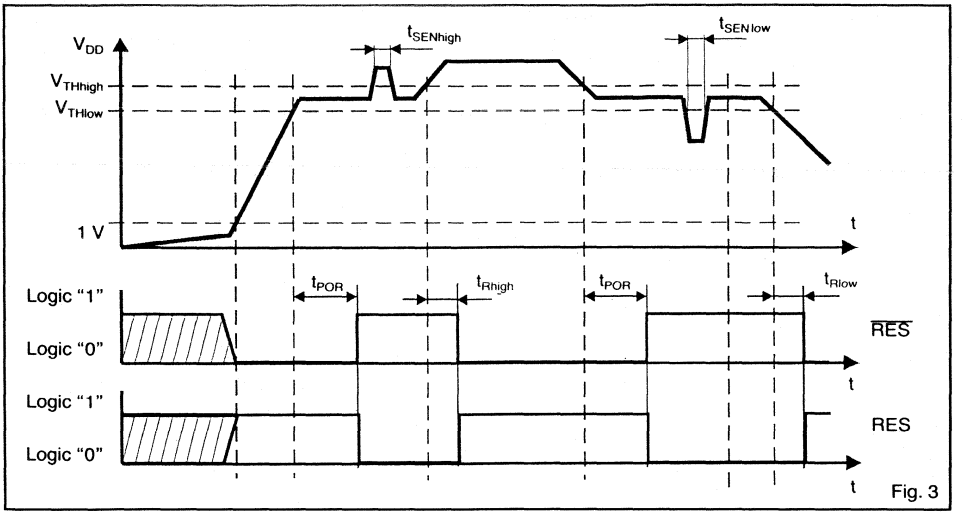


Fig. 3

Block Diagram

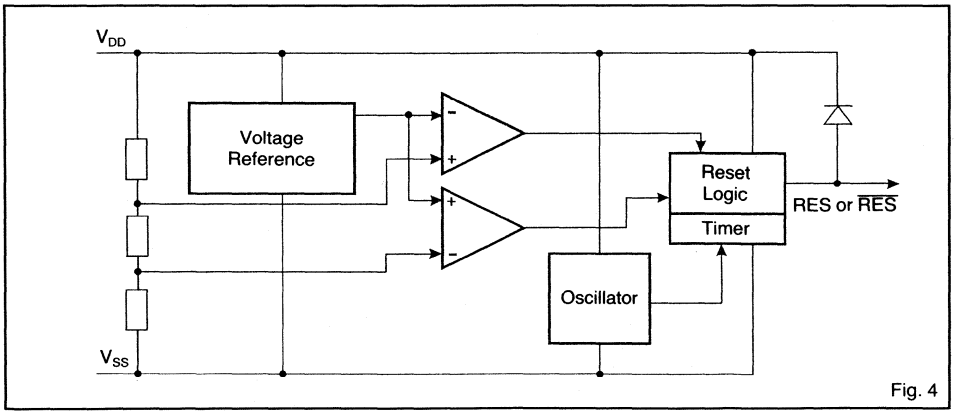


Fig. 4

Pin Description

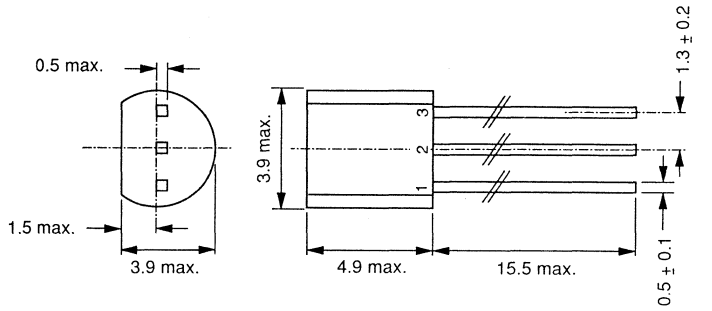
TO 92

Pin	Name	Function
1	RES or $\overline{RES}$	Reset output
2	V_{DD}	Positive Supply
3	V_{SS}	Supply ground

Table 5

Package and Ordering Information

Dimensions of TO-92 Package



Dimensions in mm

Fig. 6

Ordering Information

The V 6330 is available with Push-pull or Open drain output stage and Reset active low or high.

Ordering form: V 6330 <version letter> <packaging>

Example: Smart reset with: - Reset active low
- Open drain output
- 3.5 V threshold
- TO-92 package

V 6330 P TO-92

When ordering, please specify the complete part number.

Version letter definition

Output stage	Threshold Voltage [V]					
	2.0	2.4	2.8	3.5	4	4.5
Push-pull, Reset active low	A*	B*	C*	D*	E*	F*
Push-pull, Reset active high	G*	H*	I*	J*	K*	L*
Open drain, Reset active low	M*	N*	O*	P	Q*	R*

* and Chip form, on request

Table 6

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Table of Contents

Regulator & Watchdog

Features

- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 250 mV at 100 mA
- Low quiescent current, typically 155 μA
- Standby mode, maximum current 240 μA (without load on OUTPUT)
- Unregulated DC input can withstand −20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 3.0 V
- Reset output guaranteed for regulated output voltage down to 1.2 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Comparator for voltage monitoring, reset threshold 1.17V
- ± 1.5% voltage threshold tolerance at 25°C
- ± 3% voltage threshold tolerance from −40 to +70°C
- Programmable reset voltage monitoring
- Programmable power on reset (POR) delay
- Watchdog with programmable time windows guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ±10%
- System enable output offers added security
- TTL/CMOS compatible
- −40°C to +70°C temperature range
- DIP8 and SO8 packages

Description

The A 6130 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring in an 8 lead package. The voltage regulator has a low dropout voltage (typ. 250 mV at 100 mA) and a low quiescent current (155 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage transient of −20 V (reverse battery). The input may be connected to ground or a reverse voltage without reverse current flow from the output to the input. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies

Typical Operating Configuration

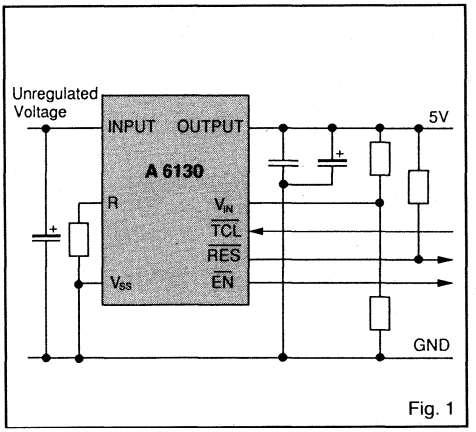


Fig. 1

Pin Assignment

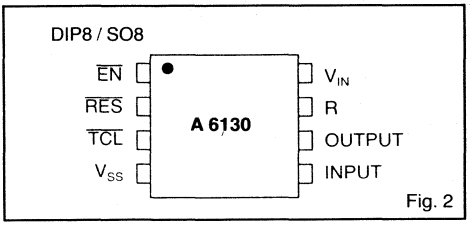


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	−0.3 to +30 V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	−20 to +60 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+70	°C
INPUT voltage [1]	V_{INPUT}	3.36		26	V
OUTPUT voltage [1)2)]	V_{OUTPUT}	3.0			V
$\overline{RES}$ & $\overline{EN}$ guaranteed [3]	V_{OUTPUT}	1.2			V
OUTPUT current [4]	I_{OUTPUT}			100	mA
Comparator input voltage	V_{IN}	0		V_{OUTPUT}	V
RC-oscillator programming	R	10		1000	kΩ
Thermal resistance from junction to ambient [5]					
– DIP8	$R_{th(j-a)}$			105	°C/W
– SO8	$R_{th(j-a)}$			160	°C/W

Table 2

1) Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 µF capacitor or greater is required on the INPUT, see Fig. 8. The 22 µF must have an effective resistance ≤ 5 Ω and a resonant frequency above 500 kHz.

2) A 10 µF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 µF must have an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

3) $\overline{RES}$ must be pulled up externally to V_{OUTPUT} even if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

4) The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A 6130 to work above the maximum junction temperature (70°C) must be avoided.

5) The thermal resistance specified assumes the package is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 100 µA			240	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 µA		155	300	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1MΩ to V_{OUTPUT}, I_L = 100 mA		1.7	4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88		5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA, −40°C ≤ T_J ≤ 70°C	4.85		5.15	V
Output voltage temperature coefficient [2]	$V_{th(coeff)}$			50	180	ppm/°C
Line regulation [3]	V_{LINE}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = 70°C		0.2	0.5	%
Load regulation [3]	V_L	100 µA ≤ I_L ≤ 100 mA		0.2	0.6	%
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 µA		40	170	mV
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 mA			420	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, I_L = 100 µA, R_{EXT} = 100 kΩ, O/Ps 1 MΩ to V_{OUTPUT}, I/Ps at V_{OUTPUT}		300	560	µA
Thermal regulation [5]	V_{thr}	T_J = 25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms		0.05	0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}			450	mA
OUTPUT noise, 10Hz to 100kHz	V_{NOISE}			200		µV rms

3.0 ≤ V_{OUTPUT} ≤ 5.5 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

$\overline{RES}$ and $\overline{EN}$						
Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$						
Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{OUTPUT} = 2.0 V, I_{OH} = −100 µA	1.8	1.9		V
	V_{OH}	V_{OUTPUT} = 1.2 V, I_{OH} = −30 µA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}		2.0		V_{OUTPUT}	V
Leakage current $\overline{TCL}$ input	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference [6] [7]	V_{REF}	T_J = 25°C	1.148	1.170	1.200	V
	V_{REF}	−20°C ≤ T_J ≤ 70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis [7]	V_{HY}			2		mV

Table 3

[1] If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A 6130.
[2] The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
[3] Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.
[4] The dropout voltage is defined as the INPUT to OUTPUT voltage differential at which the OUTPUT voltage drops 100 mV below its nominal measured at a 1 V differential.
[5] Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.
[6] The comparator and the voltage regulator have separate voltage references (see "Block Diagram" Fig. 7).
[7] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 4).

Timing Characteristics

V_{INPUT} = 6.0 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
TCL to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

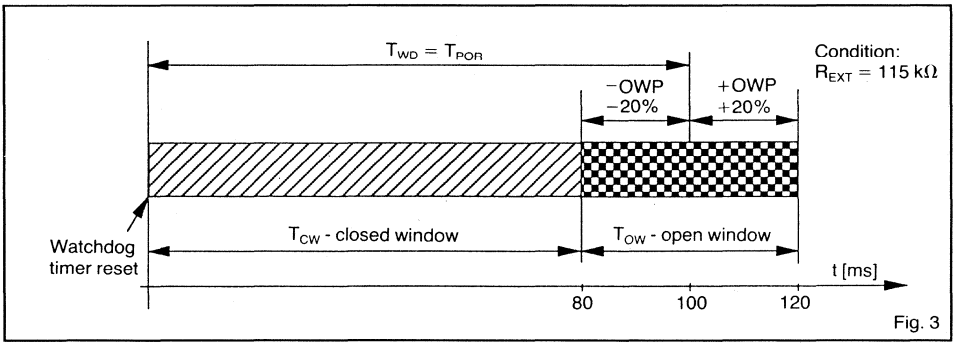


Fig. 3

Voltage Monitoring

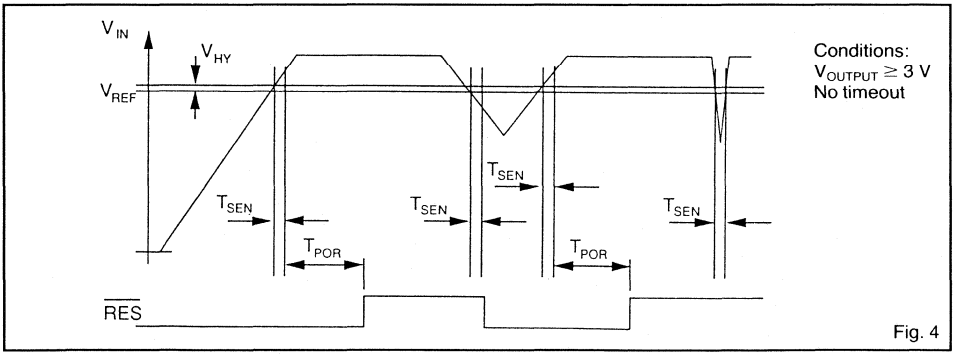


Fig. 4

Timer Reaction

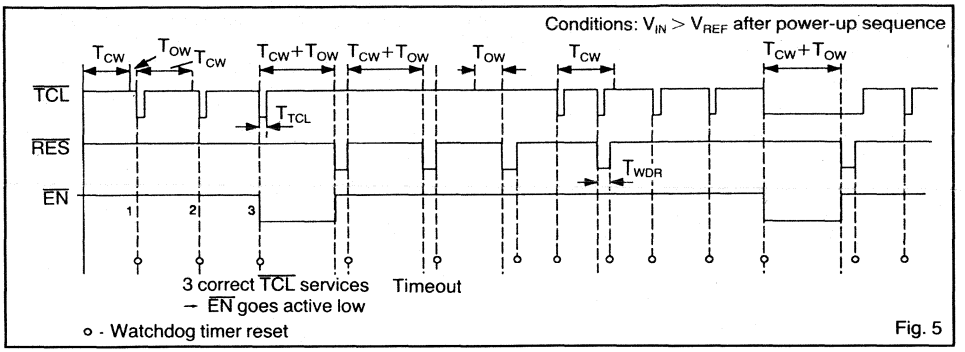


Fig. 5

Combined Voltage and Timer Reaction

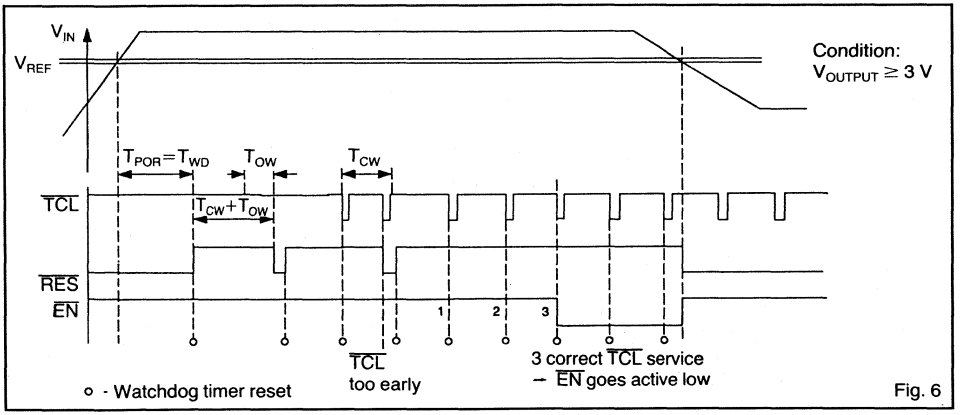


Fig. 6

Block Diagram

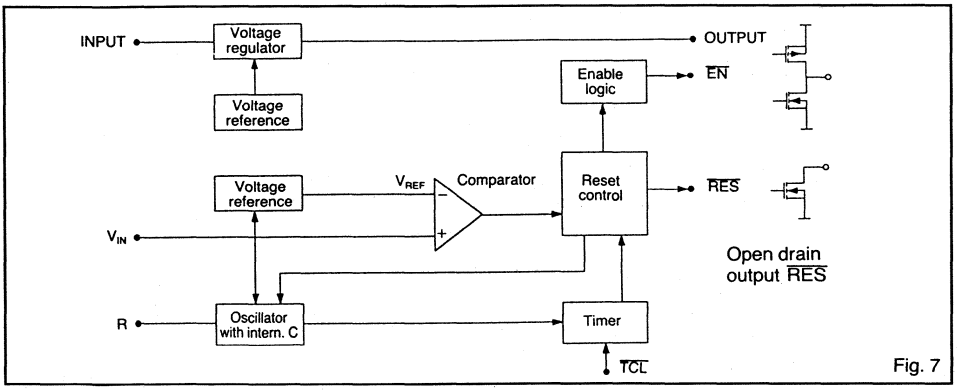


Fig. 7

Pin Description

Pin	Name	Function
1	$\overline{EN}$	Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	INPUT	Voltage regulator input
6	OUTPUT	Voltage regulator output
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

Voltage Regulator

The A 6130 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 155 μA) makes the A 6130 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 3.36 V to 26 V for operation and the input protection includes both reverse battery (negative transients up to 20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 8). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about −30°C, so tantalums are recommended for operation below −25°C. The important parameters of the 22 μF capacitor are an effective series resistance of $\leq 5\ \Omega$ and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A 6130 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Care must be taken not to exceed the maximum junction temperature (+70°C). The power dissipation within the A 6130 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (70°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (ie. ≥ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A 6130 in DIP8 package will have an effective thermal resistance from the junction to the ambient of about 10°C/W for a single 100 ms pulse.

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 8. The user uses the external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 4). After INPUT reaches 3.36 V (and so OUTPUT reaches at least 3 V) and V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 8) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 115 kΩ typical values are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 3) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if $T_{WD} = 100$ ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms ($T_{CW} = 80$ ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically $R_{EXT} \times 0.87$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if $R_{EXT} = 115$ kΩ then $T_{WD} = 100$ ms ±10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ − 2.5 ms typically (see Fig. 5).

With the open window constraint new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset.

If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though software is malfunctioning; the A 6130 would make a system reset because the watchdog would be cleared too quickly.

If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 8).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 µs overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable − $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The A 6130 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

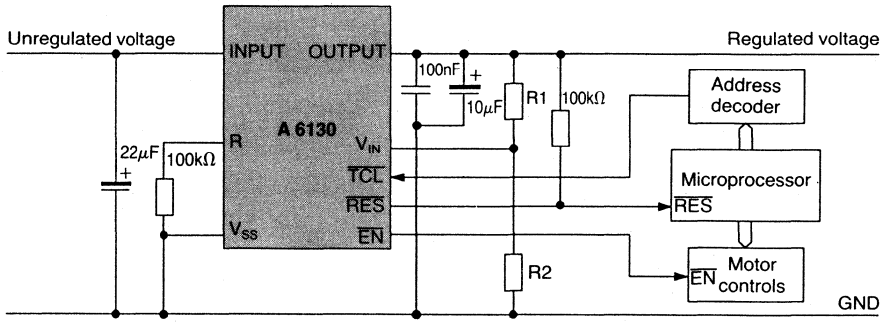


Fig. 8

OUTPUT Current versus INPUT Voltage

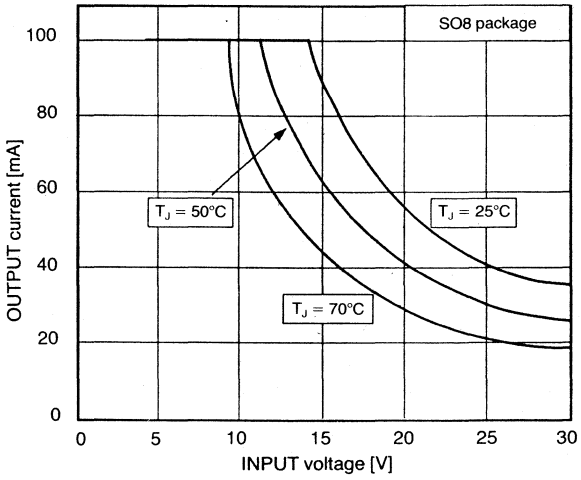


Fig. 9

T_{WD} versus Temperature at 5 V

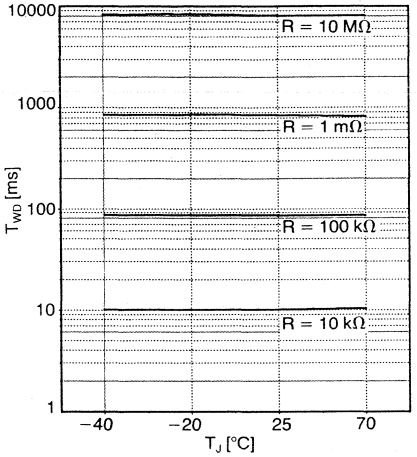


Fig. 10

T_{WD} versus R at 5 V

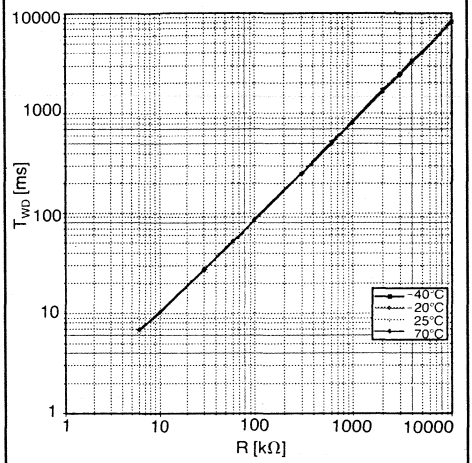


Fig. 11

T_{WD} versus V_{OUTPUT} at T_J = +25°C

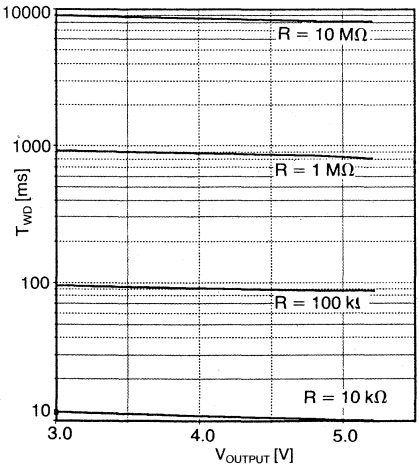


Fig. 12

T_{WD} versus R at T_J = +25°C

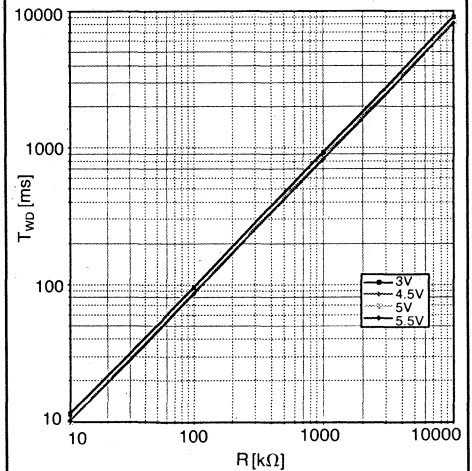


Fig. 13

8

T_{WD} versus R at $T_J = +25°C$

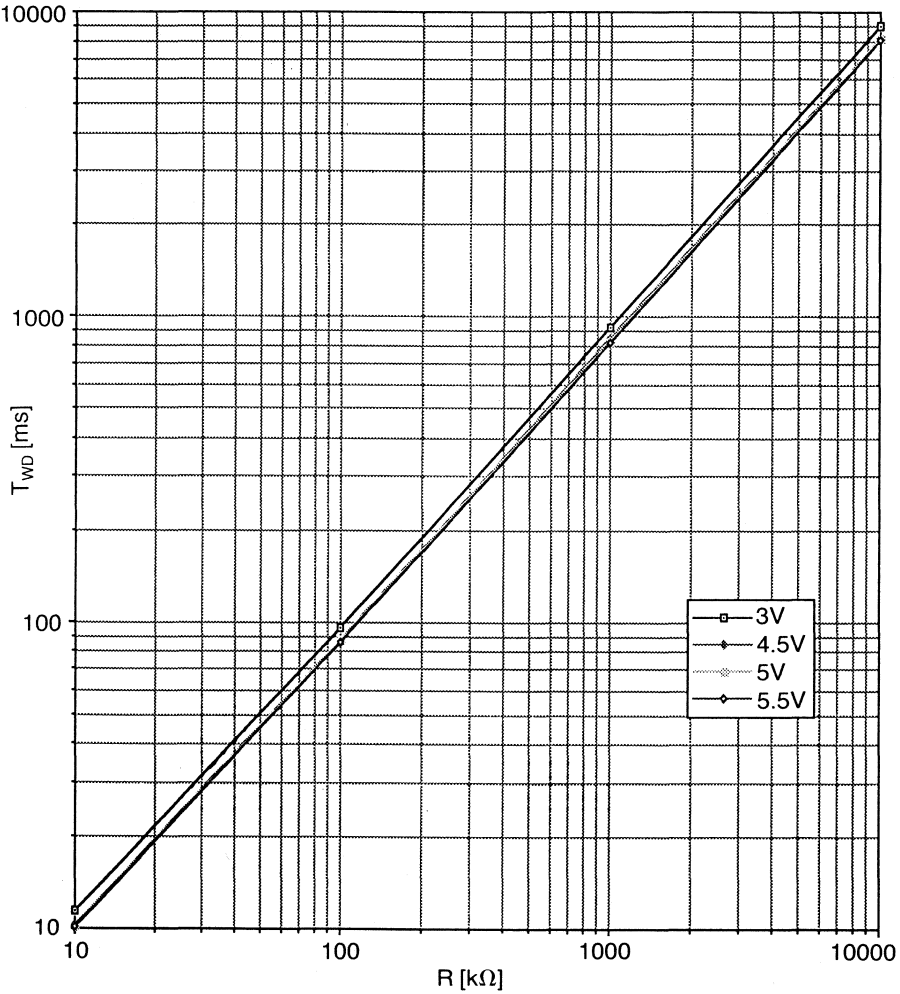


Fig. 14

T_{WD} versus V_{OUTPUT} at $T_J = +70°C$

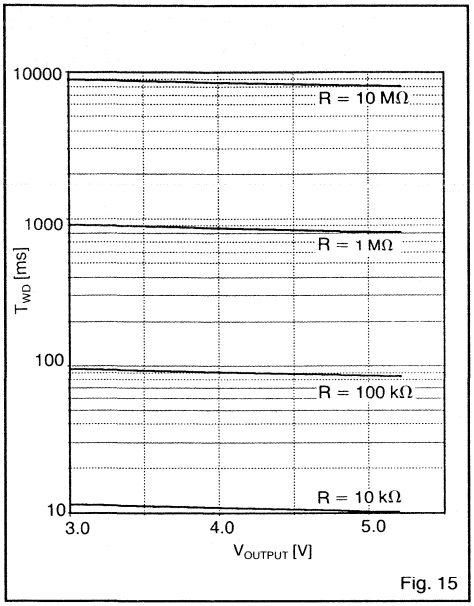


Fig. 15

T_{WD} versus R at $T_J = +70°C$

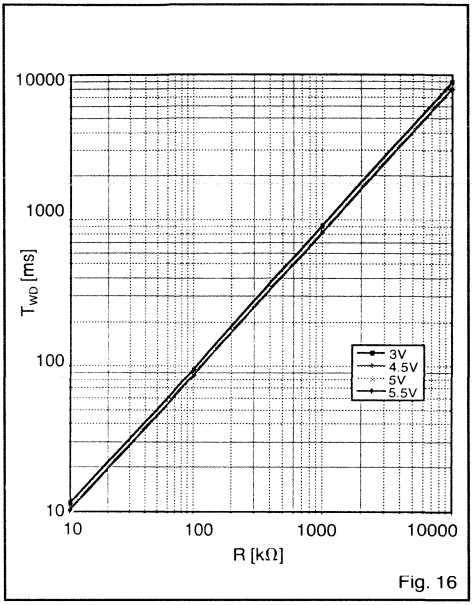


Fig. 16

T_{WD} versus V_{OUTPUT} at $T_J = -40°C$

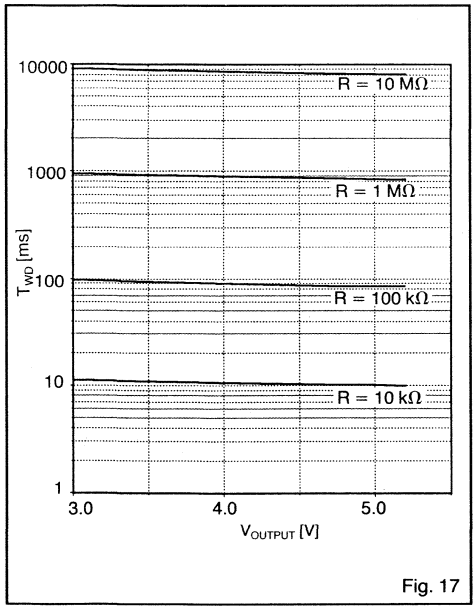


Fig. 17

T_{WD} versus R at $T_J = -40°C$

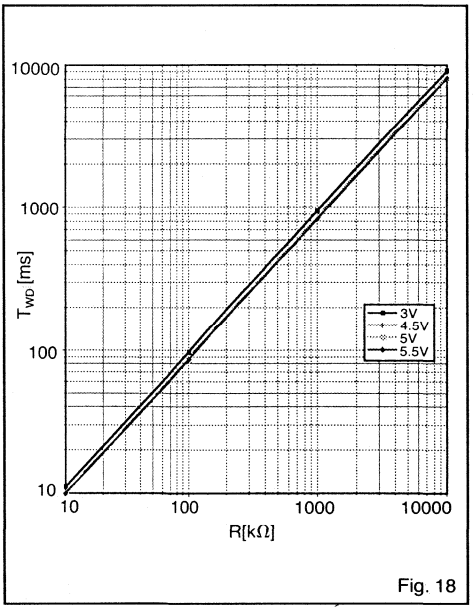
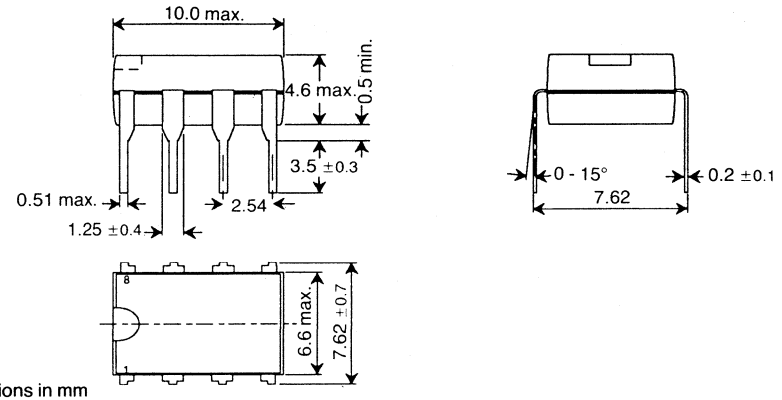


Fig. 18

8

Package and Ordering Information

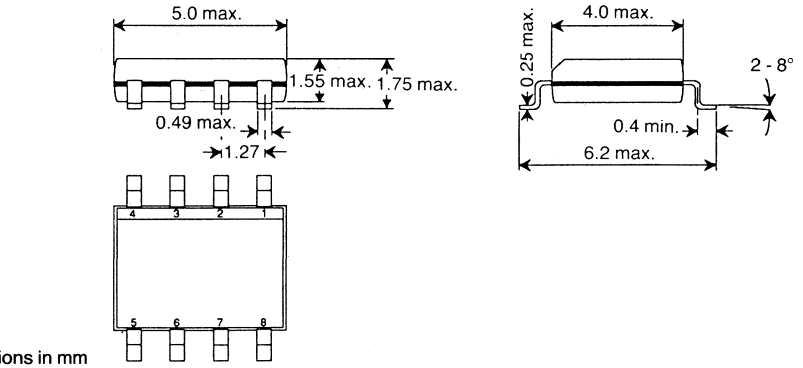
Dimensions of DIP8 Package



Dimensions in mm

Fig. 19

Dimensions of SO8 Package



Dimensions in mm

Fig. 20

Ordering Information

The A 6130 is available in the following packages:

Type	Package
A 6130 8P	DIP8
A 6130 8S	SO8

When ordering please specify complete part number.

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A 6133

Regulator & Watchdog

Features

- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 250 mV at 100 mA
- Low quiescent current, typically 155 μA
- Standby mode, maximum current 240 μA (without load on OUTPUT)
- Unregulated DC input can withstand −20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 3.0 V
- Reset output guaranteed for regulated output voltage down to 1.2 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Comparator for voltage monitoring, reset threshold 1.17V
- ± 1.5% voltage threshold tolerance at 25°C
- ± 3% voltage threshold tolerance from −40 to +70°C
- Programmable reset voltage monitoring
- Programmable power on reset (POR) delay
- Watchdog with programmable time windows guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ±10%
- System enable output offers added security
- 3 chip select feed-thru circuit controlled by $\overline{EN}$
- TTL/CMOS compatible
- −40°C to +70°C temperature range
- DIP14 and SO14 packages

Description

The A 6133 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring in an 14 lead package. The voltage regulator has a low dropout voltage (typ. 250 mV at 100 mA) and a low quiescent current (155 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage transient of −20 V (reverse battery). The input may be connected to ground or a reverse voltage without reverse current flow from the output to the input. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies

Typical Operating Configuration

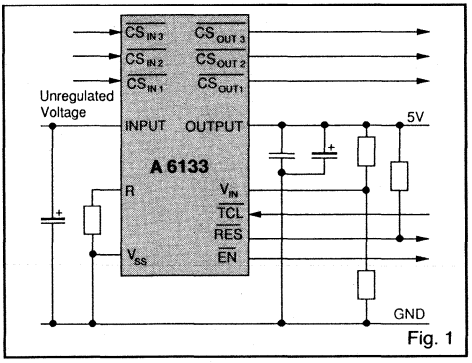


Fig. 1

Pin Assignment

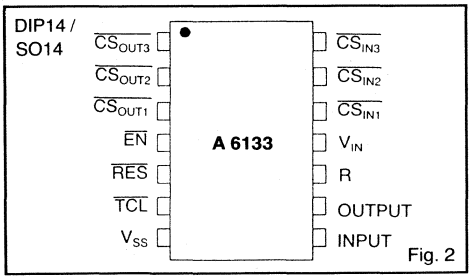


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	−0.3 to +30 V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	−20 to +60 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+70	°C
INPUT voltage [1]	V_{INPUT}	3.36		26	V
OUTPUT voltage [1)2)]	V_{OUTPUT}	3.0			V
$\overline{RES}$ & $\overline{EN}$ guaranteed [3]	V_{OUTPUT}	1.2			V
OUTPUT current [4]	I_{OUTPUT}			100	mA
Comparator input voltage	V_{IN}	0		V_{OUTPUT}	V
RC-oscillator programming	R	10		1000	kΩ
Thermal resistance from junction to ambient [5]					
– DIP14	$R_{th(j-a)}$			100	°C/W
– SO14	$R_{th(j-a)}$			150	°C/W

Table 2

1) Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 µF capacitor or greater is required on the INPUT, see Fig. 9. The 22 µF must have an effective resistance ≤ 5 Ω and a resonant frequency above 500 kHz.

2) A 10 µF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 µF must have an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

3) $\overline{RES}$ must be pulled up externally to V_{OUTPUT} even if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

4) The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A 6133 to work above the maximum junction temperature (70°C) must be avoided.

5) The thermal resistance specified assumes the package is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 100 µA			240	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 µA		155	300	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 mA		1.7	4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88		5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA, −40°C ≤ T_J ≤ 70°C	4.85		5.15	V
Output voltage temperature coefficient [2]	$V_{th(coeff)}$			50	180	ppm/°C
Line regulation [3]	V_{LINE}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = 70°C		0.2	0.5	%
Load regulation [3]	V_L	100 µA ≤ I_L ≤ 100 mA		0.2	0.6	%
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 µA		40	170	mV
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 mA			420	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, I_L = 100 µA, R_{EXT} = 100 kΩ, O/Ps 1 MΩ to V_{OUTPUT}, I/Ps at V_{OUTPUT}		300	560	µA
Thermal regulation [5]	V_{thr}	T_J = 25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms		0.05	0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}			450	mA
OUTPUT noise, 10Hz to 100kHz	V_{NOISE}			200		µV rms

3.0 ≤ V_{OUTPUT} ≤ 5.5 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

$\overline{RES}$, $\overline{EN}$ and $\overline{CS}_{OUT1/2/3}$						
Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$ and $\overline{CS}_{OUT1/2/3}$						
Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{OUTPUT} = 2.0 V, I_{OH} = −100 µA	1.8	1.9		V
	V_{OH}	V_{OUTPUT} = 1.2 V, I_{OH} = −30 µA	1.0	1.1		V
$\overline{TCL}$, V_{IN} and $\overline{CS}_{IN1/2/3}$						
$\overline{TCL}$ and $\overline{CS}_{IN1/2/3}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ and $\overline{CS}_{IN1/2/3}$ Input High Level	V_{IH}		2.0		V_{OUTPUT}	V
Leakage current $\overline{TCL}$ input	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference [6] [7]	V_{REF}	T_J = 25°C	1.148	1.170	1.200	V
	V_{REF}	T_J = −20°C to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis [7]	V_{HY}			2		mV

Table 3

[1] If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A 6133.
[2] The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
[3] Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.
[4] The dropout voltage is defined as the INPUT to OUTPUT voltage differential at which the OUTPUT voltage drops 100 mV below its nominal measured at a 1 V differential.
[5] Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.
[6] The comparator and the voltage regulator have separate voltage references (see "Block Diagram" Fig. 8).
[7] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

8

Timing Characteristics

V_{INPUT} = 6.0 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at rising edge	T_{CSH}			125	200	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at falling edge	T_{CSL}			75	150	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

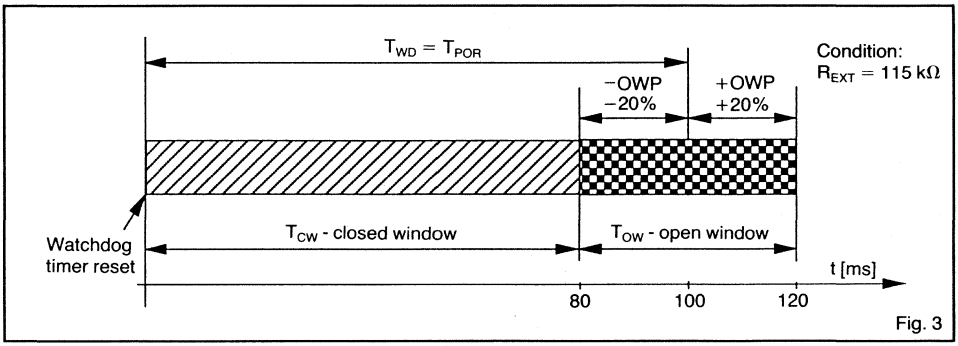


Fig. 3

Chip Select

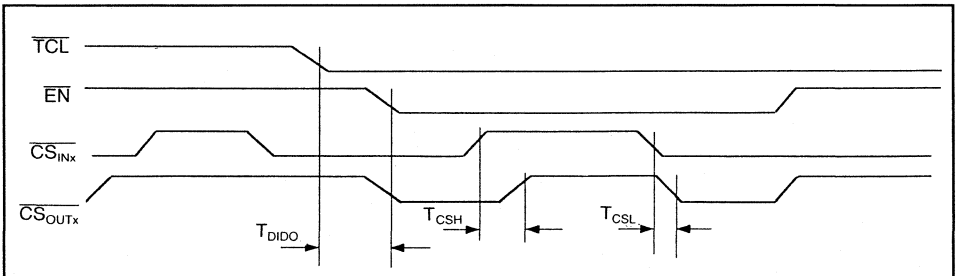


Fig. 4

Voltage Monitoring

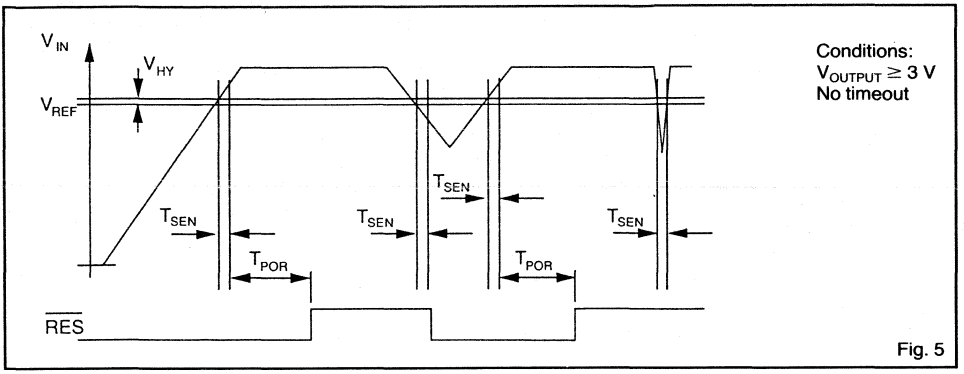


Fig. 5

Timer Reaction

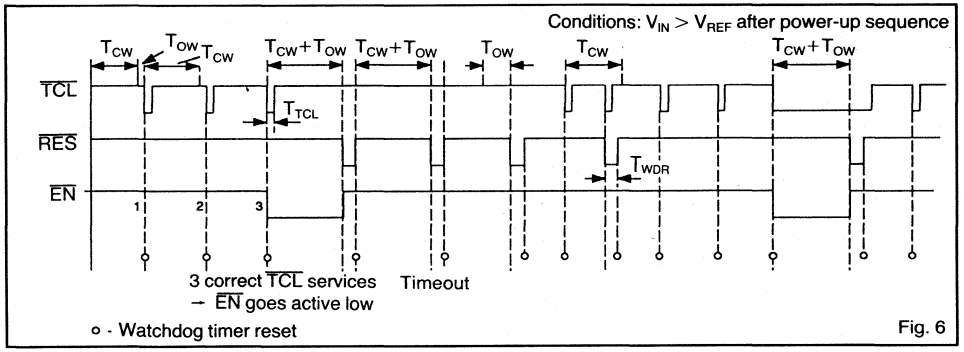


Fig. 6

Combined Voltage and Timer Reaction

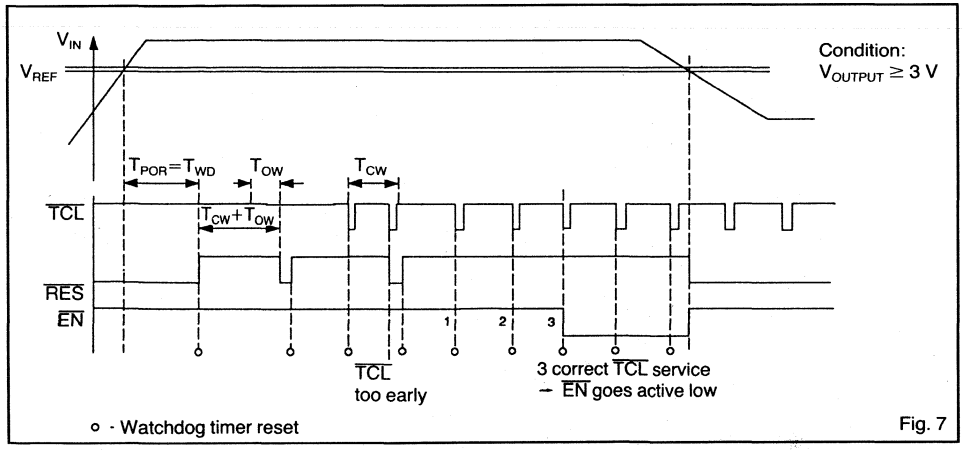


Fig. 7

Block Diagram

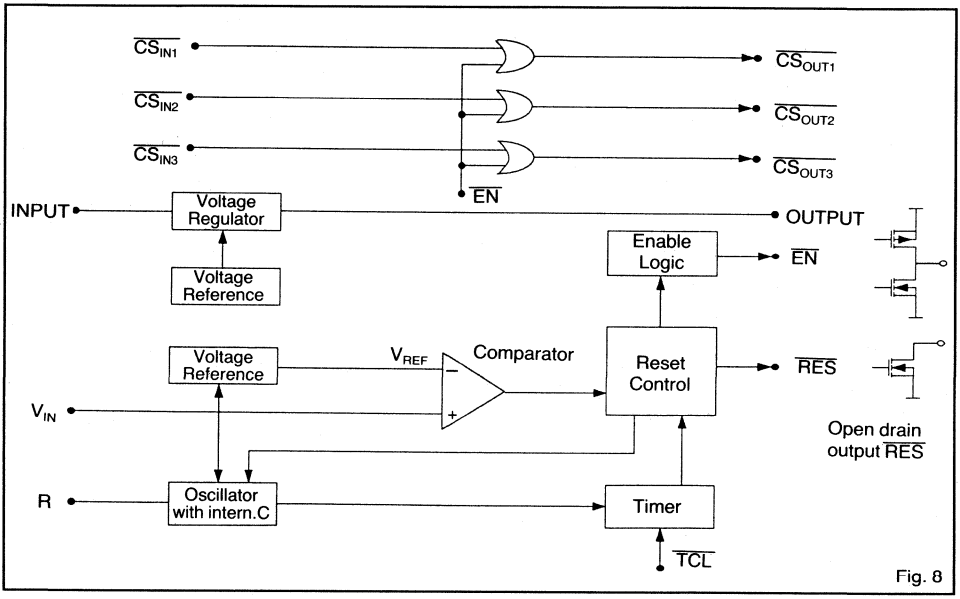


Fig. 8

Pin Description

Pin	Name	Function
1	$\overline{CS}_{OUT3}$	Push-pull active low chip select output 3
2	$\overline{CS}_{OUT2}$	Push-pull active low chip select output 2
3	$\overline{CS}_{OUT1}$	Push-pull active low chip select output 1
4	$\overline{EN}$	Push-pull active low enable output
5	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
6	$\overline{TCL}$	Watchdog timer clear input signal
7	V_{SS}	GND terminal
8	INPUT	Voltage regulator input
9	OUTPUT	Voltage regulator output
10	R	R_{EXT} input for RC oscillator tuning
11	V_{IN}	Voltage comparator input
12	$\overline{CS}_{IN1}$	Chip select input 1
13	$\overline{CS}_{IN2}$	Chip select input 2
14	$\overline{CS}_{IN3}$	Chip select input 3

Table 5

Functional Description

Voltage Regulator

The A 6133 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 155 μA) makes the A 6133 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 3.36 V to 26 V for operation and the input protection includes both reverse battery (negative transients up to 20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 9). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about −30°C, so tantalums are recommended for operation below −25°C. The important parameters of the 22 μF capacitor are an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A 6133 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Care must be taken not to exceed the maximum junction

temperature (+70°C). The power dissipation within the A 6133 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (70°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (ie. ≥ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A 6133 in DIP14 package will have an effective thermal resistance from the junction to the ambient of about 9°C/W for a single 100 ms pulse.

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 9. The user uses the external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5). After INPUT reaches 3.36 V (and so OUTPUT reaches at least 3 V) and V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of RES even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 µs.

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 115 kΩ typical values are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 3) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal TCL during the open window: Typically R_{EXT} x 0.87 where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 115 kΩ then T_{WD} = 100 ms ±10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 6)

With the open window constraint new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though software is malfunctioning; the A 6133 would make a system reset because the watchdog would be cleared too quickly.

If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 9).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs,

$\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable – $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low. A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The A 6133 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

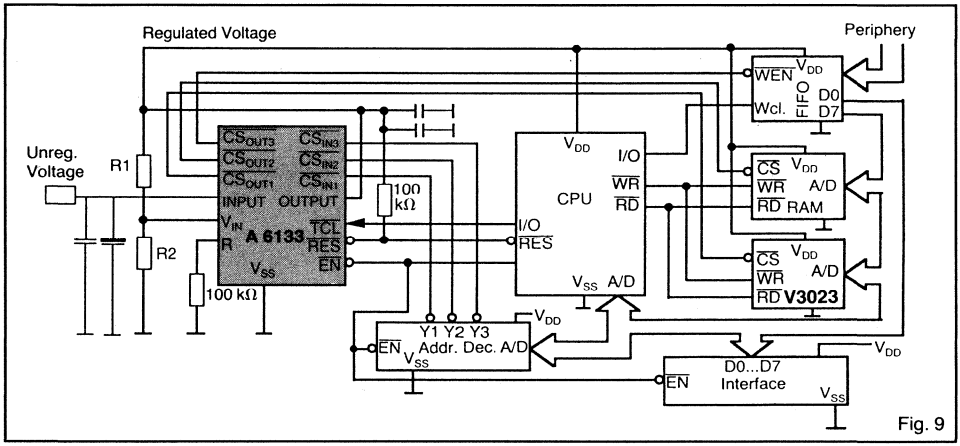


Fig. 9

OUTPUT Current Versus INPUT Voltage

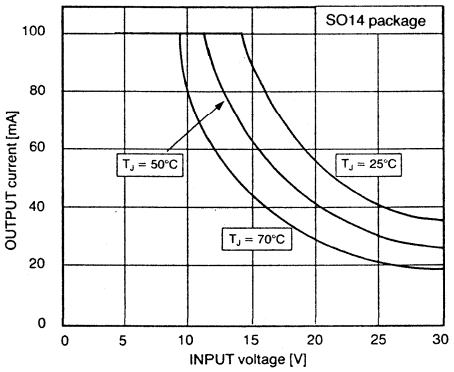


Fig. 10

T_{WD} versus Temperature at 5 V

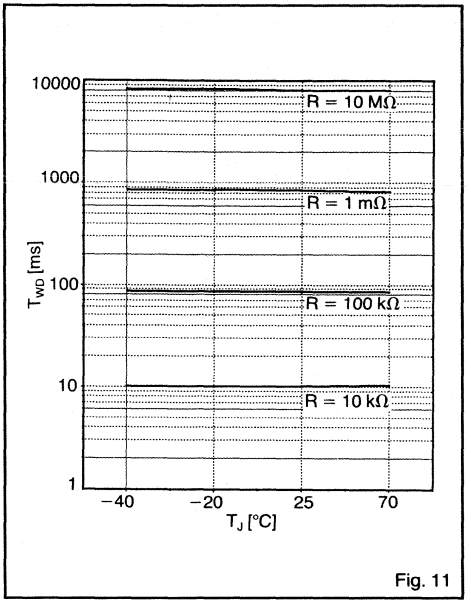


Fig. 11

T_{WD} versus R at 5 V

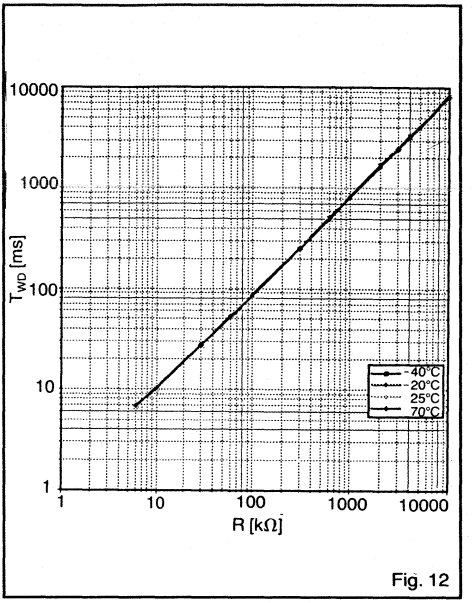


Fig. 12

T_{WD} versus V_{OUTPUT} at T_J = +25°C

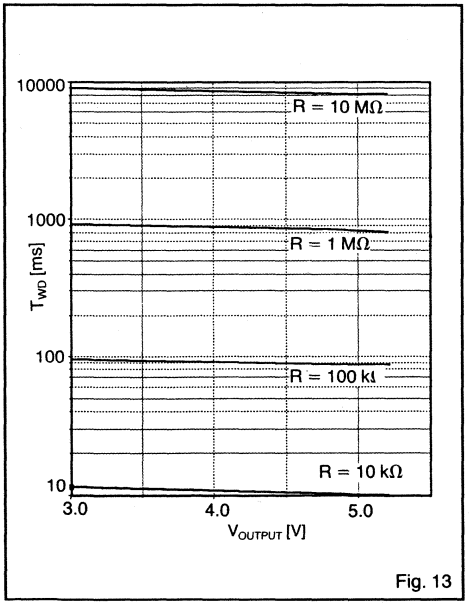


Fig. 13

T_{WD} versus R at T_J = +25°C

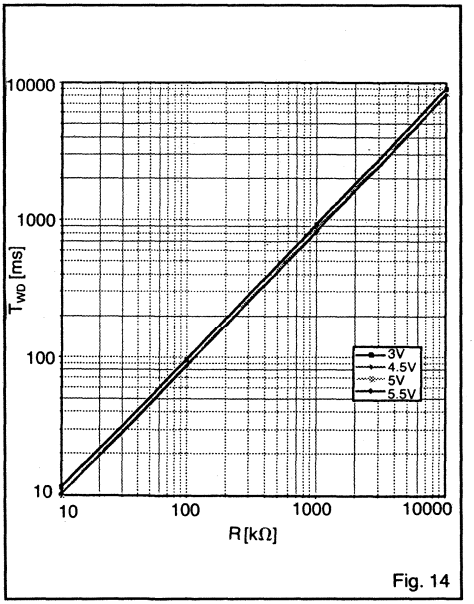


Fig. 14

8

T_{WD} versus R at T_J = +25°C

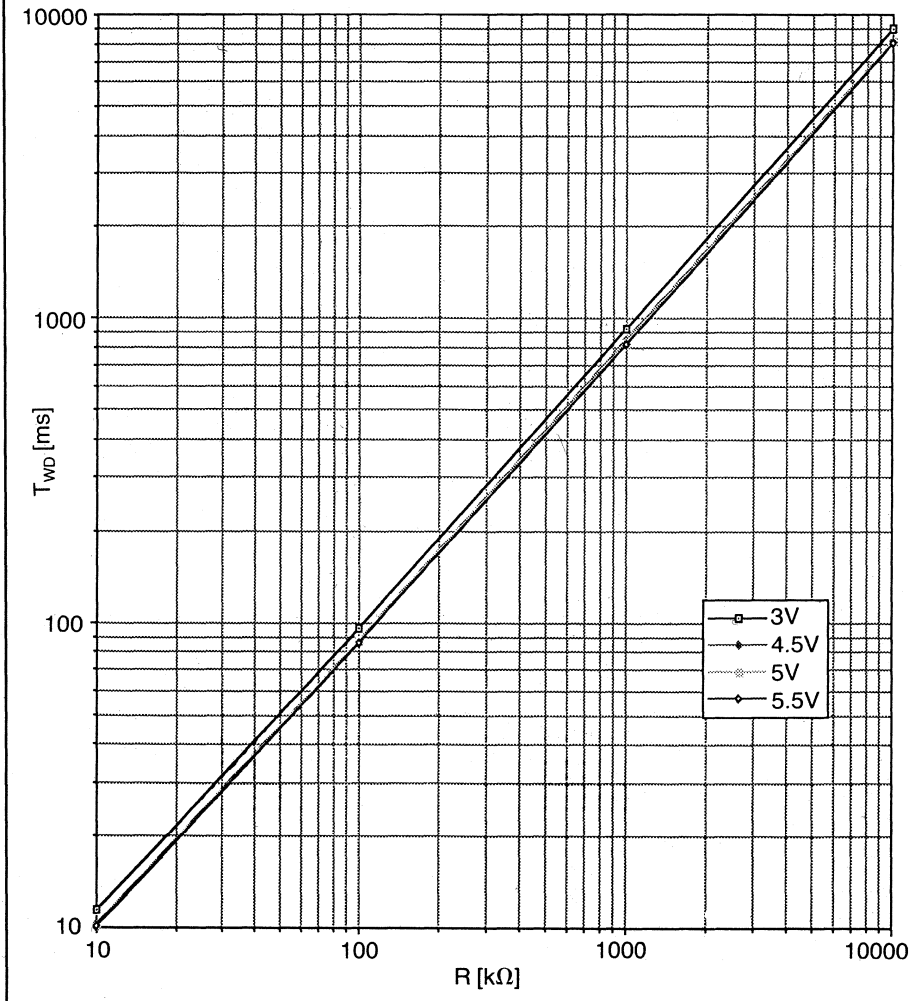


Fig. 15

T_{WD} versus V_{OUTPUT} at $T_J = +70°C$

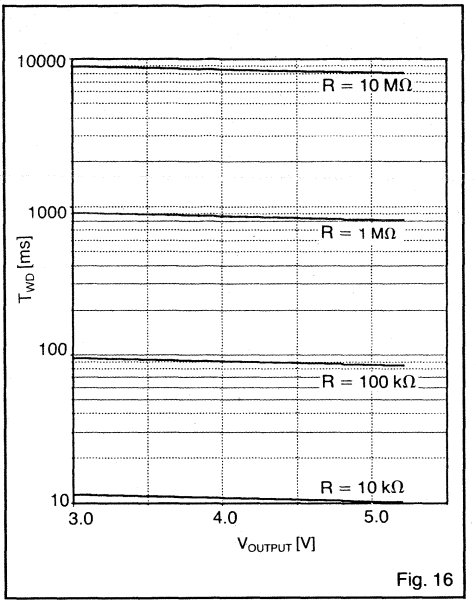


Fig. 16

T_{WD} versus R at $T_J = +70°C$

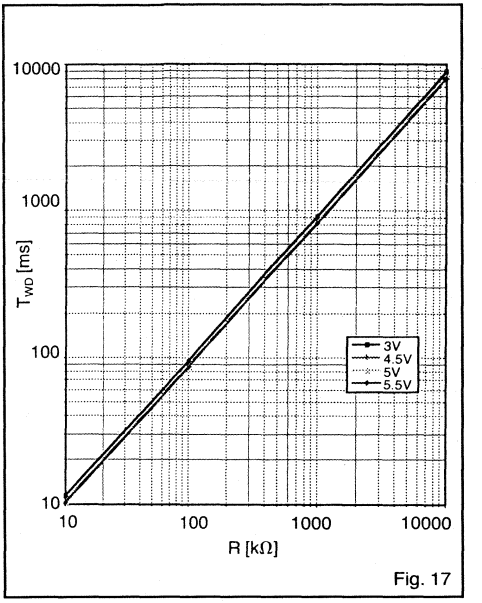


Fig. 17

T_{WD} versus V_{OUTPUT} at $T_J = -40°C$

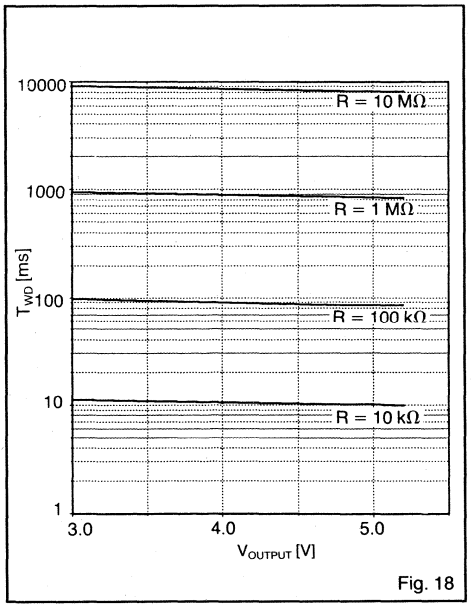


Fig. 18

T_{WD} versus R at $T_J = -40°C$

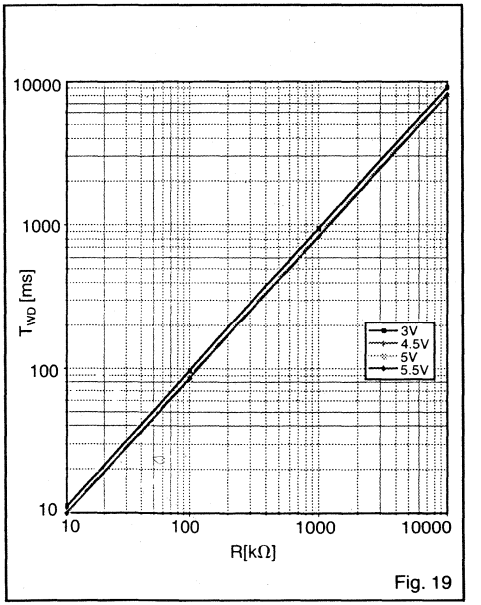
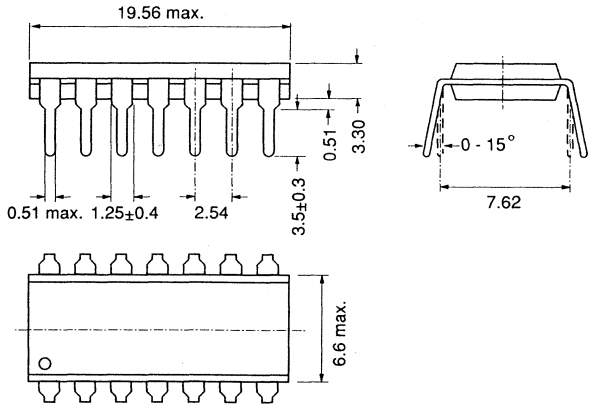


Fig. 19

8

Package and Ordering Information

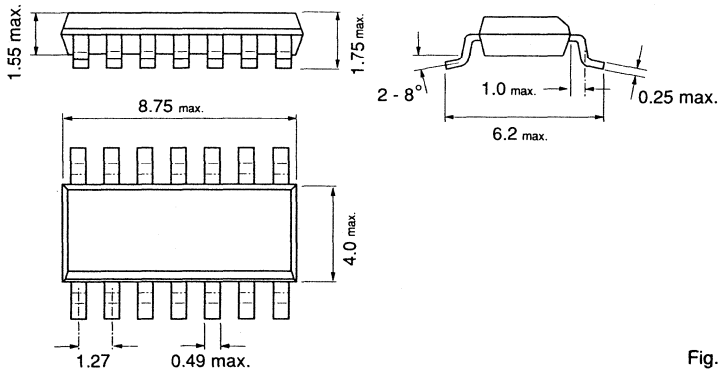
Dimensions of DIP14 Package



Dimensions in mm

Fig. 20

Dimensions of SO14 Package



Dimensions in mm

Fig. 21

Ordering Information

The A 6133 is available in the following packages:

Type	Package
A 6133 14P	DIP14
A 6133 14S	SO14

When ordering please specify complete part number.

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Low Power Regulator & Watchdog

Features

- Supply current 10 μA max. for the load current range 0 - 50 mA, 5 V regulated output
- Digitally programmable voltage regulator, 5 V, 3 V or 2 V
- Low dropout voltage, typically 4 mV at 100 μA load
- Fully operational for unregulated DC input voltage up to 10 V and regulated output voltage down to 1.5 V
- Short circuit and thermal protection
- Battery fail warning, regulator input tested (5 mA for 300 μs) every 15 minutes
- Power-on reset and power-down reset
- Watchdog with 2 s timeout
- Watchdog offers the possibility to detect a microcontroller in sleep mode
- Pulse output every 15 minutes for time management
- Clock output with three modes of operation:
  1. A 92 s retriggerable monostable
  2. A 2 kHz square wave for piezo electric buzzer
  3. A 32.768 kHz system clock
- −40°C to +85°C temperature range
- DIP16 and SO16 packages

Applications

- Security systems
- Remote smart sensors
- Pagers
- Battery operated and portable products

Typical Operating Configuration

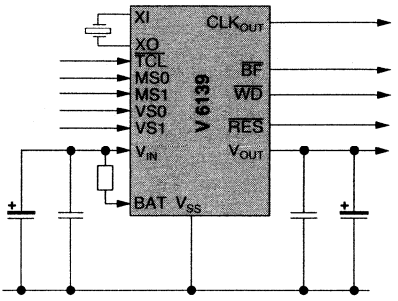


Fig. 1

Description

The V 6139, with a total current consumption of 10 μA max., is very suited to battery driven portable microcontroller systems. Combined on one IC are a digitally programmable voltage regulator, power surveillance and battery fail circuitry, a watchdog, pulse and clock outputs and a crystal oscillator. The state of the battery supply is sampled every 15 minutes by drawing a current of 5 mA for 30 ms. If the voltage dropped across a resistor brings the voltage below the reference voltage then the BF pin goes active.

The P15 output supplies a pulse of 30 ms every 15 minutes which allows regular long term time management by the user's software. The CLK output can supply a retriggerable monostable with a timeout of 92 seconds or square waves of 2 kHz or 32.768 kHz.

The watchdog function monitors software execution by checking the $\overline{TCL}$ signal for a change of state within a timeout period of 2 seconds. If the watchdog times out, $\overline{RES}$ is activated; the $\overline{WD}$ output is also activated to indicate to software that a watchdog time out caused the reset. If the microcontroller $\overline{TCL}$ output is put in a high impedance condition, the V 6139 will detect this condition as a microcontroller in the sleep mode and prevent its watchdog from timing out.

Pin Assignment

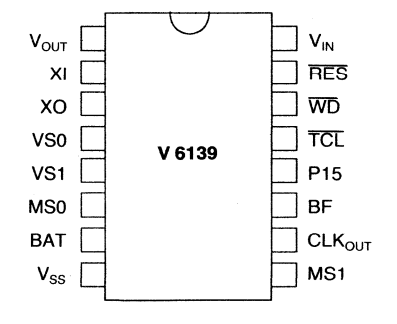


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{IN} to V_{SS}	V_{IN}	−0.5 to +11 V
Max. voltage at any signal pin	V_{MAX}	V_{OUT} +0.3 V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3 V
Operating junction temp. range	T_J	−40 to +125°C
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+85	°C
Supply voltage [1]	V_{IN}	2		10	V
Operating V_{OUT} voltage[1]	V_{OUT}	1.5		6.0	V
I_{OUT}[2] at V_{OUT} = 5 V	I_{OUT}			50	mA
at V_{OUT} = 3 V	I_{OUT}			20	mA
at V_{OUT} = 2 V	I_{OUT}			10	mA
Thermal resistance[3] (junction to ambient)					
– DIP16	$R_{th(j-a)}$			160	°C/W
– SO16	$R_{th(j-a)}$			240	°C/W
Decoupling capacitors on V_{IN} and V_{OUT}	C_T	100			nF
Load capacitors on V_{IN} and V_{OUT}[4]	C_L	2.2			µF
Crystal characteristics					
Frequency	f		32.768		kHz
Load capacitance	C_L	7	8.2	30	pF
Series resistance	R_S		35	50	kΩ

Table 2

[1] Full operation guaranteed. If the regulator is bypassed (ie. V_{IN} tied to V_{OUT}) the V_{OUT} voltage must not exceed 6.0 V.

[2] I_{OUT} will not apply for all possible combinations of input voltage and output current. Combinations that would require the V 6139 to work above the maximum junction temperature (85°C) must be avoided.

[3] The thermal resistance from junction to ambient specified assumes that the package is soldered onto a PCB.

[4] The 2.2 µF capacitor must have an effective resistance of 5 Ω or less and a resonant frequency of above 500 kHz.

Electrical Characteristics

V_{IN} = 7 V, V_{OUT} programmed for 5 V, I_L = 0, BAT pulled up to V_{IN} with 700 Ω, V_{SS} = 0 V, −40 ≤ T_J ≤ +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static supply current	I_{DD}	V_{IN} = 10 V, 0 ≤ I_L ≤ 50 mA, I/Ps at V_{SS}		7	12	μA
Dynamic supply current	I_{DD}	CLK_{OUT} programmed for 2 kHz, output load capacitance ≤ 50 pF		8.5	14	μA
Output voltage	V_{OUT}	0 ≤ I_L ≤ 50 mA	4.75	5	5.25	V
Output voltage	V_{OUT}	V_{IN} = 4.5 V, V_{OUT} programmed for 3 V, 0 ≤ I_L ≤ 20 mA	2.85	3	3.15	V
Output voltage	V_{OUT}	V_{IN} = 3 V, V_{OUT} programmed for 2 V, 0 ≤ I_L ≤ 10 mA	1.9	2	2.2	V
Line regulation	V_{LINE}	6 V ≤ V_{IN} ≤ 10 V, I_L = 10 mA		0.03	0.35	%
Load regulation	V_L	0 ≤ I_L ≤ 30 mA		0.4	1	%
Dropout voltage[1]	$V_{DROPOUT}$	I_L = 100 μA		4	50	mV
Dropout voltage[1]	$V_{DROPOUT}$	I_L = 30 mA, T_J = 25°C			850	mV
Current limit	I_{Lmax}	V_{OUT} tied to V_{SS}			180	mA
Inputs						
Input logic high	V_{IH}		V_{OUT}−1			V
Input logic low	V_{IL}				V_{OUT}+1	V
W_{IN} high impedance detect current	I_Z		50	100	150	μA
BAT test voltage	V_T		1.2	1.3	1.4	V
BAT sink current	I_T		4.5		7	mA
Outputs						
CLK_{OUT} output logic high	V_{OH}	I_{OH} = 3 mA	V_{OUT}−0.4			V
CLK_{OUT} output logic low	V_{OL}	I_{OL} = 5 mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 5 mA	V_{OUT}−0.4			V
Output logic low	V_{OL}	I_{OL} = 8 mA			0.4	V

Table 3

[1] The dropout voltage is defined as the V_{IN} to V_{OUT} differential at which V_{OUT} drops 100 mV below its nominal value measured at a 1 V differential. The supply current does not increase significantly in dropout.

Timing Characteristics

V_{IN} = 7 V, V_{OUT} programmed for 5 V, I_L = 0, BAT pulled up to V_{IN} with 700 Ω, V_{SS} = 0 V, $-40 \leq T_J \leq +85°C$, unless otherwise specified

Parameter[1)]	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power-on reset delay	T_{POR}			30		ms
Reset pulse width	T_{RES}			30		ms
Watchdog timeout	T_{WD}		1.93		2.0	s
TCL pulse width	T_{TCL}		31			µs
TCL high impedance detection period	P_{TCLZ}			60		ms
TCL high impedance detection width	T_{TCLZ}			30.5		µs
P15 output period	P_{P15}			15		min
P15 output pulse width	T_{P15}			30		ms
CLK_{OUT} programmed for monostable timeout	T_{CLKOUT}		92		96	s
CLK_{OUT} programmed for 2 kHz clock	f_{CLKOUT}			2.048		kHz
CLK_{OUT} programmed for 32 kHz clock	f_{CLKOUT}			32.768		kHz
Logic transition times for all O/Ps	T_{TR}	Load = 50 pF		300	600	ns

Table 4

[1)] The accuracy of the timing parameters is given by the accuracy of the external crystal plus or minus 100 ppm unless otherwise specified.

Timing Waveforms

Watchdog Timer

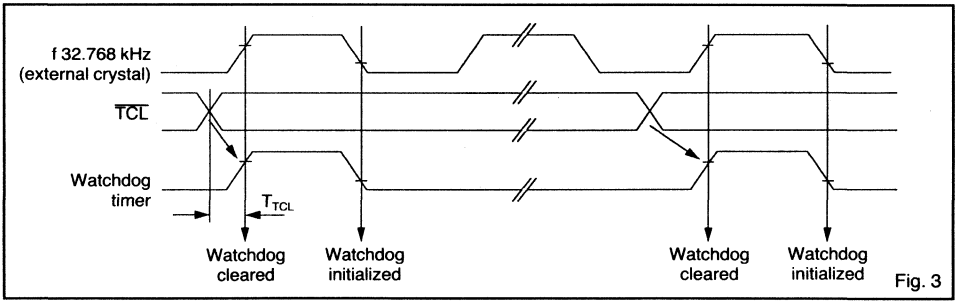


Fig. 3

Watchdog and Reset Timing

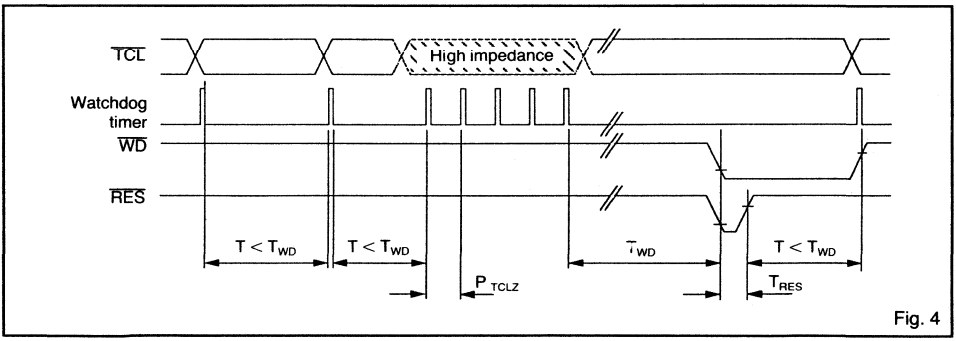


Fig. 4

Monostable Timing

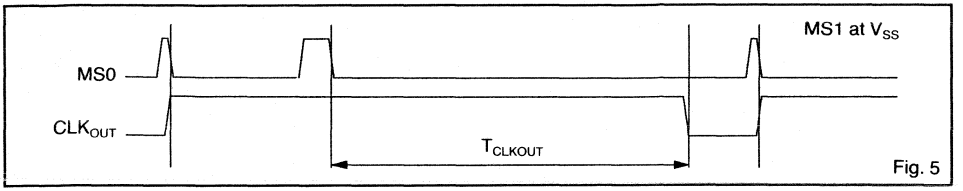


Fig. 5

15 Minute Pulse on P15 and Battery Test

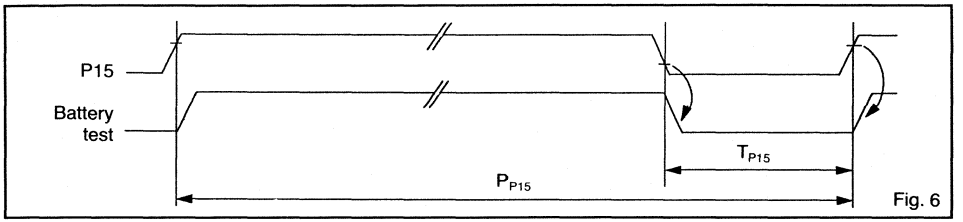


Fig. 6

$\overline{TCL}$ High Impedance Detection

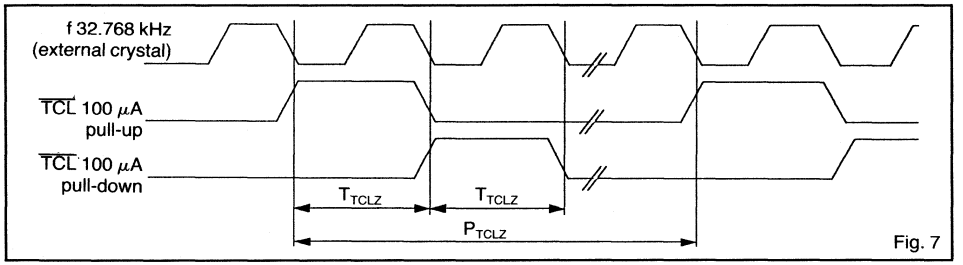


Fig. 7

Block Diagram

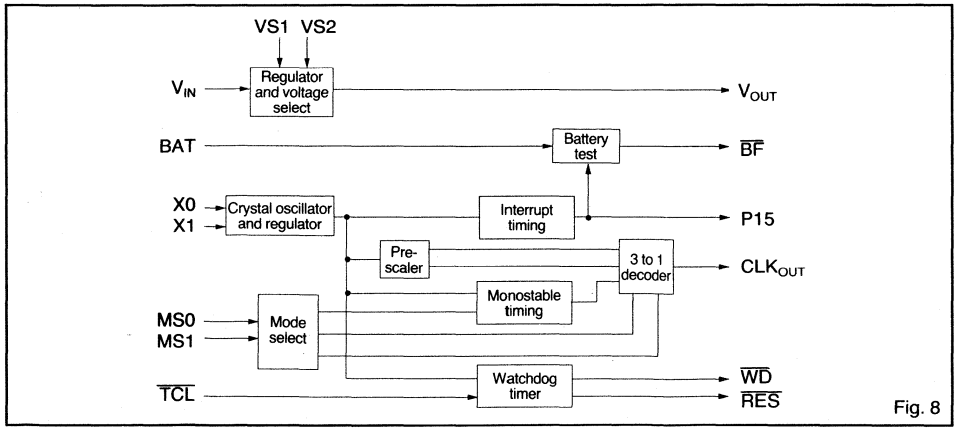


Fig. 8

Pin Description

Pin	Name	Function
1	V_{OUT}	Voltage regulator output
2	XI	32.768 kHz crystal input
3	XO	32.768 kHz crystal output
4	VS0	Voltage regulator programming input 0
5	VS1	Voltage regulator programming input 1
6	M_{S0}	Mode select input 0
7	BAT	Battery voltage monitoring input
8	V_{SS}	GND terminal
9	M_{S1}	Mode select input 1
10	CLK_{OUT}	Clock output
11	BF	Active high battery fail output
12	$\overline{P15}$	15 minutes pulse output
13	$\overline{TCL}$	Watchdog timer clear input
14	$\overline{WD}$	Active low watchdog timeout output
15	$\overline{RES}$	Active low reset output
16	V_{IN}	Voltage regulator input

Table 5

Functional Description

Voltage Regulator

The V 6139 has a digitally programmable voltage regulator. The logic levels on the inputs VS0 and VS1 program the regulator for 5 V, 3 V or 2 V output in accordance with Table 6. The regulator output voltage can be changed at any time, for example normal program execution could be at 5 V and for standby mode the microcontroller could switch to 3 V. The regulator has current limit and thermal protection. **If the regulator is not needed it can be bypassed by short circuiting V_{IN} to V_{OUT}; in this case the voltage at V_{IN} must not exceed 6 V; all other features function as normal.**

V_{S1}	V_{S0}	V_{OUT}
0	0	5 V
0	1	3 V
1	0	2 V
1	1	Factory test mode

Table 6

The low supply current (7 μA typically over the temperature range) and low dropout voltage makes the V 6139 very suitable for low power battery operated systems. The V_{IN} ranges from 2 to 10 V which covers most battery values on the market. Two decoupling capacitors should be added, one for V_{IN} and one for V_{OUT} and their value should be 100 nF. A load capacitor of $\geq$ 2.2 μF is needed on V_{OUT} for stability. To achieve good line regulation a capacitor of $\geq$ 2.2 μF is needed on V_{IN}.

Care should be taken not to exceed the maximum operating junction temperature (85°C). The power dissipation within the V 6139 can be approximated by the formula:

$$P = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

The maximum continuous power dissipation at a given ambient temperature can be calculated using the formula:

$$P_{MAX} = (85°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. The $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB.

The formula for maximum continuous power dissipation assumes a constant load (ie. $\geq$ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the V 6139 in DIP16 package will have an effective thermal resistance from the junction to the ambient of about 15°C/W for a single 100 ms pulse.

Power-up and Power-down

When the power is applied the $\overline{RES}$ output stays low until 30 ms after the device has reached its regulated voltage level this is the POR time. If the voltage at V_{IN} falls below the regulated voltage level a reset is generated.

Battery Test

The battery is tested every 15 minutes by drawing 5 mA of current through a resistor connected to V_{IN} (see Fig. 6 and 11). The test time is 30 ms. During this time the voltage at the BAT pin is compared to the internal voltage reference (V_T). If the voltage at the BAT pin is lower than V_T, the BF output is taken active high. The average current due to the battery test is 0.17 μA and so is not significant. The resistor should be chosen to suit the particular battery voltage being used.

Reset and Watchdog

The watchdog circuit monitors the activity of the microcontroller. If the user's software does not send a pulse to the $\overline{TCL}$ input within the watchdog timeout period, a $\overline{RES}$ pulse is generated. The $\overline{TCL}$ input is sampled at the rate of 32.768 kHz or every 31 μs. If no change of state is detected inside the timeout period of 2 seconds, the watchdog timer times out and $\overline{RES}$ is taken active (see Fig. 4). If $\overline{RES}$ goes active because of a watchdog timeout, then the $\overline{WD}$ pin goes active low to indicate to the microcontroller that the cause of the reset is a watchdog timeout and not a drop-in voltage. If a level change on $\overline{TCL}$ appears before the 2 seconds, the watchdog timer is cleared and intialized (see Fig. 3).

The $\overline{WD}$ output is deactivated by a change of state of the $\overline{TCL}$ input or the detection of a high Z condition on the $\overline{TCL}$ pad as explained below (see Fig. 4). The $\overline{WD}$ output goes inactive only after the $\overline{RES}$ has gone inactive.

Many low-power microcontroller systems do not run 100% of the time, instead they are put in a sleep mode where an interrupt or reset can awaken them, for example a key-push on a user interface could be used to cause an interrupt to the microcontroller. The V 6139 offers the possibility to detect a microcontroller in the sleep mode and will prevent its watchdog from timing out in such a case. If the microcontroller $\overline{TCL}$ output is put into a tri-state condition (high Z), the V 6139 will detect this condition and prevent its watchdog from timing out. The V 6139 uses the high impedance state on $\overline{TCL}$ to

detect a microcontroller in the sleep mode as opposed to software mal-functioning. The $\overline{TCL}$ pad is subjected to an internally produced 100 μA pull-up and then a 100 μA pull-down every 60 ms (see Fig. 4 and 7). If the TCL pad follows both pulses then the microcontroller is in high Z and the watchdog timer is prevented from timing out. If the microcontroller is not in high Z, then the pull-up and pull-down pulses will not be able to fight against the level on the pad.

CLK_{OUT}

The CLK_{OUT} output can be programmed for one of three possible modes of operation:

1. It can provide a monostable timeout every 92 s which is retriggerable by a falling edge on MS0.
2. It can provide a 2 kHz square wave which could be useful for activating a piezo electric buzzer.
3. It can provide a system clock of 32.768 kHz.

The logic levels on the mode select inputs MS0 and MS1 program the CLK_{OUT} mode (see Table 7).

MS1	MS0	CLK_{OUT}
0	Falling edge	Initializes the monostable
0	0	Monostable pulse 92 s after initialisation
1	0	2 kHz frequency
1	1	32.768 kHz frequency

Table 7

Oscillator

Use a crystal of nominal C_L = 8.2 pF as specified in the section "Operating Conditions". The MX series from Microcrystal is recommended. The accuracy of the time keeping is dependent upon the frequency tolerance and the load capacitance of the crystal. To measure the accuracy use the CLK_{OUT} with MS0 and MS1 tied to V_{OUT}. 11.57 ppm correspond to one second a day.

Crystal Layout

In order to ensure correct oscillator operation we recommend the following standard practices:

- Keep traces as short as possible.
- Use a guard ring connected to V_{SS} around the crystal.

Fig. 9 shows the recommended layout.

Layout

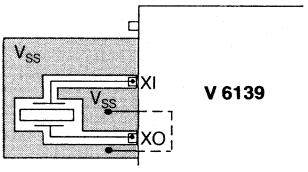


Fig. 9

Typical Applications

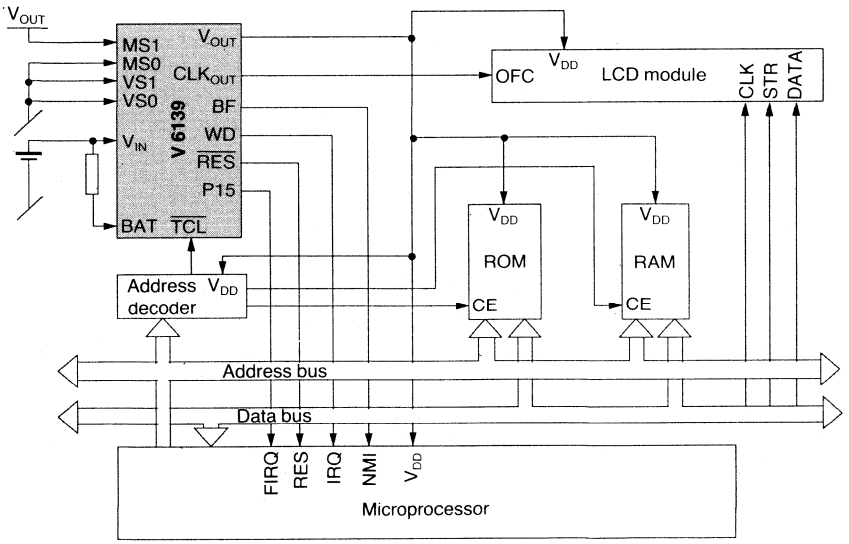
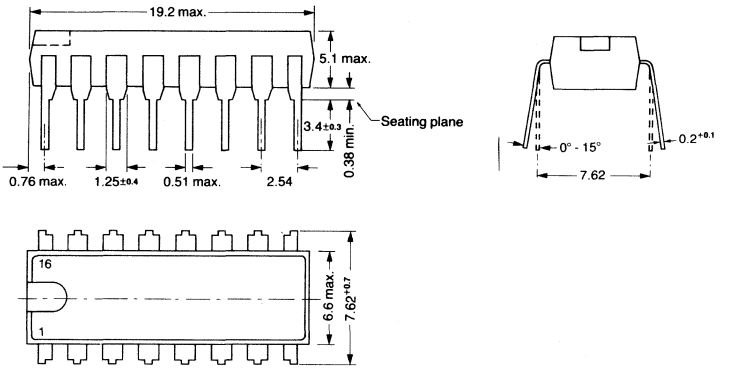


Fig. 11

8

Package and Ordering Information

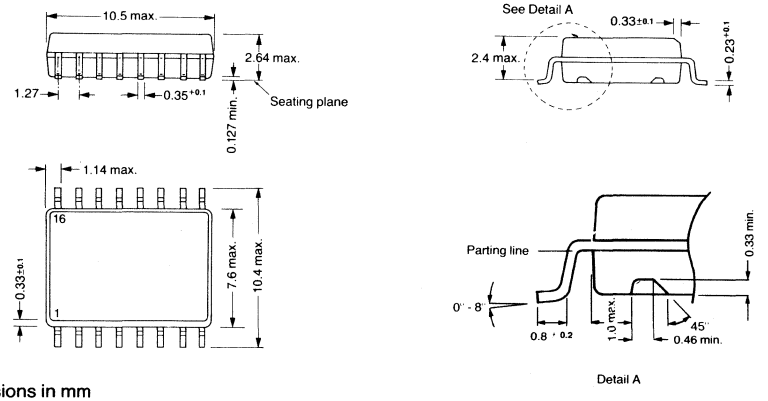
Dimensions of DIP16 Package



Dimensions in mm

Fig. 12

Dimensions of SO16 Package



Dimensions in mm

Fig. 13

Ordering Information

The V 6139 is available in the following packages:

DIP16 pin plastic package	V 6139 16P
SO16 pin plastic package	V 6139 16S

When ordering, please specify the complete part number and package.

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A 6150

Regulator & Watchdog

Features

- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 250 mV at 100 mA
- Low quiescent current, typically 175 μA
- Standby mode, maximum current 240 μA (without load on OUTPUT)
- Unregulated DC input can withstand −20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 3.0 V
- Reset output guaranteed for regulated output voltage down to 1.2 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Comparator for voltage monitoring, reset threshold 1.5V
- Programmable reset voltage monitoring
- Programmable power on reset (POR) delay
- Watchdog with programmable time windows guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ±10%
- System enable output offers added security
- TTL/CMOS compatible
- −40°C to +85°C temperature range
- On request extended temperature range −40 to +125°C
- DIP8 and SO8 packages

Description

The A 6150 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring in an 8 lead package. The voltage regulator has a low dropout voltage (typ. 250 mV at 100 mA) and a low quiescent current (175 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage transient of −20 V (reverse battery). The input may be connected to ground or a reverse voltage without reverse current flow from the output to the input. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.5 V reference. The power-on reset function is initialized after V_{IN} reaches 1.5 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.5 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Automotive systems
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies

Typical Operating Configuration

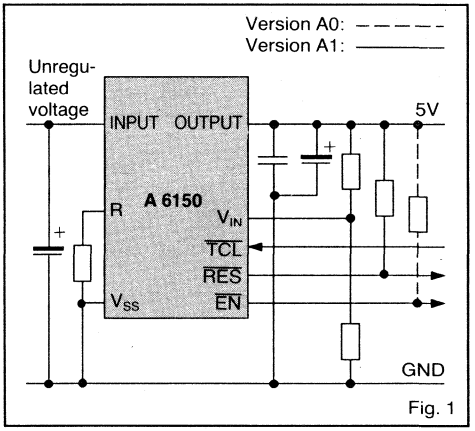

Fig. 1

Pin Assignment

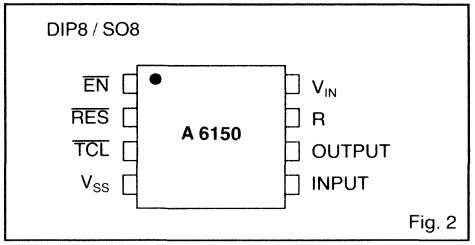

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	−0.3 to +30 V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	−20 to +60 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+125	°C
INPUT voltage [1]	V_{INPUT}	3.36		26	V
OUTPUT voltage [1][2]	V_{OUTPUT}	3.0			V
$\overline{RES}$ & $\overline{EN}$ guaranteed [3]	V_{OUTPUT}	1.2			V
OUTPUT current [4]	I_{OUTPUT}			100	mA
Comparator input voltage	V_{IN}	0		V_{OUTPUT}	V
RC-oscillator programming	R	10		1000	kΩ
Thermal resistance from junction to ambient [5]					
– DIP8	$R_{th(j-a)}$			105	°C/W
– SO8	$R_{th(j-a)}$			160	°C/W

Table 2

1) Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 µF capacitor or greater is required on the INPUT, see Fig. 18. The 22 µF must have an effective resistance ≤ 5 Ω and a resonant frequency above 500 kHz.

2) A 10 µF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 µF must have an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

3) $\overline{RES}$ and $\overline{EN}$ ($\overline{EN}$ only for version A0) must be pulled up externally to V_{OUTPUT} even if they are unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

4) The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A 6150 to work above the maximum junction temperature (125°C) must be avoided.

5) The thermal resistance specified assumes the package is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 100 µA			240	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 µA		175	300	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1MΩ to V_{OUTPUT}, I_L = 100 mA		1.7	4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88		5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA, −40°C ≤ T_J ≤ 125°C	4.85		5.15	V
Output voltage temperature coefficient [2]	$V_{th(coeff)}$			50	180	ppm/°C
Line regulation [3]	V_{LINE}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = 125°C		0.2	0.5	%
Load regulation [3]	V_L	100 µA ≤ I_L ≤ 100 mA		0.2	0.6	%
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 µA		40	170	mV
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 mA			420	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, I_L = 100 µA, R_{EXT} = 100 kΩ, O/Ps 1 MΩ to V_{OUTPUT}, I/Ps at V_{OUTPUT}		300	560	µA
Thermal regulation [5]	V_{thr}	T_J = 25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms		0.05	0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}			450	mA
OUTPUT noise, 10Hz to 100kHz	V_{NOISE}			200		µV rms
$\overline{RES}$ (vers. A0, A1) **& $\overline{EN}$** (vers. A0)						
Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$ (vers. A1)						
Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{OUTPUT} = 2.0 V, I_{OH} = −100 µA	1.8	1.9		V
	V_{OH}	V_{OUTPUT} = 1.2 V, I_{OH} = −30 µA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}		2.0		V_{OUTPUT}	V
Leakage current	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference [6] [7]	V_{REF}	T_J = 25°C	1.474	1.52	1.566	V
	V_{REF}		1.436		1.620	V
	V_{REF}	−40°C ≤ T_J ≤ 125°C	1.420		1.620	V
Comparator hysteresis [7]	V_{HY}			2		mV

Table 3

[1] If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A 6150.

[2] The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

[3] Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.

[4] The dropout voltage is defined as the INPUT to OUTPUT voltage differential at which the OUTPUT voltage drops 100 mV below its nominal measured at a 1 V differential.

[5] Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.

[6] The comparator and the voltage regulator have separate voltage references (see "Block Diagram" Fig. 7).

[7] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 4).

Timing Characteristics

V_{INPUT} = 6.0 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +125°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays: $\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 123 kΩ ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 123 kΩ ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 123 kΩ ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 123 kΩ ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 123 kΩ ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

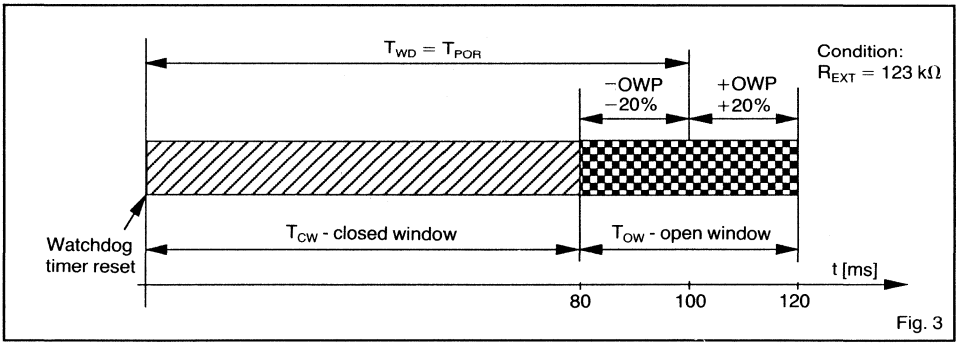

Fig. 3

Voltage Monitoring

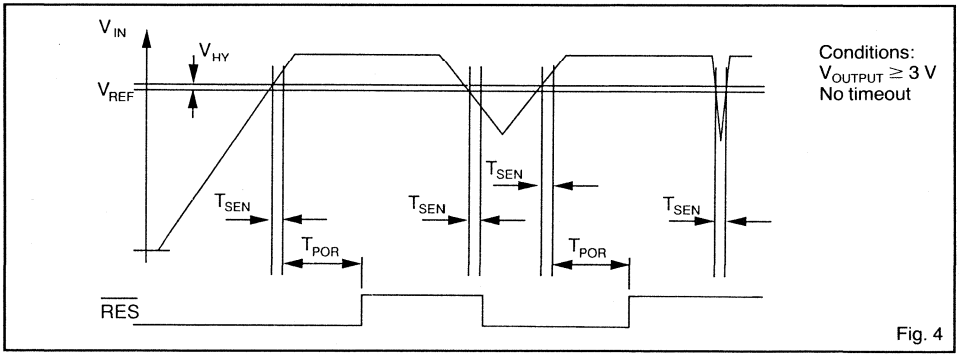

Fig. 4

Timer Reaction

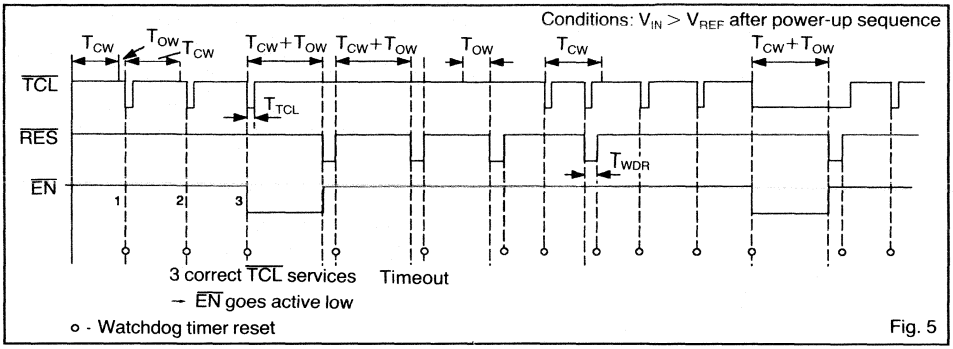

Fig. 5

Combined Voltage and Timer Reaction

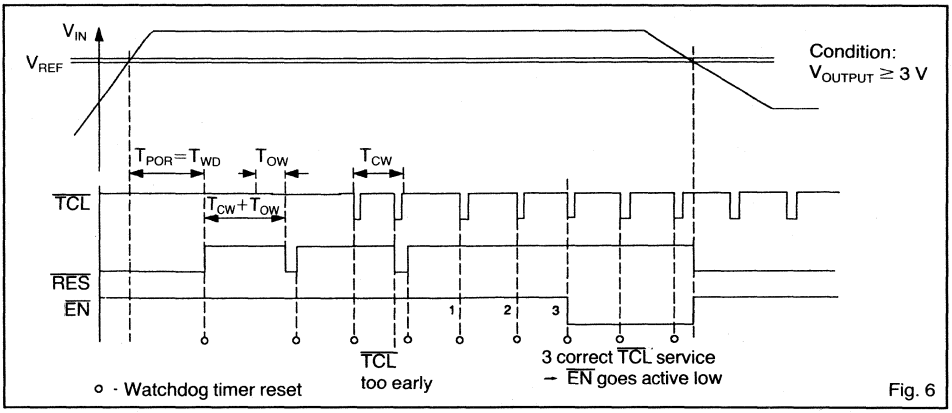

Fig. 6

Block Diagram

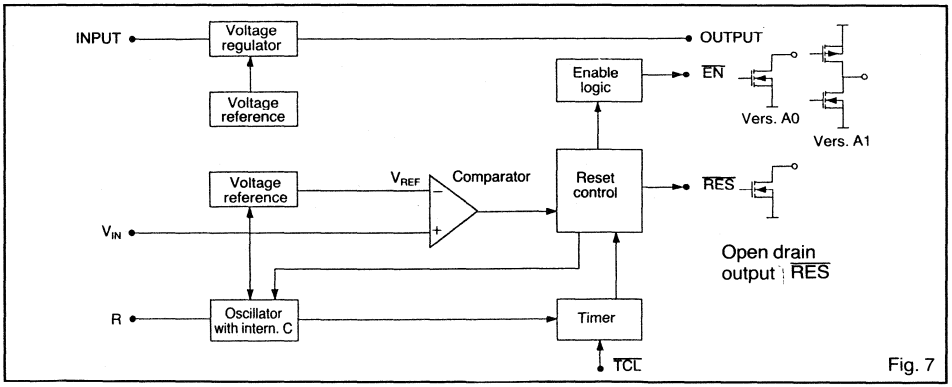

Fig. 7

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Pin Description

Pin	Name	Function
1	$\overline{EN}$	Vers. A0: Open drain active lowenable output. $\overline{EN}$ must be pulled up to V_{OUTPUT} even if unused Vers. A1: Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	INPUT	Voltage regulator input
6	OUTPUT	Voltage regulator output
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

Voltage Regulator

The A 6150 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 175 μA) makes the A 6150 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 3.36 V to 26 V for operation and the input protection includes both reverse battery (negative transients up to 20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 18). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about −30°C, so tantalums are recommended for operation below −25°C. The important parameters of the 22 μF capacitor are an effective series resistance of $\leq 5\ \Omega$ and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A 6150 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Care must be taken not to exceed the maximum junction temperature (+125°C). The power dissipation within the A 6150 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (125°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (ie. ≥ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A 6150 in DIP8 package will have an effective thermal resistance from the junction to the ambient of about 10°C/W for a single 100 ms pulse.

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 18. The user uses the external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.52 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 4). After INPUT reaches 3.36 V (and so OUTPUT reaches at least 3 V) and V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 123 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 18) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 123 kΩ typical values are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 3) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula as the limits for servicing signal $\overline{TCL}$ during the open window:

$R_{EXT} \times 0.75$ to $R_{EXT} \times 0.85$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ).

For example, if R_{EXT} = 123 kΩ then T_{WD} = 100 ms ±10% and the useful open window limits for software are 90 to 110 ms.

T_{WD} versus V_{OUTPUT} at T_J = +25°C

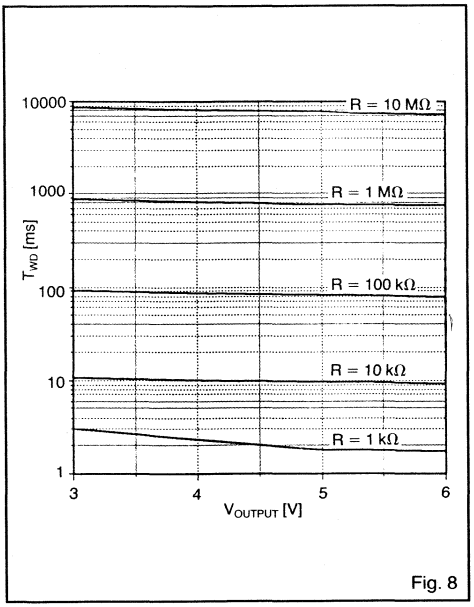

Fig. 8

T_{WD} versus R at T_J = +25°C

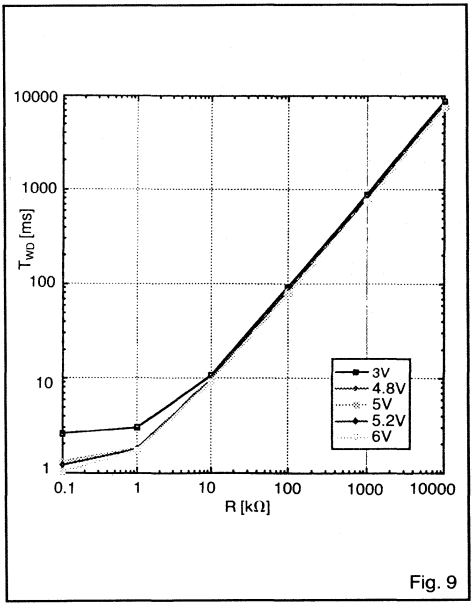

Fig. 9

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T_{WD} versus R at T_J = +25°C

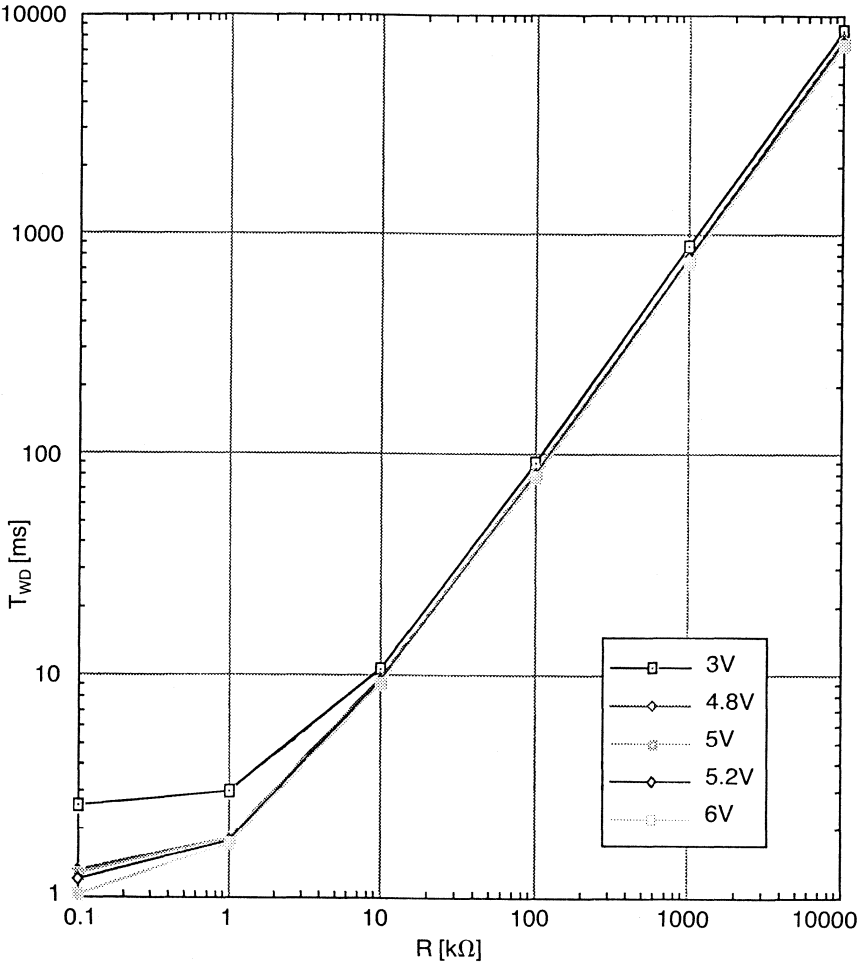


Fig. 10

T_{WD} versus V_{OUTPUT} at $T_J = +85°C$

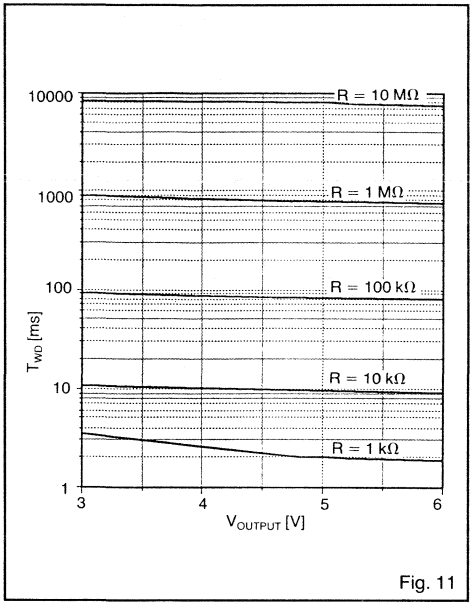


Fig. 11

T_{WD} versus R at $T_J = +85°C$

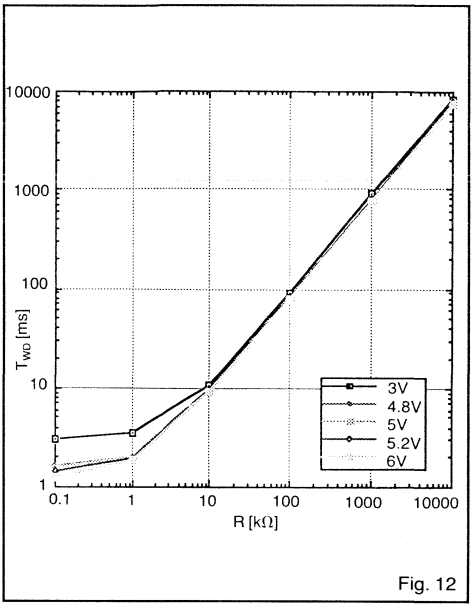


Fig. 12

T_{WD} versus V_{OUTPUT} at $T_J = -40°C$

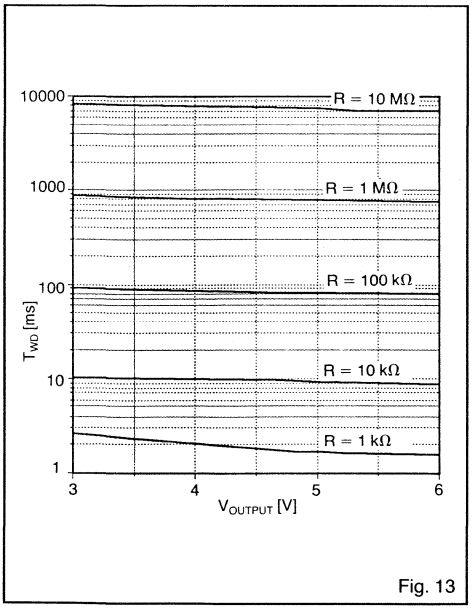


Fig. 13

T_{WD} versus R at $T_J = -40°C$

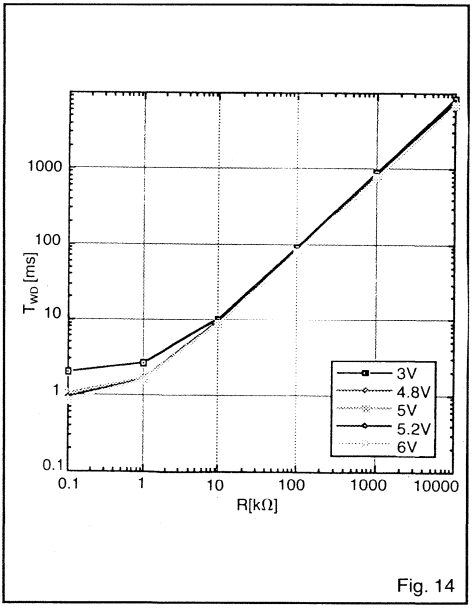


Fig. 14

8

T_{WD} versus temperature at 5 V

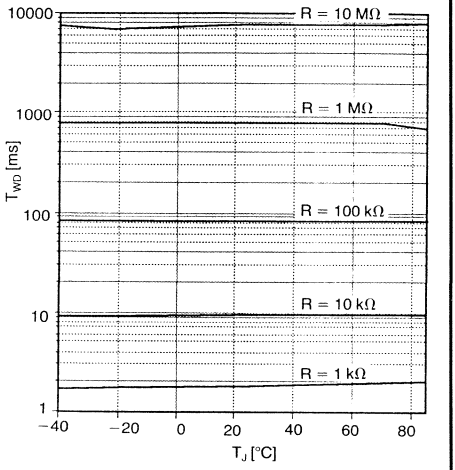


Fig. 15

T_{WD} versus R at 5 V

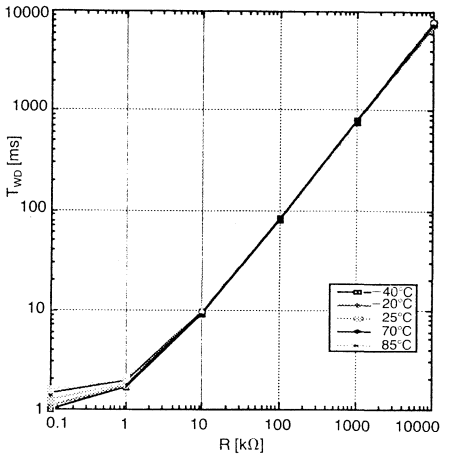


Fig. 16

OUTPUT Current versus INPUT Voltage

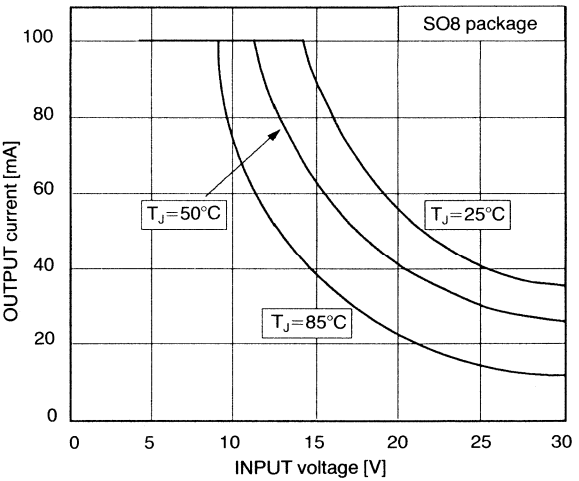


Fig. 17

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40 = 2.5$ ms typically (see Fig. 5).
With the open window constraint new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though software is malfunctioning; the A 6150 would make a system reset because the watchdog would be cleared too quickly.
If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").
The $\overline{RES}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 18).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable – $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.
A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The A 6150 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).
For the version A0 the $\overline{EN}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 18).

8

Typical Application

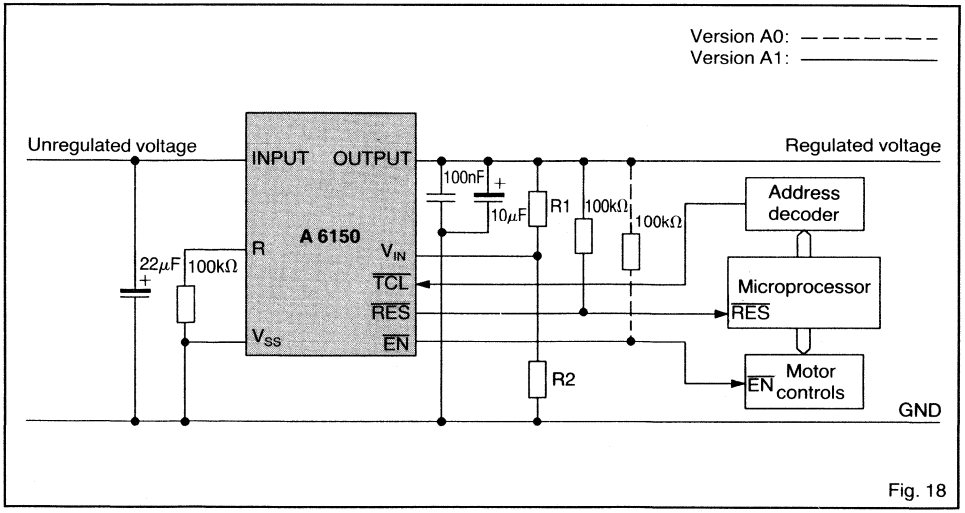
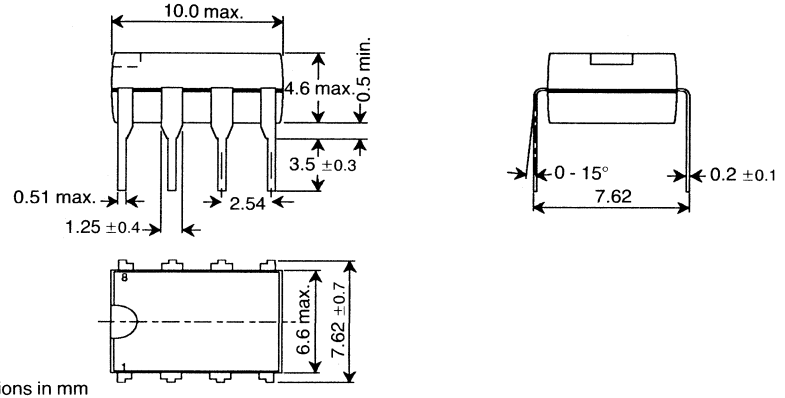


Fig. 18

Package and Ordering Information

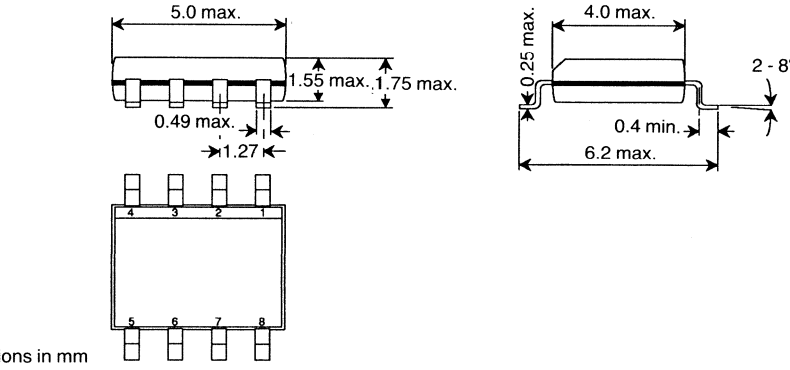
Dimensions of DIP8 Package



Dimensions in mm

Fig. 19

Dimensions of SO8 Package



Dimensions in mm

Fig. 20

Ordering Information

Industrial temperature range (−40°C to +85°C):

Type[1]	Package
A 6150 nn 8P	DIP8
A 6150 nn 8S	SO8

When ordering please specify complete part number.

Marking on package:

Package	Marking[1]
DIP8	A 6150 nn
SO8	6150 nn

[1] nn stands for the versions A0*, A1.

Extended temperature range (−40°C to +125°C):

Type[1]	Package
A 6150 nn X 8P	DIP8*
A 6150 nn X 8S	SO8*

* on request

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Regulator & Watchdog

Features

- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 250 mV at 100 mA
- Low quiescent current, typically 155 μA
- Standby mode, maximum current 240 μA (without load on OUTPUT)
- Unregulated DC input can withstand −20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 3.0 V
- Reset output guaranteed for regulated output voltage down to 1.2 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Comparator for voltage monitoring, reset threshold 1.17V
- ± 1.5% voltage threshold tolerance at 25°C
- ± 3% voltage threshold tolerance from −40 to +70°C
- Programmable reset voltage monitoring
- Voltage window, high threshold 5.9 V
- Programmable power on reset (POR) delay
- Watchdog with programmable time windows guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ±10%
- System enable output offers added security
- TTL/CMOS compatible
- −40°C to +70°C temperature range
- DIP8 and SO8 packages

Description

The A 6170 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring in an 8 lead package. The voltage regulator has a low dropout voltage (typ. 250 mV at 100 mA) and a low quiescent current (155 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage transient of −20 V (reverse battery). The input may be connected to ground or a reverse voltage without reverse current flow from the output to the input. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies

Typical Operating Configuration

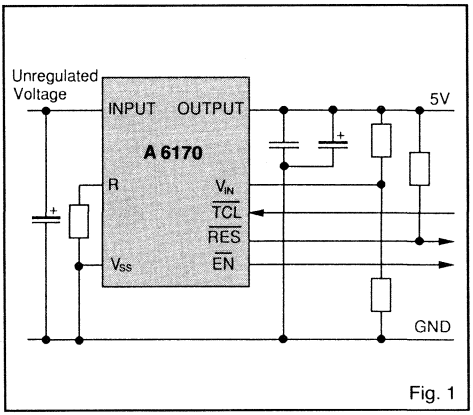


Fig. 1

Pin Assignment

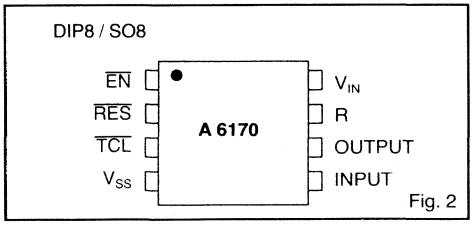


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	−0.3 to +30 V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	−20 to +60 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+70	°C
INPUT voltage [1]	V_{INPUT}	3.36		26	V
OUTPUT voltage [1)2)]	V_{OUTPUT}	3.0			V
$\overline{RES}$ & $\overline{EN}$ guaranteed [3]	V_{OUTPUT}	1.2			V
OUTPUT current [4]	I_{OUTPUT}			100	mA
Comparator input voltage	V_{IN}	0		V_{OUTPUT}	V
RC-oscillator programming	R	10		1000	kΩ
Thermal resistance from junction to ambient [5]					
– DIP8	$R_{th(j-a)}$			105	°C/W
– SO8	$R_{th(j-a)}$			160	°C/W

Table 2

1) Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 µF capacitor or greater is required on the INPUT, see Fig. 8. The 22 µF must have an effective resistance ≤ 5 Ω and a resonant frequency above 500 kHz.

2) A 10 µF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 µF must have an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

3) $\overline{RES}$ must be pulled up externally to V_{OUTPUT} even if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

4) The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A 6170 to work above the maximum junction temperature (70°C) must be avoided.

5) The thermal resistance specified assumes the package is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 100 µA			240	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 µA		155	300	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 mA		1.7	4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88		5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA, −40°C ≤ T_J ≤ 70°C	4.85		5.15	V
Output voltage temperature coefficient [2]	$V_{th(coeff)}$			50	180	ppm/°C
Line regulation [3]	V_{LINE}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = 70°C		0.2	0.5	%
Load regulation [3]	V_L	100 µA ≤ I_L ≤ 100 mA		0.2	0.6	%
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 µA		40	170	mV
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 mA			420	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, I_L = 100 µA, R_{EXT} = 100 kΩ, O/Ps 1 MΩ to V_{OUTPUT}, I/Ps at V_{OUTPUT}		300	560	µA
Thermal regulation [5]	V_{thr}	T_J = 25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms		0.05	0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}			450	mA
OUTPUT noise, 10Hz to 100kHz	V_{NOISE}			200		µV rms

3.0 ≤ V_{OUTPUT} ≤ 5.5 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

$\overline{RES}$ and $\overline{EN}$						
Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$						
Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{OUTPUT} = 2.0 V, I_{OH} = −100 µA	1.8	1.9		V
	V_{OH}	V_{OUTPUT} = 1.2 V, I_{OH} = −30 µA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}		2.0		V_{OUTPUT}	V
Leakage current $\overline{TCL}$ input	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference [6] [7]	V_{REF}	T_J = 25°C	1.148	1.170	1.200	V
	V_{REF}	T_J = −20°C to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis [7]	V_{HY1}			2		mV
Level detector of V_{OUTPUT} [8]	V_{HIGH}	T_J = 25°C	5.78	5.95	6.12	V
	V_{HIGH}		5.60		6.30	V
Hysteresis	V_{HY2}			50		mV

Table 3

[1] If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A 6170.
[2] The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
[3] Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.
[4] The dropout voltage is defined as the INPUT to OUTPUT voltage differential at which the OUTPUT voltage drops 100 mV below its nominal measured at a 1 V differential.
[5] Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.
[6] The comparator and the voltage regulator have separate voltage references (see "Block Diagram" Fig. 7).
[7] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 4).
[8] The level detector of V_{OUTPUT} (V_{HIGH}) is the level when V_{OUTPUT} is rising. The level detector when V_{OUTPUT} is falling equals V_{HIGH} minus the hysteresis (V_{HY2}) (see Fig. 4).

Timing Characteristics

V_{INPUT} = 6.0 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD}/40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

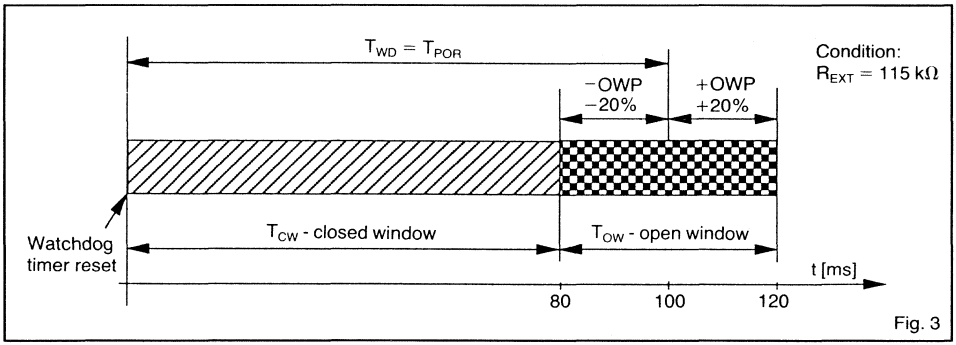


Fig. 3

Voltage Monitoring

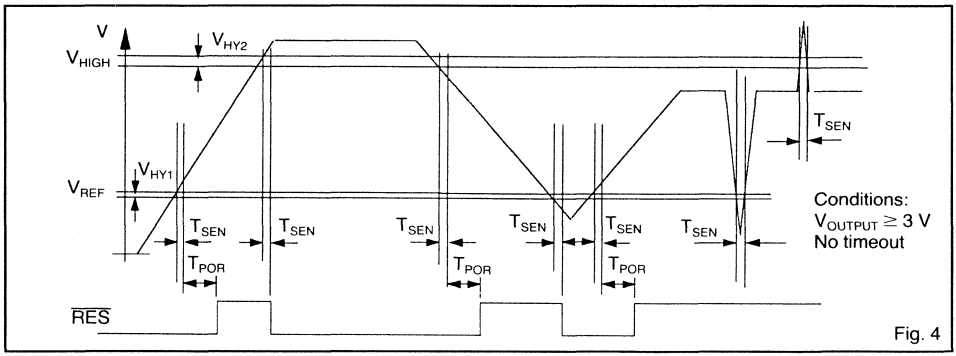


Fig. 4

Timer Reaction

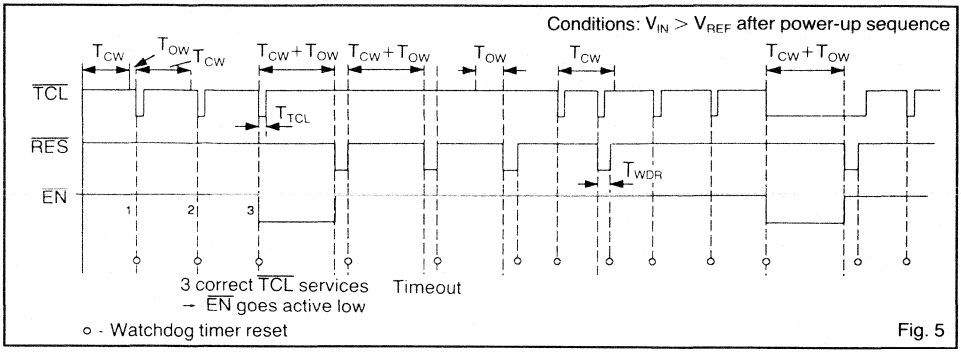


Fig. 5

Combined Voltage and Timer Reaction

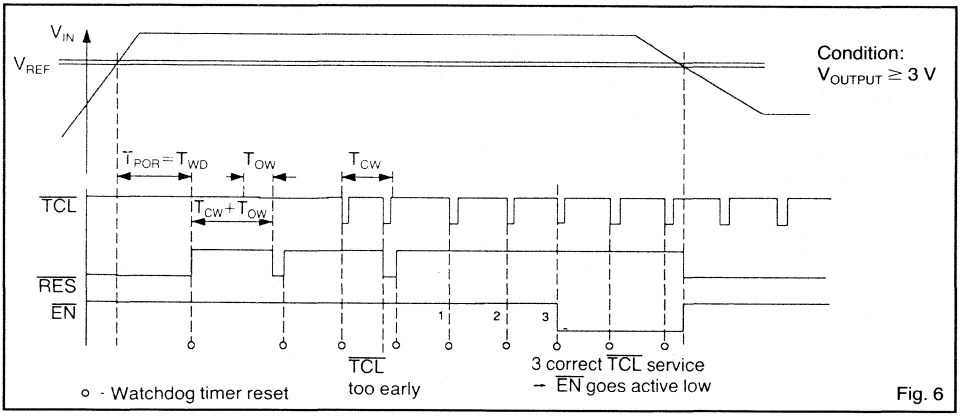


Fig. 6

Block Diagram

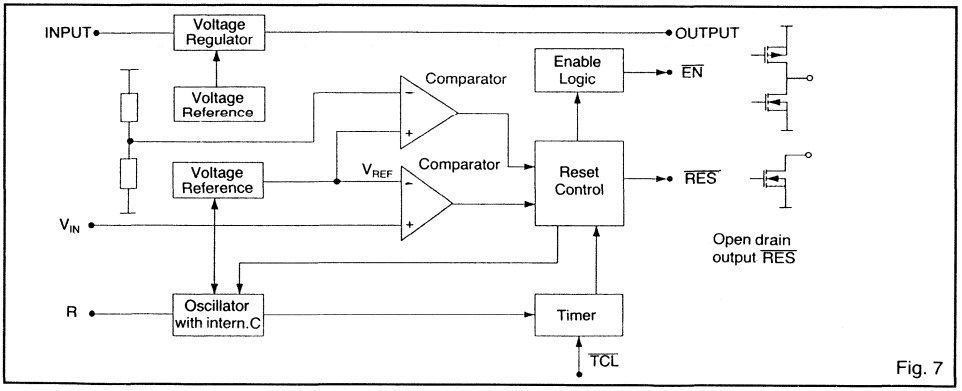


Fig. 7

Pin Description

Pin	Name	Function
1	$\overline{EN}$	Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	INPUT	Voltage regulator input
6	OUTPUT	Voltage regulator output
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

Voltage Regulator

The A 6170 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 155 μA) makes the A 6170 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 3.36 V to 26 V for operation and the input protection includes both reverse battery (negative transients up to 20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 8). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about −30°C, so tantalums are recommended for operation below −25°C. The important parameters of the 22 μF capacitor are an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A 6170 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Care must be taken not to exceed the maximum junction temperature (+70°C). The power dissipation within the A 6170 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (70°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (ie. ≥ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A 6170 in DIP8 package will have an effective thermal resistance from the junction to the ambient of about 10°C/W for a single 100 ms pulse.

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 8. The user uses the external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 4). After INPUT reaches 3.36 V (and so OUTPUT reaches at least 3 V) and V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Voltage Window

The reset output ($\overline{RES}$) is inactive when V_{IN} is higher than V_{REF} and when V_{OUTPUT} is lower than V_{HIGH}. If V_{IN} is less than V_{REF} or V_{OUTPUT} higher than V_{HIGH}, the reset output goes active low (see Fig. 4).

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 8) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With R_{EXT} = 115 kΩ typical values are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 3) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if $T_{WD} = 100$ ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms ($T_{CW} = 80$ ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically $R_{EXT} \times 0.87$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if $R_{EXT} = 115$ kΩ then $T_{WD} = 100$ ms ±10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD} / 40 = 2.5$ ms typically (see Fig. 5).

With the open window constraint new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though software is malfunctioning; the A 6170 would make a system reset because the watchdog would be cleared too quickly.

If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 8).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 µs overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable − $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The A 6170 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

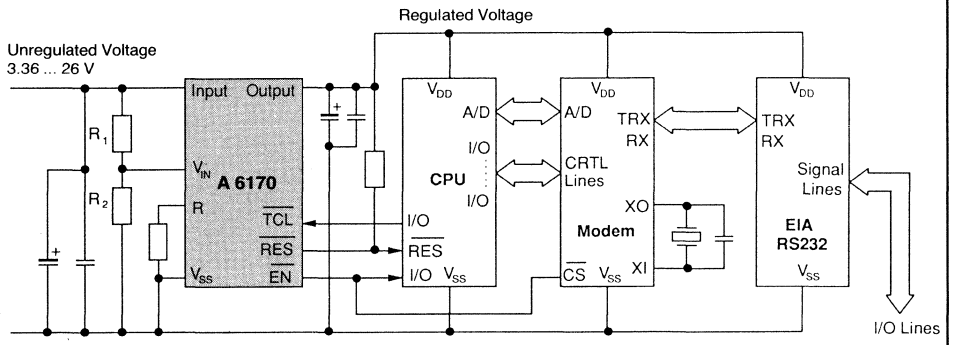


Fig. 8

OUTPUT Current versus INPUT Voltage

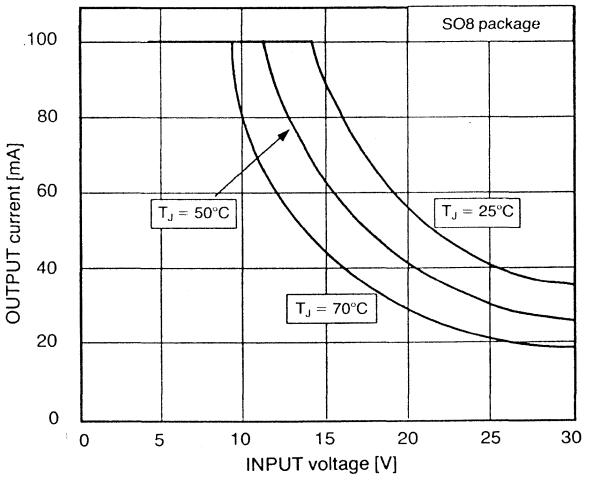


Fig. 9

T_{WD} versus Temperature at 5 V

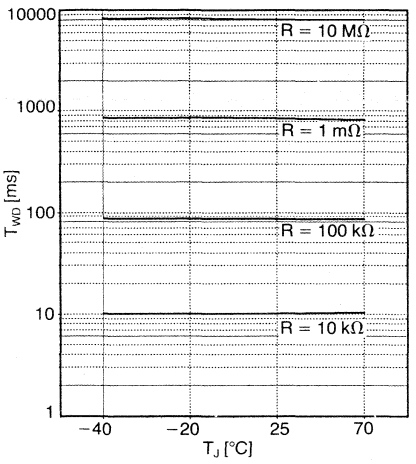


Fig. 10

T_{WD} versus R at 5 V

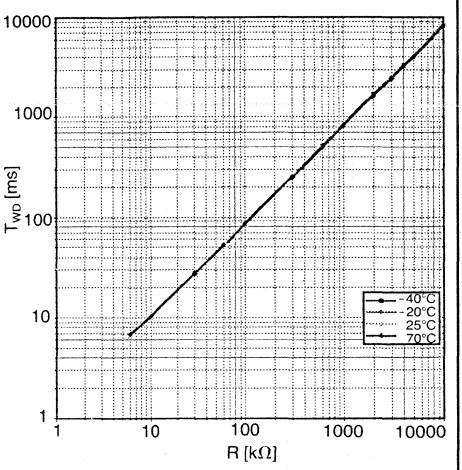


Fig. 11

T_{WD} versus V_{OUTPUT} at T_J = +25°C

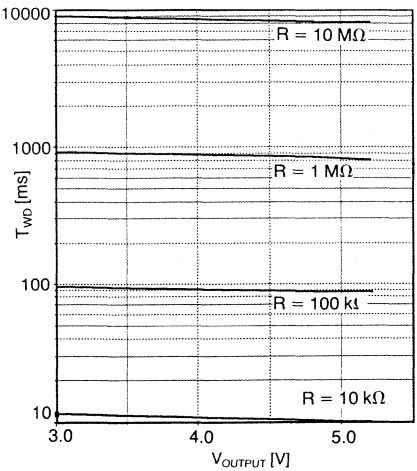


Fig. 12

T_{WD} versus R at T_J = +25°C

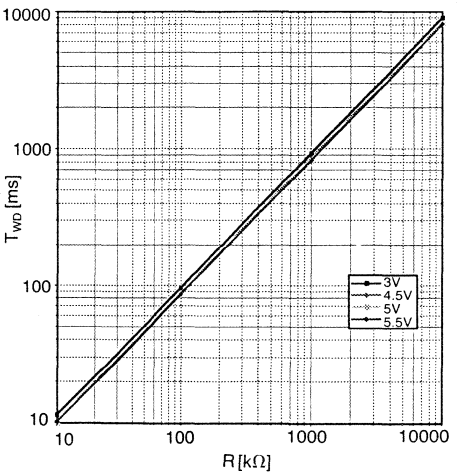


Fig. 13

8

T_{WD} versus R at T_J = +25°C

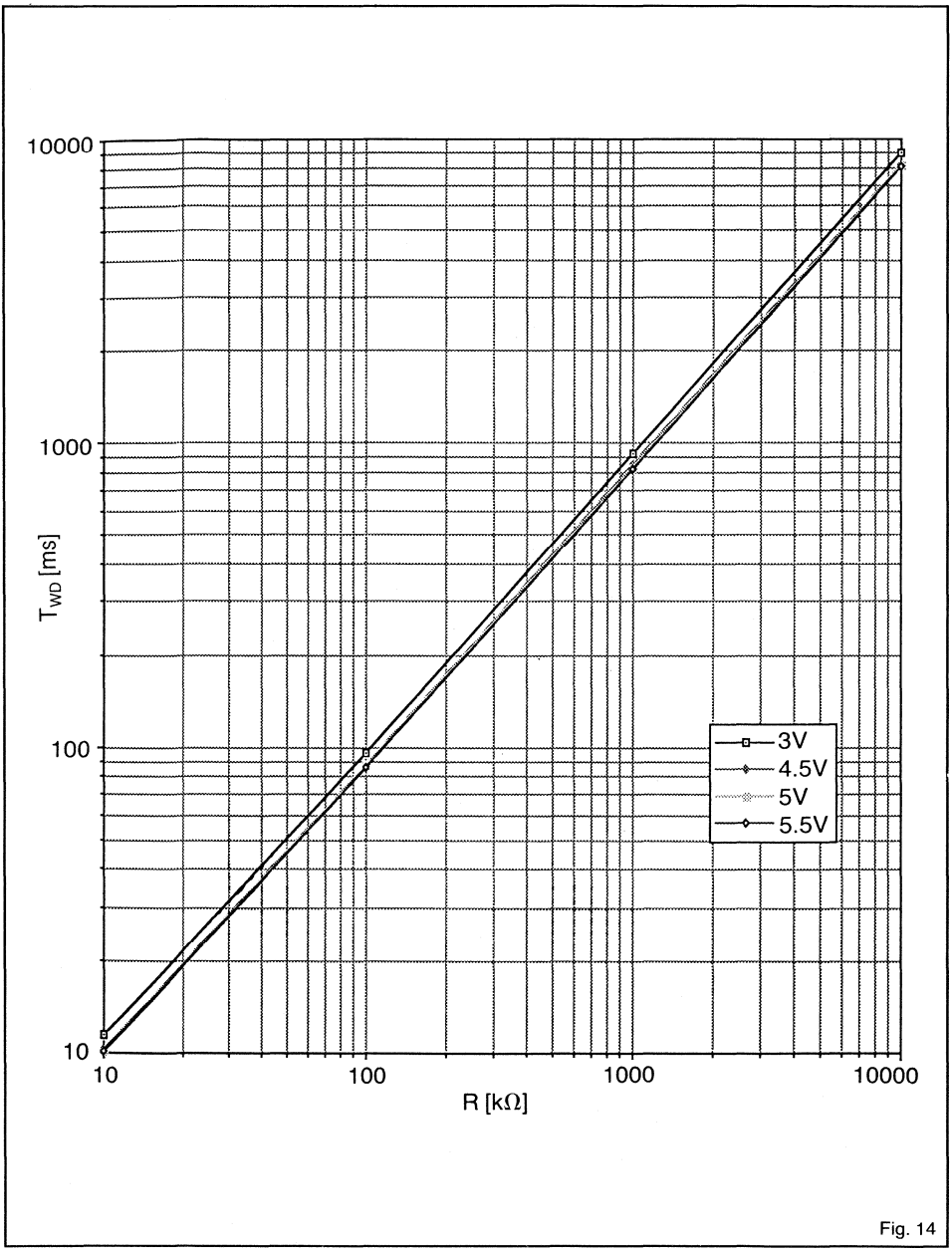


Fig. 14

T_{WD} versus V_{OUTPUT} at T_J = +70°C

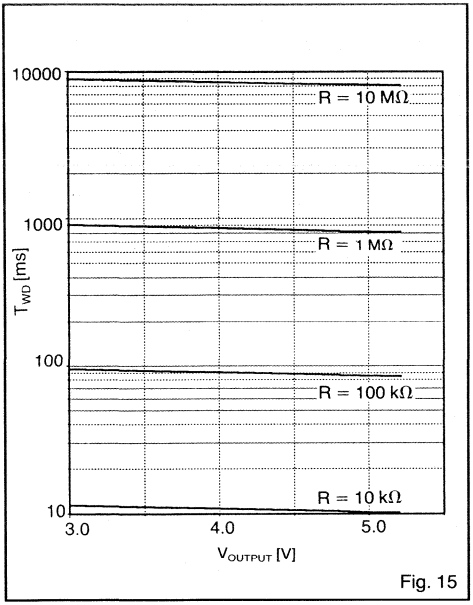


Fig. 15

T_{WD} versus R at T_J = +70°C

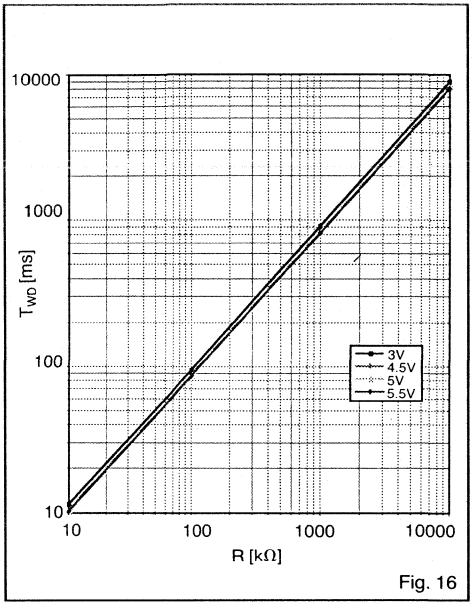


Fig. 16

T_{WD} versus V_{OUTPUT} at T_J = −40°C

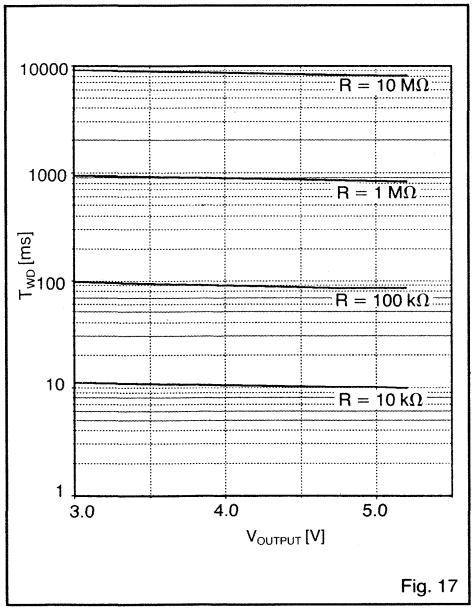


Fig. 17

T_{WD} versus R at T_J = −40°C

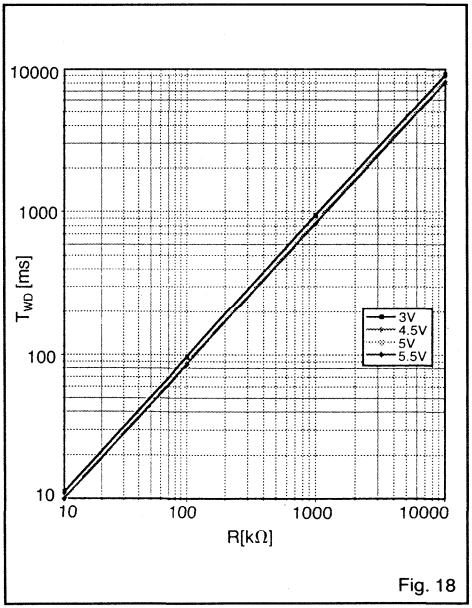
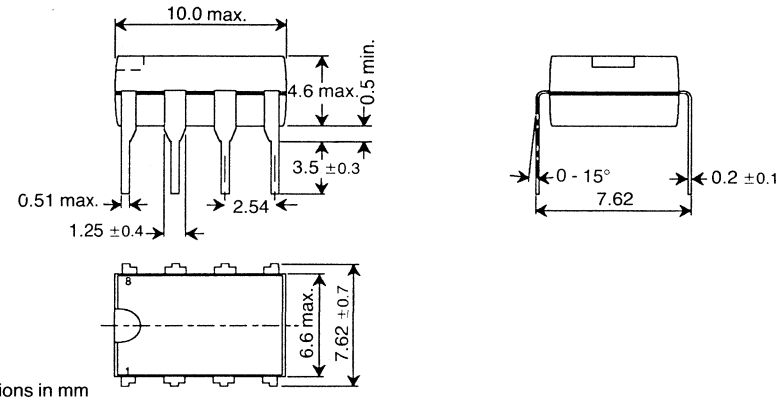


Fig. 18

8

Package and Ordering Information

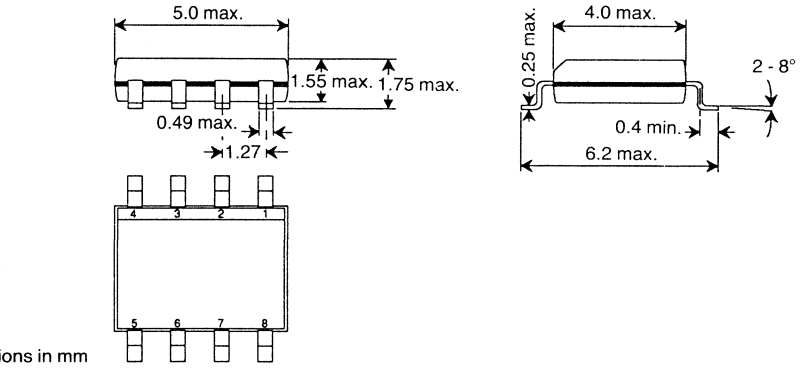
Dimensions of DIP8 Package



Dimensions in mm

Fig. 19

Dimensions of SO8 Package



Dimensions in mm

Fig. 20

Ordering Information

The A 6170 is available in the following packages:

Type	Package
A 6170 8P	DIP8
A 6170 8S	SO8

When ordering please specify complete part number.

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A 6173

Regulator & Watchdog

Features

- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 250 mV at 100 mA
- Low quiescent current, typically 155 μA
- Standby mode, maximum current 240 μA (without load on OUTPUT)
- Unregulated DC input can withstand −20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 3.0 V
- Reset output guaranteed for regulated output voltage down to 1.2 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Comparator for voltage monitoring, reset threshold 1.17V
- ± 1.5% voltage threshold tolerance at 25°C
- ± 3% voltage threshold tolerance from −40 to +70°C
- Programmable reset voltage monitoring
- Voltage window, high threshold 5.9 V
- Programmable power on reset (POR) delay
- Watchdog with programmable time windows guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ±10%
- System enable output offers added security
- 3 chip select feed-thru circuit controlled by $\overline{EN}$
- TTL/CMOS compatible
- −40°C to +70°C temperature range
- DIP14 and SO14 packages

Description

The A 6173 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring in an 14 lead package. The voltage regulator has a low dropout voltage (typ. 250 mV at 100 mA) and a low quiescent current (155 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage transient of −20 V (reverse battery). The input may be connected to ground or a reverse voltage without reverse current flow from the output to the input. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies

Typical Operating Configuration

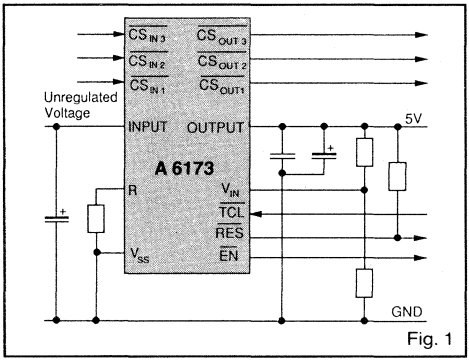


Fig. 1

Pin Assignment

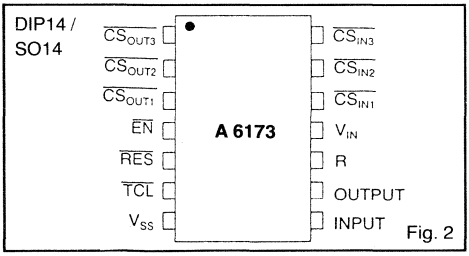


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	−0.3 to +30 V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	−20 to +60 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+70	°C
INPUT voltage [1]	V_{INPUT}	3.36		26	V
OUTPUT voltage [1] [2]	V_{OUTPUT}	3.0			V
$\overline{RES}$ & $\overline{EN}$ guaranteed [3]	V_{OUTPUT}	1.2			V
OUTPUT current [4]	I_{OUTPUT}			100	mA
Comparator input voltage	V_{IN}	0		V_{OUTPUT}	V
RC-oscillator programming	R	10		1000	kΩ
Thermal resistance from junction to ambient [5]					
– DIP14	$R_{th(j-a)}$			100	°C/W
– SO14	$R_{th(j-a)}$			150	°C/W

Table 2

[1] Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 µF capacitor or greater is required on the INPUT, see Fig. 9. The 22 µF must have an effective resistance ≤ 5 Ω and a resonant frequency above 500 kHz.

[2] A 10 µF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 µF must have an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

[3] $\overline{RES}$ must be pulled up externally to V_{OUTPUT} even if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

[4] The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A 6173 to work above the maximum junction temperature (70°C) must be avoided.

[5] The thermal resistance specified assumes the package is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 100 µA			240	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 µA		155	300	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 mA		1.7	4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88		5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA, −40°C ≤ T_J ≤ 70°C	4.85		5.15	V
Output voltage temperature coefficient [2]	$V_{th(coeff)}$			50	180	ppm/°C
Line regulation [3]	V_{LINE}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = 70°C		0.2	0.5	%
Load regulation [3]	V_L	100 µA ≤ I_L ≤ 100 mA		0.2	0.6	%
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 µA		40	170	mV
Dropout voltage [4]	$V_{DROPOUT}$	I_L = 100 mA			420	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, I_L = 100 µA, R_{EXT} = 100 kΩ, O/Ps 1 MΩ to V_{OUTPUT}, I/Ps at V_{OUTPUT}		300	560	µA
Thermal regulation [5]	V_{thr}	T_J = 25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms		0.05	0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}			450	mA
OUTPUT noise, 10Hz to 100kHz	V_{NOISE}			200		µV rms

3.0 ≤ V_{OUTPUT} ≤ 5.5 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

$\overline{RES}$, $\overline{EN}$ and $\overline{CS}_{OUT1/2/3}$						
Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$ and $\overline{CS}_{OUT1/2/3}$						
Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{OUTPUT} = 2.0 V, I_{OH} = −100 µA	1.8	1.9		V
	V_{OH}	V_{OUTPUT} = 1.2 V, I_{OH} = −30 µA	1.0	1.1		V
$\overline{TCL}$, V_{IN} and $\overline{CS}_{IN1/2/3}$						
$\overline{TCL}$ and $\overline{CS}_{IN1/2/3}$ Input Low Level	V_{IL}			V_{SS}	0.8	V
$\overline{TCL}$ and $\overline{CS}_{IN1/2/3}$ Input High Level	V_{IH}		2.0		V_{OUTPUT}	V
Leakage current $\overline{TCL}$ input	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference [6][7]	V_{REF}	T_J = 25°C	1.148	1.170	1.200	V
	V_{REF}	T_J = −20°C to +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis [7]	V_{HY1}			2		mV
Level detector of V_{OUTPUT} [8]	V_{HIGH}	T_J = 25°C	5.78	5.95	6.12	V
	V_{HIGH}		5.60		6.30	V
Hysteresis	V_{HY2}			50		mV

Table 3

[1] If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A 6173.

[2] The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

[3] Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.

[4] The dropout voltage is defined as the INPUT to OUTPUT voltage differential at which the OUTPUT voltage drops 100 mV below its nominal measured at a 1 V differential.

[5] Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.

[6] The comparator and the voltage regulator have separate voltage references (see "Block Diagram" Fig. 8).

[7] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

[8] The level detector of V_{OUTPUT} (V_{HIGH}) is the level when V_{OUTPUT} is rising. The level detector when V_{OUTPUT} is falling equals V_{HIGH} minus the hysteresis (V_{HY2}) (see Fig. 5).

8

Timing Characteristics

V_{INPUT} = 6.0 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at rising edge	T_{CSH}			125	200	ns
$\overline{CS_{INx}}$ to $\overline{CS_{OUTx}}$ at falling edge	T_{CSL}			75	150	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 115 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 115 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 115 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 115 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

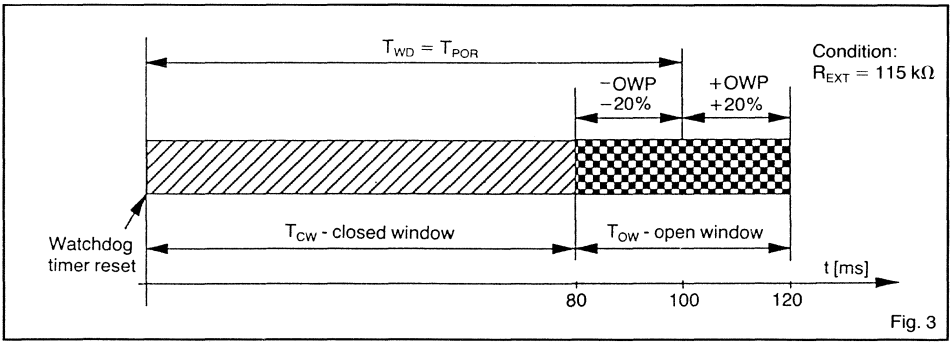


Fig. 3

Chip Select

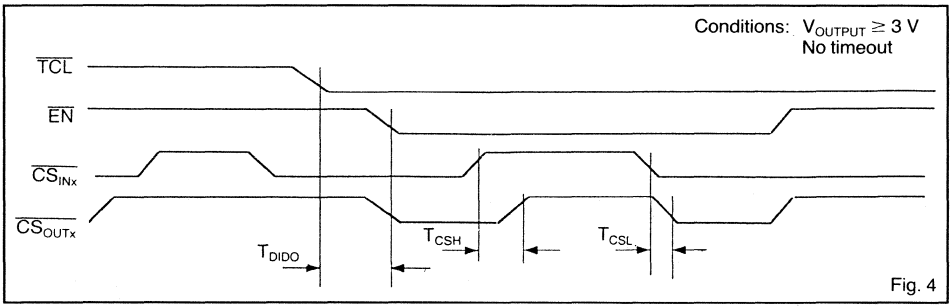


Fig. 4

Voltage Monitoring

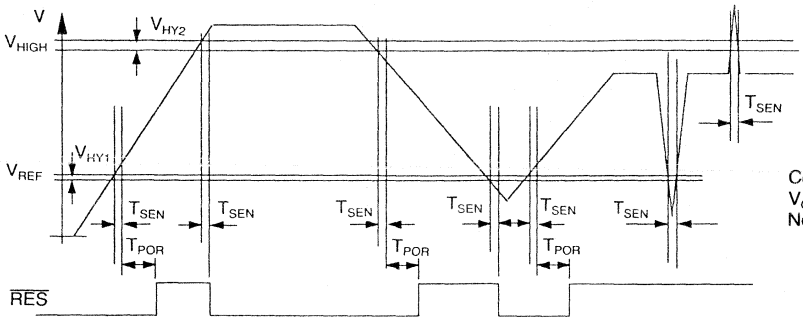


Fig. 5

Timer Reaction

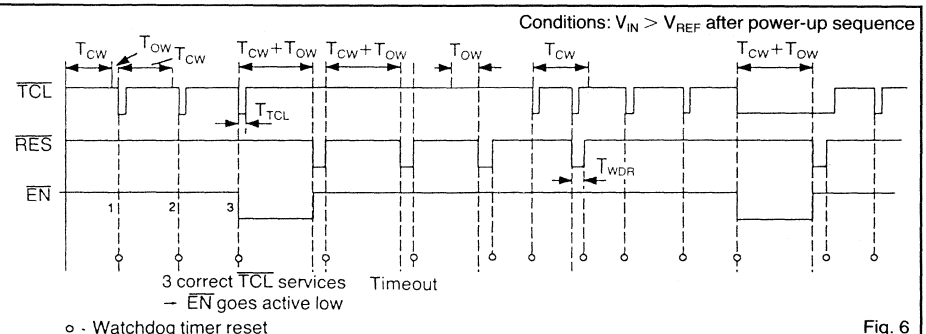


Fig. 6

Combined Voltage and Timer Reaction

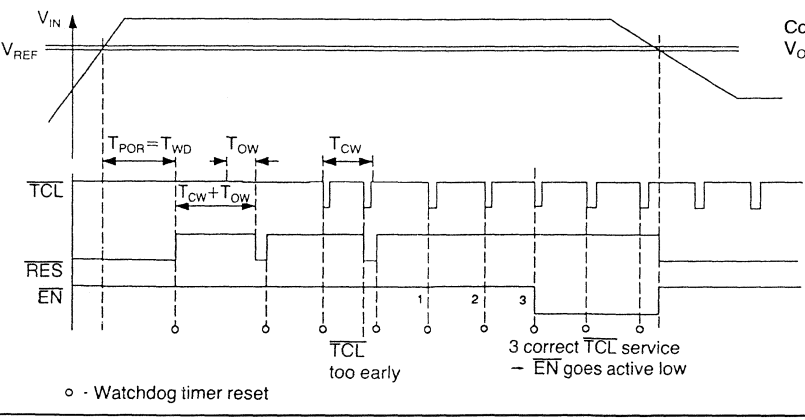


Fig. 7

Block Diagram

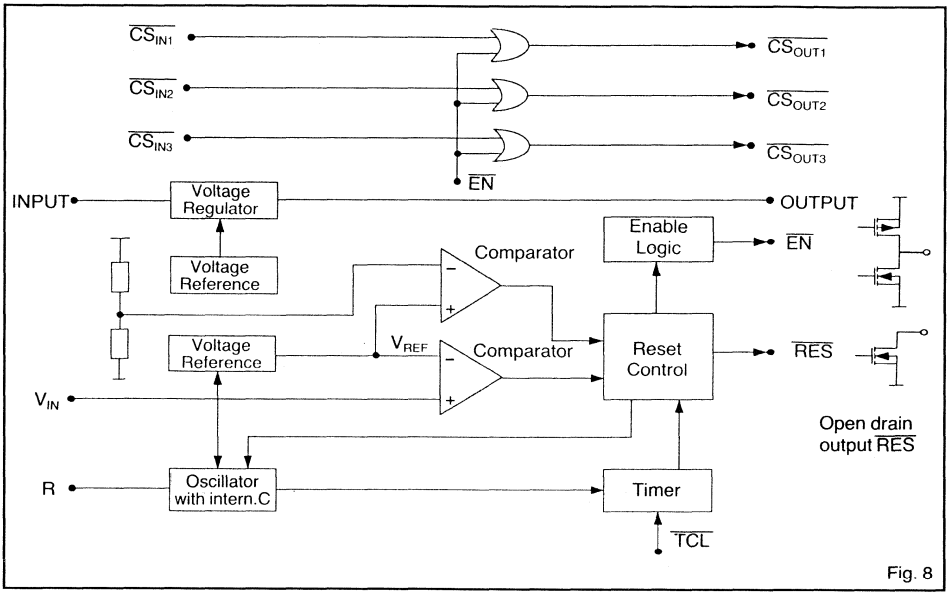


Fig. 8

Pin Description

Pin	Name	Function
1	$\overline{CS}_{OUT3}$	Push-pull active low chip select output 3
2	$\overline{CS}_{OUT2}$	Push-pull active low chip select output 2
3	$\overline{CS}_{OUT1}$	Push-pull active low chip select output 1
4	$\overline{EN}$	Push-pull active low enable output
5	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
6	TCL	Watchdog timer clear input signal
7	V_{SS}	GND terminal
8	INPUT	Voltage regulator input
9	OUTPUT	Voltage regulator output
10	R	R_{EXT} input for RC oscillator tuning
11	V_{IN}	Voltage comparator input
12	$\overline{CS}_{IN1}$	Chip select input 1
13	$\overline{CS}_{IN2}$	Chip select input 2
14	$\overline{CS}_{IN3}$	Chip select input 3

Table 5

Functional Description

Voltage Regulator

The A 6173 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 155 μA) makes the A 6173 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 3.36 V to 26 V for operation and the input protection includes both reverse battery (negative transients up to 20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 9). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about −30°C, so tantalums are recommended for operation below −25°C. The important parameters of the 22 μF capacitor are an effective series resistance of $\leq 5\ \Omega$ and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A 6173 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Care must be taken not to exceed the maximum junction

temperature (+70°C). The power dissipation within the A 6173 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (70°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (ie. ≥ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A 6173 in DIP14 package will have an effective thermal resistance from the junction to the ambient of about 9°C/W for a single 100 ms pulse.

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 9. The user uses the external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5). After INPUT reaches 3.36 V (and so OUTPUT reaches at least 3 V) and V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 115 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 µs.

Voltage Window

The reset output ($\overline{RES}$) is inactive when V_{IN} is higher than V_{REF} and when V_{OUTPUT} is lower than V_{HIGH}. If V_{IN} is less than V_{REF} or V_{OUTPUT} higher than V_{HIGH}, the reset output goes active low (see Fig. 5).

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$). With R_{EXT} = 115 kΩ typical values are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 3) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms − 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following formula for servicing signal $\overline{TCL}$ during the open window: Typically $R_{EXT} \times 0.87$ where R_{EXT} is in kΩ for T_{WD} in ms (the formula is valid for $R_{EXT} \geq 70$ kΩ). For example, if R_{EXT} = 115 kΩ then T_{WD} = 100 ms ±10% and the useful open window limits for software are 90 to 110 ms.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period a short watchdog $\overline{RES}$ pulse is generated which is equal to $T_{WD}/40$ = 2.5 ms typically (see Fig. 6).

With the open window constraint new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though software is malfunctioning; the A 6173 would make a system reset because the watchdog would be cleared too quickly.

If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output").

The $\overline{RES}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 9).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the

watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable – $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The A 6173 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

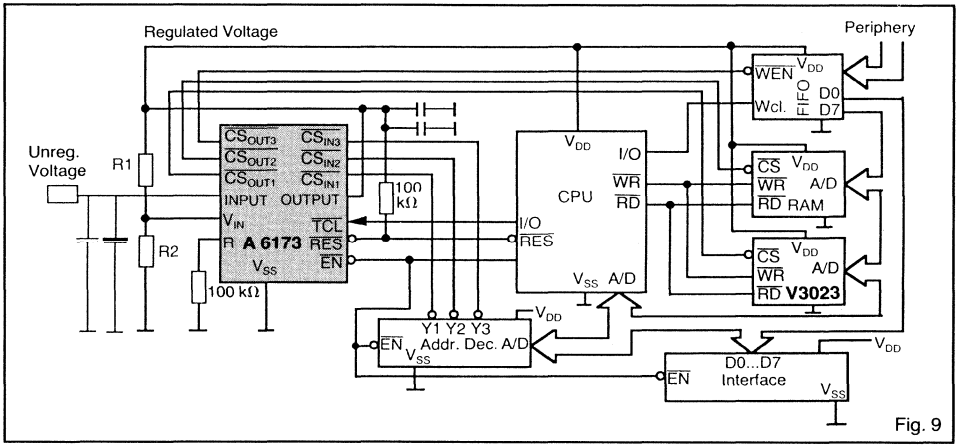


Fig. 9

OUTPUT Current Versus INPUT Voltage

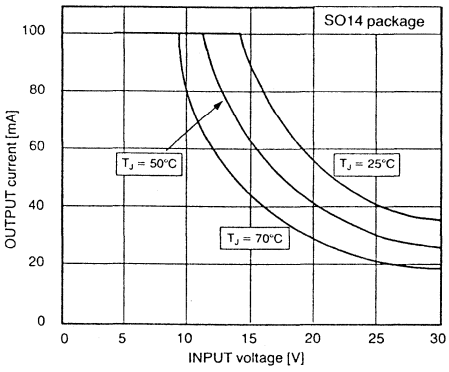


Fig. 10

T_{WD} versus Temperature at 5 V

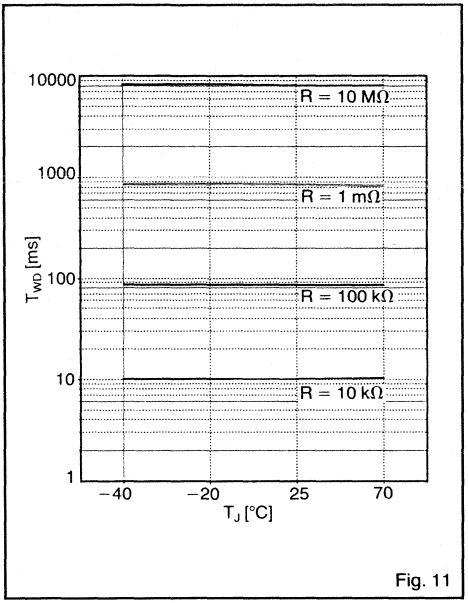


Fig. 11

T_{WD} versus R at 5 V

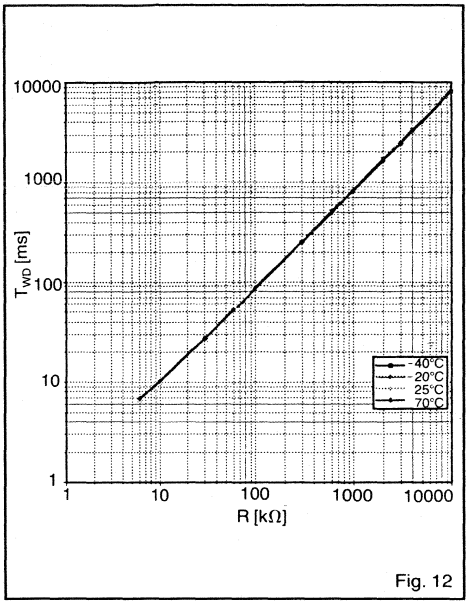


Fig. 12

T_{WD} versus V_{OUTPUT} at T_J = +25°C

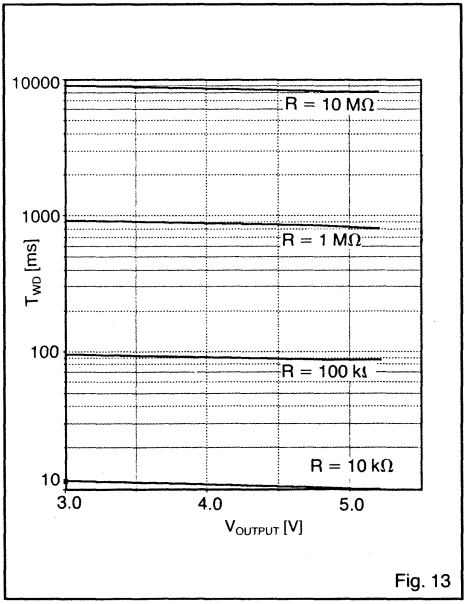


Fig. 13

T_{WD} versus R at T_J = +25°C

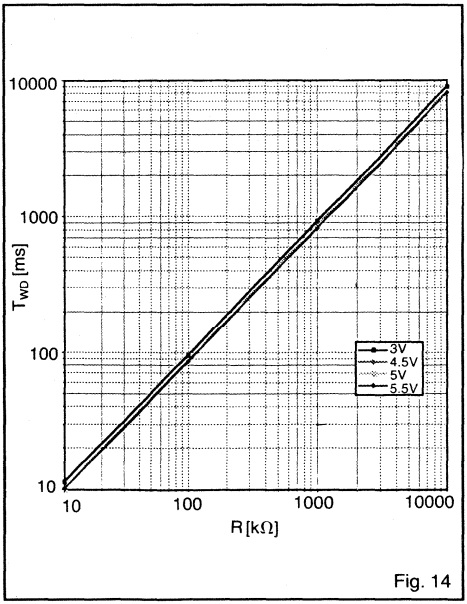


Fig. 14

8

T_{WD} versus R at $T_J = +25°C$

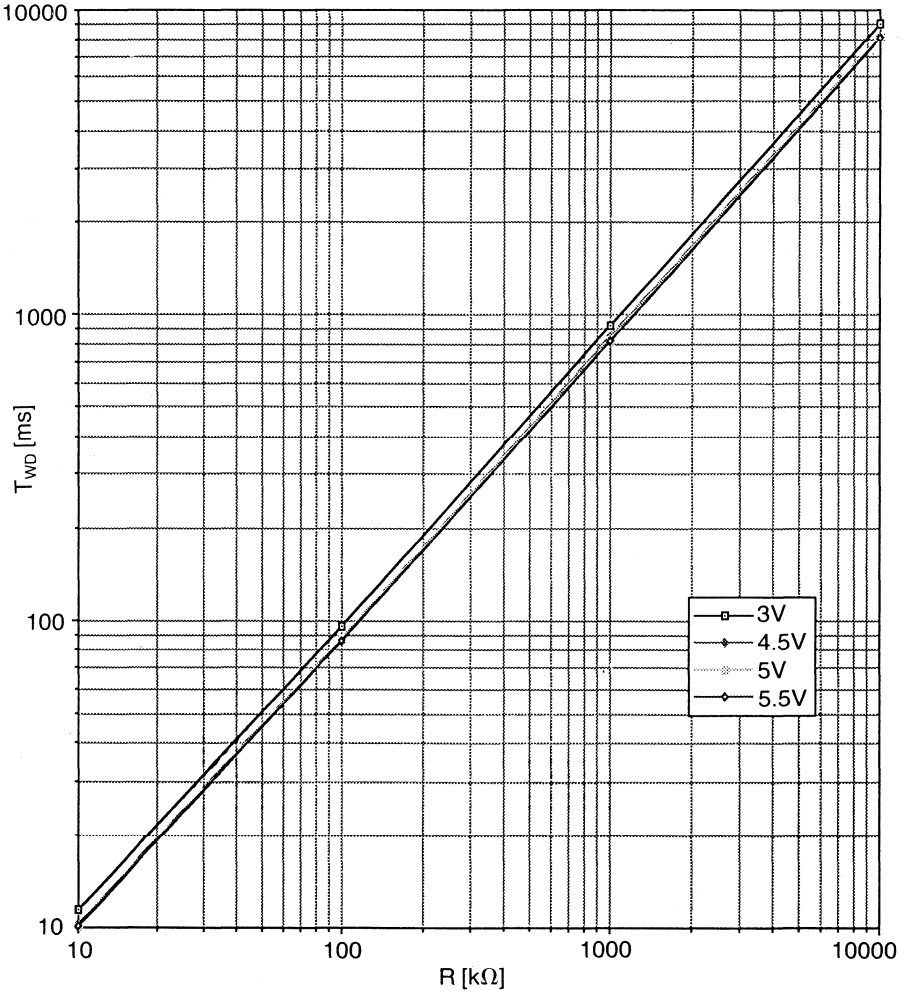


Fig. 15

T_{WD} versus V_{OUTPUT} at $T_J = +70°C$

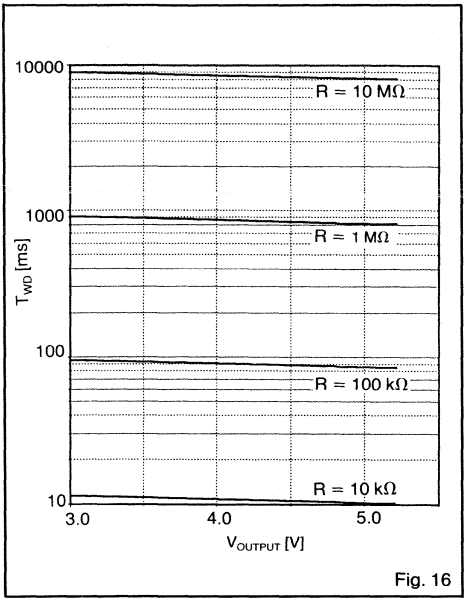


Fig. 16

T_{WD} versus R at $T_J = +70°C$

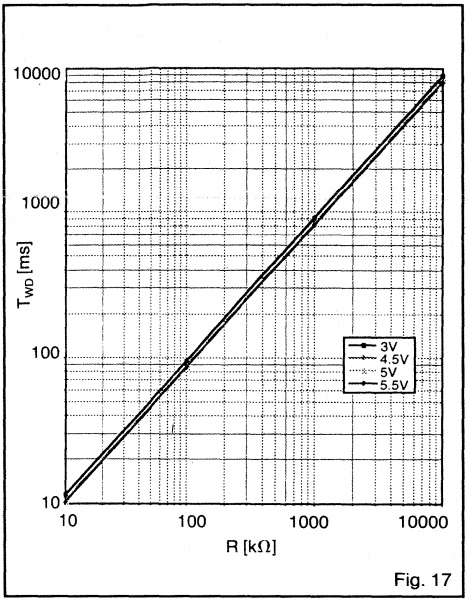


Fig. 17

T_{WD} versus V_{OUTPUT} at $T_J = -40°C$

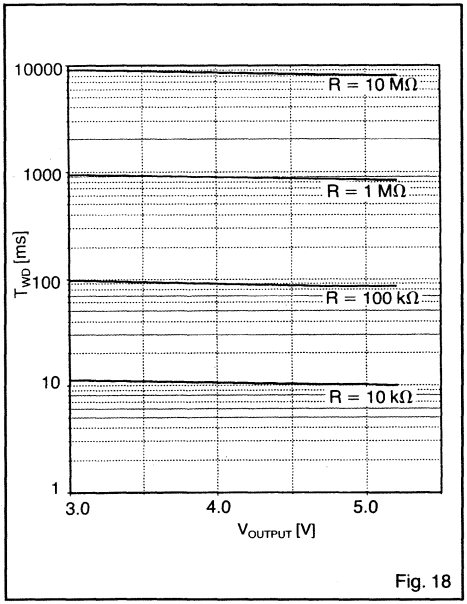


Fig. 18

T_{WD} versus R at $T_J = -40°C$

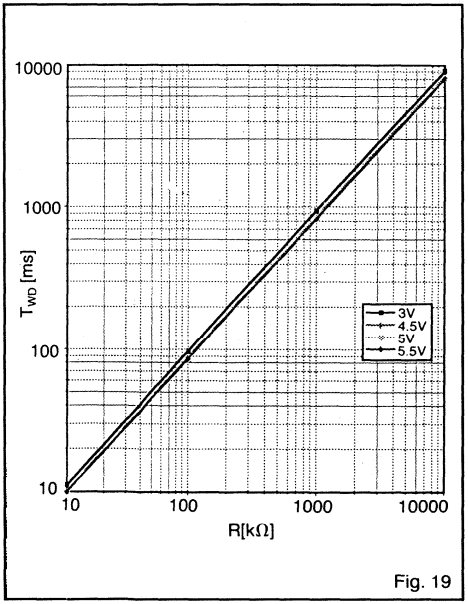
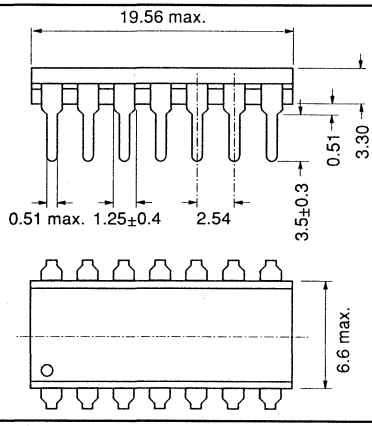


Fig. 19

8

Package and Ordering Information

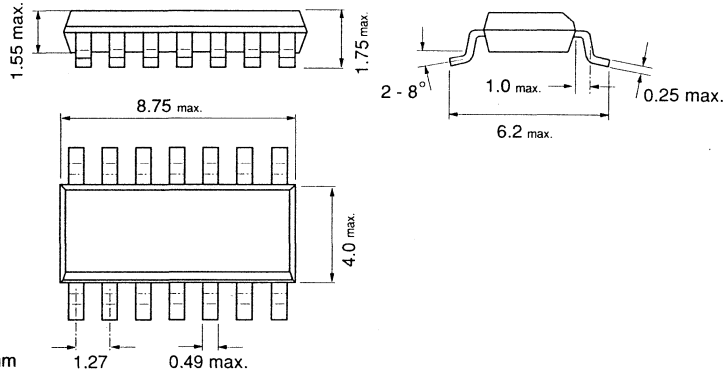
Dimensions of DIP14 Package



Dimensions in mm

Fig. 20

Dimensions of SO14 Package



Dimensions in mm

Fig. 21

Ordering Information

The A 6173 is available in the following packages:

Type	Package
A 6173 14P	DIP14
A 6173 14S	SO14

When ordering please specify complete part number.

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Regulator with Smart Reset

Features

- Supply voltage monitoring
- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 250 mV at 100 mA
- Low quiescent current, typically 100 μA
- Standby mode, maximum current 210 μA (without load on OUTPUT)
- Unregulated DC input can withstand −20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 1 V
- Reset output guaranteed for regulated output voltage down to 1 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Clear microprocessor restart after power up
- Time base accuracy ± 10%
- Push-pull or Open drain output
- −40°C to +85°C temperature range
- DIP8 and SO8 packages

Description

The A 6300 offers a high level of integration by combining voltage regulation and voltage monitoring. The voltage regulator has a low dropout voltage (typ. 250 mV at 100 mA) and a low quiescent current (100 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage transient of −20 V (reverse battery). The INPUT may be connected to ground or a reverse voltage without reverse current flow from the OUTPUT to the INPUT. Upon the OUTPUT voltage rising above V_{TH}, the reset output, whether RES or $\overline{RES}$, will remain active (Res = 1, $\overline{RES}$ = 0) for an additional time of 50 ms. This allows the system voltage and the oscillator of the microprocessor to stabilize before they becomes fully active. When V_{OUTPUT} falls below V_{TH}, the reset output goes active. Threshold voltage can be obtained in different versions: 2 V, 2.4 V, 2.8 V, 3.5 V, 4 V.

Applications

- White / brown goods
- Industrial electronics
- Automotive electronics
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies

Typical Operating Configuration

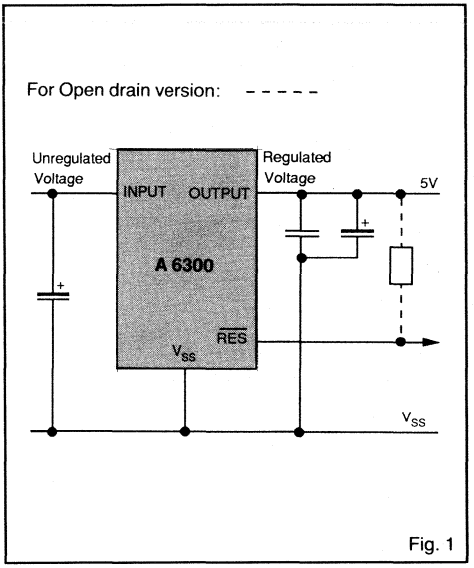


Fig. 1

Pin Assignment

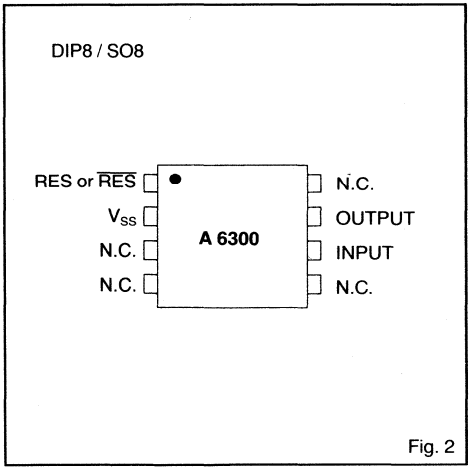


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	−0.3 to +30 V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	−20 to +60 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} −0.3V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	−40		+85	°C
INPUT voltage [1]	V_{INPUT}	2.3		26	V
OUTPUT voltage [1)2)]	V_{OUTPUT}	1.0			V
Reset output guaranteed	V_{OUTPUT}	1.0			V
OUTPUT current [3]	I_{OUTPUT}			100	mA
Thermal resistance from junction to ambient [4]					
– DIP8	$R_{th(j-a)}$			105	°C/W
– SO8	$R_{th(j-a)}$			160	°C/W

Table 2

1) Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 μF capacitor or greater is required on the INPUT, see Fig. 6. The 22 μF must have an effective resistance $\leq 5\ \Omega$ and a resonant frequency above 500 kHz.

2) A 10 μF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 μF must have an effective series resistance of $\leq 5\ \Omega$ and a resonant frequency above 500 kHz.

3) The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A 6300 to work above the maximum junction temperature (85°C) must be avoided.

4) The thermal resistance specified assumes the pakkage is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Min. 25°C	Typ.	Max. 25°C	Max.	Unit
Supply current in standby mode	I_{SS}	Reset output open, I_L = 100 µA			100		210	µA
Supply current[1]	I_{SS}	Reset output open, I_L = 100 mA			1.7		4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88				5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA	4.85				5.15	V
Output voltage temperature coefficient[2]	$V_{th(coeff)}$				50		180	ppm/°C
Line regulation[3]	V_{Line}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = 85°C			0.2		0.5	%
Load regulation[3]	V_L	100 µA ≤ I_L ≤ 100 mA			0.2		0.6	%
Dropout voltage[4]	$V_{DROPOUT}$	I_L = 100 µA			40		170	mV
Dropout voltage[4]	$V_{DROPOUT}$	I_L = 100 mA					420	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, i_L = 100 µA			300		560	µA
Thermal regulation[5]	V_{thr}	T_J = 25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms			0.05		0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}					450	mA
OUTPUT moise, 10 Hz to 100 kHz	V_{NOISE}				200			µV rms
Threshold voltage	V_{TH}	Version: AA, AG, AM	1.77	1.84	1.95	2.04	2.17	V
	V_{TH}	Version: AB, AH, AN	2.09	2.18	2.32	2.41	2.55	V
	V_{TH}	Version: AC, AI, AO	2.48	2.59	2.73	2.86	3.03	V
	V_{TH}	Version: AD, AJ, AP	3.11	3.23	3.42	3.59	3.80	V
	V_{TH}	Version: AE, AK, AQ	3.55	3.70	3.88	4.08	4.32	V
Threshold hysteresis	V_{HYS}				25			mV
RES Output Low Level	V_{OL}	V_{OUTPUT} = 5 V, I_{OL} = 8 mA			175		400	mV
	V_{OL}	V_{OUTPUT} = 3 V, I_{OL} = 4 mA			140		300	mV
	V_{OL}	V_{OUTPUT} = 1 V, I_{OL} = 50 µA			20		90	mV
RES Output High Level	V_{OH}	V_{OUTPUT} = 5 V, I_{OH} = −8 mA	4.3		4.5			V
	V_{OH}	V_{OUTPUT} = 3 V, I_{OH} = −4 mA	2.3		2.6			V
	V_{OH}	V_{OUTPUT} = 1 V, I_{OH} = −100 µA	850		970			mV
Leakage current[6]	I_{LEAK}	V_{OUTPUT} = 5 V			0.05		1	µA

Table 3

1) If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A 6300.
2) The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
3) Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.
4) The dropout voltage is defined as the INPUT to OUTPUT voltage differential at which the OUTPUT voltage drops 100 mV below its nominal measured at a 1 V differential.
5) Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.
6) Only for open drain versions.

Timing Characteristics

V_{OUTPUT} = 5.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_j = −40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power-on Reset time	t_{POR}		25	50	75	ms
Sensitivity[1)]	t_{SEN}	V_{OUTPUT} = 5 V to 3 V in 5 µs	20	0.8 · t_R		µs
Propagation time[1)]	t_R	V_{OUTPUT} = 5 V to 3 V in 5 µs	22	75	150	µs

Table 4

Timing Waveforms

Voltage Monitoring

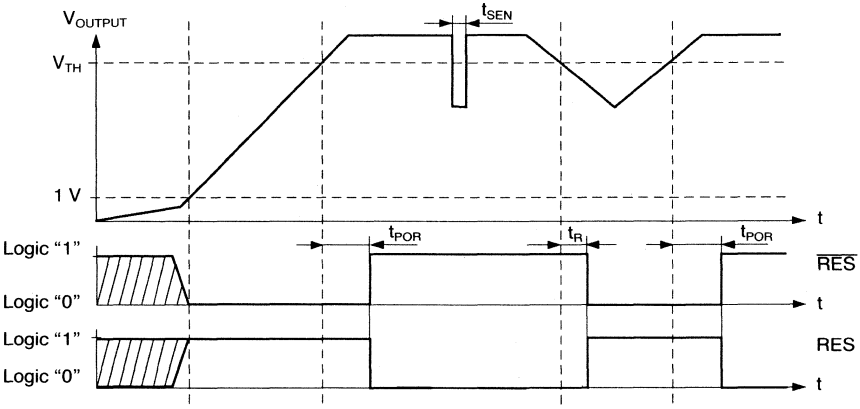


Fig. 3

Block Diagram

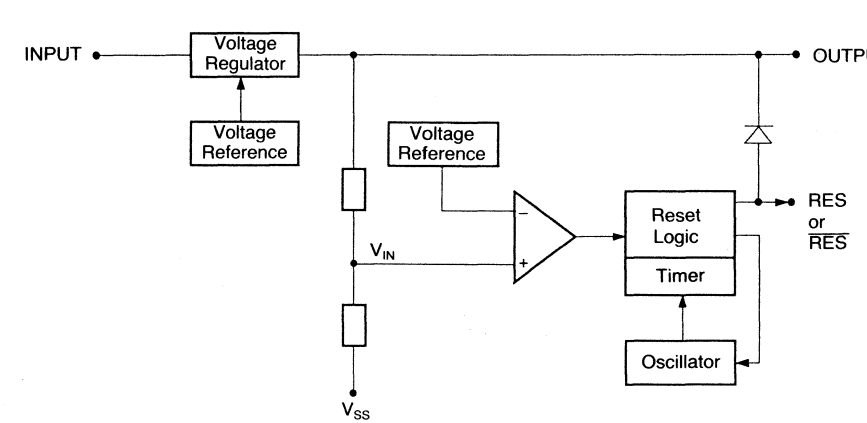


Fig. 4

Pin Description

Pin	Name	Function
1	RES or $\overline{RES}$	Reset output
2	V_{SS}	Supply ground
3	N.C.	Not connected
4	N.C.	Not connected
5	N.C.	Not connected
6	INPUT	Unregulated positive supply
7	OUTPUT	Regulated output
8	N.C.	Not connected

Table 5

Functional Description

Voltage Regulator

The A 6300 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 100 μA) makes the A 6300 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 2.3 V to 26 V for operation and the input protection includes both reverse battery (negative transients up to 20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 5). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about −30°C, so tantalums are recommended for operation below −25°C. The important parameters of the 22 μF capacitor are an effective series resistance of $\leq 5\ \Omega$ and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A 6300 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Voltage Monitoring

The power-on reset and the power-down reset are generated internally with a voltage comparison of the voltage reference and the resistor divider (see Fig. 4).

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 3). After OUTPUT reaches V_{TH}, the $\overline{RES}$ output is held low for an additional power-on reset delay t_{POR} (typically 50 ms). The power-on reset delay prevents repeated toggling of $\overline{RES}$ even if V_{OUTPUT} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to stabilize and to ensure correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{OUTPUT} falls below V_{TH}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 70 μs.

Temperature Consideration

Care must be taken not to exceed the maximum junction temperature (85°C). The power dissipation within the A 6300 is given by the formula:

$$T_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{max} = (85°C - T_A) / R_{th(j\text{-}a)}$$

where $R_{th(j\text{-}a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j\text{-}a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (i.e. $\geq$ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A 6300 in DIP8 package will have an effective thermal resistance from the junction to the ambient of about 10°C/W for a single 100 ms pulse.

OUTPUT Current versus INPUT Voltage

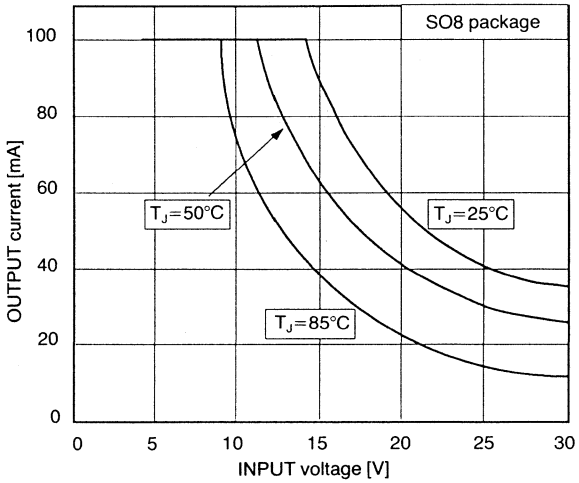


Fig. 5

Typical Application

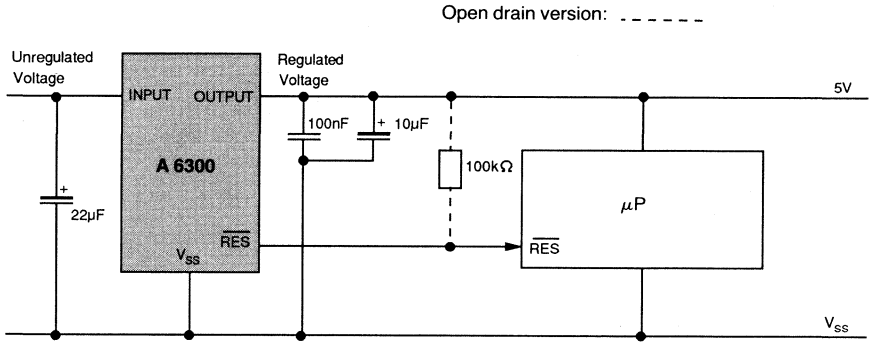
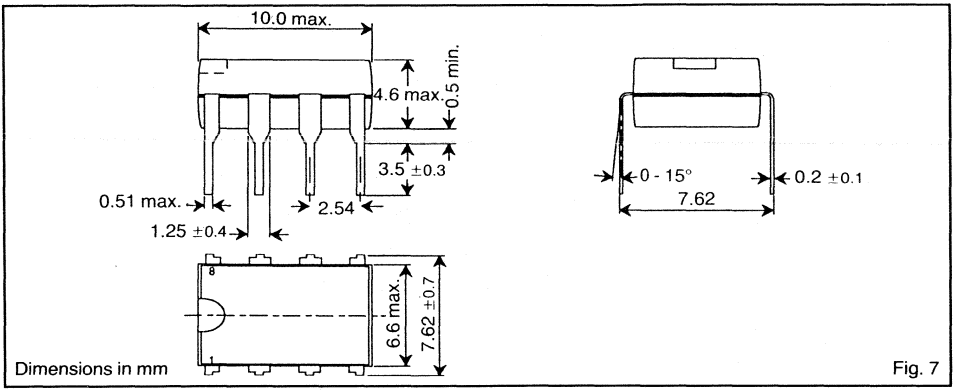


Fig. 6

Package and Ordering Information

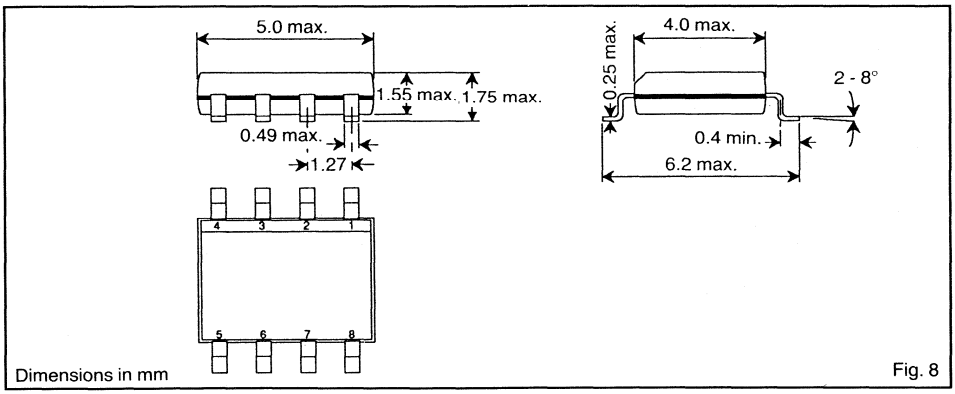
Dimensions of DIP8 Package



Dimensions in mm

Fig. 7

Dimensions of SO8 Package



Dimensions in mm

Fig. 8

Ordering Information

The A 6300 is available with Push-pull or Open drain output stage and Reset active low or high.

Ordering form: A 6300 <version letter> <packaging>

Example: Regulator with: - Reset active low
- Open drain output
- 4.0 V threshold

In DIP8 package: **A 6300 AQ 8P**
In SO8 package: **A 6300 AQ 8S**

When ordering, please specify the complete part number.

Version letter definition

Output stage	Threshold voltage [V]				
	2.0	2.4	2.8	3.5	4.0
Push-pull, reset active low	AA*	AB*	AC*	AD*	AE*
Push-pull, reset active high	AG*	AH*	AI*	AJ*	AK*
Open drain, reset active low	AM*	AN*	AO*	AP	AQ

* on request

Table 7

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Table of Contents

DUAL Two Channel Level Shifter

Features

- DUAL two bit wide TTL compatible with 2 separated $\overline{OE}$ pin for bus capability
- 4 separated Input / Output Power Supplies
- Fully operational from 1.5 V to 10 V
- Standby current: typ. 100 nA at $V_{DD} = V_{CC} = 10$ V
- TTL / CMOS compatibility
- Push-pull or Open drain outputs
- −40°C to +85°C temperature range
- DIP16 and SO16 packages

Description

The V 6910 is a CMOS device which shifts digital signal levels from V_{DDx} to V_{CCx}. The voltage of V_{DDx} can be higher or lower than V_{CCx}. The outputs can be set into a high impedance state by pulling the $\overline{OE}$ to "1". These functions allow a bidirectional communication between two systems which have different power supplies.

Applications

Any system needing a voltage interface, such as:

- Interface between peripherals or between peripherals and microprocessor
- To drive a D/A or an A/D converter from a 5 V control system
- Data communication
- Bus repeater

Typical Operating Configuration

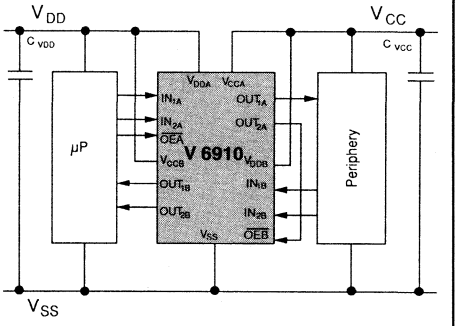


Fig. 1

Pin Assignment

DIP16 / SO16

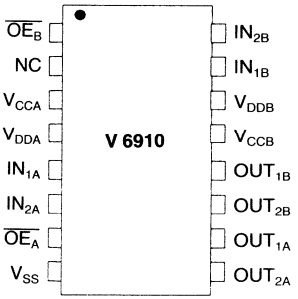


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Max. voltage at V_{DDx}	V_{DDmax}	V_{SS} + 10 V
Max. voltage at V_{CCx}	V_{CCmax}	V_{SS} + 10 V
Min. voltage at V_{DDx}	V_{DDmin}	V_{SS} − 0.3 V
Min. voltage at V_{CCx}	V_{CCmin}	V_{SS} − 0.3 V
Max. voltage at any input pin	V_{INmax}	V_{DD} + 0.3 V
Min. voltage at any input pin	V_{INmin}	V_{SS} − 0.3 V
Max. voltage at any output pin	V_{OUTmax}	V_{CC} + 0.3 V
Min. voltage at any output pin	V_{OUTmin}	V_{SS} − 0.3 V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40	+25	+85	°C
Supply voltage V_{DDx} [1]	V_{DD}	1.5		10	V
Supply voltage V_{CCx} [1]	V_{CC}	1.5		10	V
Frequency $V_{DDx} = V_{CCx} = 10$ V	f	DC		8	MHz

Table 2

[1] A 100 nF decoupling capacitor is required on both V_{DDx} and V_{CCx} for stability (see Fig. 1).

Electrical Characteristics

T_A = −40 to +85°C, C_{VDDx} = 100 nF, C_{VCCx} = 100 nF, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby current	I_{SB}	$V_{DDx} = 10$ V, $V_{CCx} = 10$ V, $I_{OUT} = 0$ mA		0.1	20	µA
V_{DD} current, operating	I_{DD}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ to 10 V, f = 500 kHz, $I_{OUT} = 0$ mA		4	70	µA
	I_{DD}	$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ to 10 V, f = 500 kHz, $I_{OUT} = 0$ mA		40	100	µA
V_{CC} current, operating	I_{CC}	$V_{CCx} = 1.5$ V, $V_{DDx} = 1.5$ to 10 V, f = 500 kHz, $I_{OUT} = 0$ mA		40	100	µA
	I_{CC}	$V_{CCx} = 10$ V, $V_{DDx} = 1.5$ to 10 V, f = 500 kHz, $I_{OUT} = 0$ mA		1.2	8.0	mA
Input Low Voltage	V_{IL}	$V_{DDx} = 10$ V			1.5	V
	V_{IL}	$V_{DDx} = 4.5$ V			0.8	V
	V_{IL}	$V_{DDx} = 1.5$ V			0.3	V
Input High Voltage	V_{IH}	$V_{DDx} = 10$ V	3.0			V
	V_{IH}	$V_{DDx} = 5.5$ V	2.0			V
	V_{IH}	$V_{DDx} = 1.5$ V	1.2			V
Output Low Voltage	V_{OL}	$V_{CCx} = 10$ V, $I_{OL} = 8$ mA		0.2	0.4	V
	V_{OL}	$V_{CCx} = 4.5$ V, $I_{OL} = 4$ mA		0.2	0.4	V
	V_{OL}	$V_{CCx} = 1.5$ V, $I_{OL} = 250$ µA		0.05	0.2	V
Output High Voltage (Push-pull version only)	V_{OH}	$V_{CCx} = 10$ V, $I_{OH} = -8$ mA	9.5	9.75		V
	V_{OH}	$V_{CCx} = 4.5$ V, $I_{OH} = -4$ mA	4.0	4.3		V
	V_{OH}	$V_{CCx} = 1.5$V, $I_{OH} = -250$ µA	1.3	1.46		V
Input leakage current	I_{LI}	$0 V \le V_{IN} \le V_{DDx}$			1	µA
Output leakage current	I_{LO}	$0 V \le V_{OUT} \le V_{CCx}$, $\overline{OE_x} = V_{DDx}$			1	µA

Table 3

Propagation Time

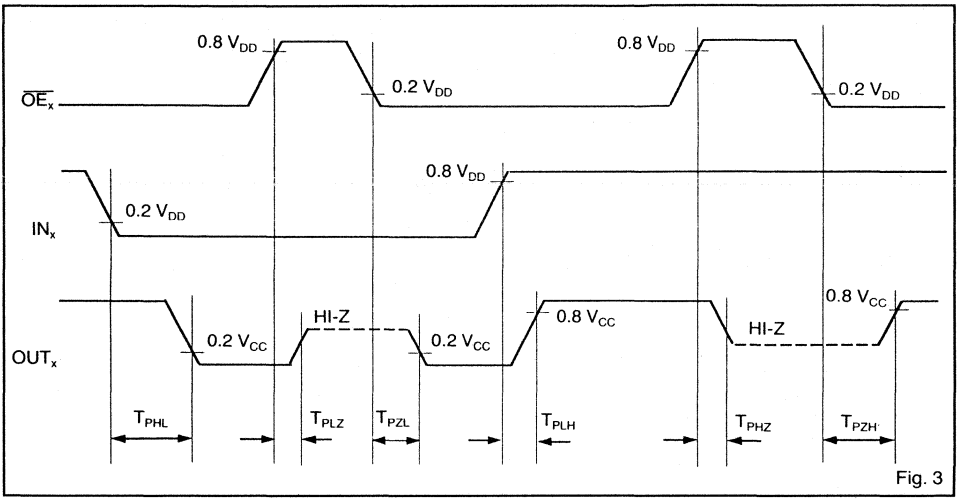


Fig. 3

Timing Characteristics

T_A = −40 to +85°C, C_{VDDx} = 100 nF, C_{VCCx} = 100 nF, R_L = 10 kΩ and C_L = 50 pF, unless otherwise specfied

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delay: High to Low	T_{PHL}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 V		350	600	ns
		V_{DDx} = 1.5 V, V_{CCx} = 10 V		70	150	ns
		V_{DDx} = 10 V, V_{CCx} = 1.5 V		350	600	ns
		V_{DDx} = 10 V, V_{CCx} = 10 V		30	70	ns
Propagation delay: Low to High	T_{PLH}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 V		250	500	ns
		V_{DDx} = 1.5 V, V_{CCx} = 10 V		50	100	ns
		V_{DDx} = 10 V, V_{CCx} = 1.5 V		250	500	ns
		V_{DDx} = 10 V, V_{CCx} = 10 V		20	50	ns
Output disable time from High Level[1]	T_{PHZ}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 V		100	200	ns
		V_{DDx} = 1.5 V, V_{CCx} = 10 V		70	150	ns
		V_{DDx} = 10 V, V_{CCx} = 1.5 V		80	150	ns
		V_{DDx} = 10 V, V_{CCx} = 10 V		35	70	ns
Output enable time to High Level	T_{PZH}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 V		250	500	ns
		V_{DDx} = 1.5 V, V_{CCx} = 10 V		70	150	ns
		V_{DDx} = 10 V, V_{CCx} = 1.5 V		250	500	ns
		V_{DDx} = 10 V, V_{CCx} = 10 V		30	70	ns
Output disable time from Low Level[2]	T_{PLZ}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 V		60	120	ns
		V_{DDx} = 1.5 V, V_{CCx} = 10 V		60	120	ns
		V_{DDx} = 10 V, V_{CCx} = 1.5 V		50	100	ns
		V_{DDx} = 10 V, V_{CCx} = 10 V		20	50	ns
Output enable time to Low Level	T_{PZL}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 V		250	500	ns
		V_{DDx} = 1.5 V, V_{CCx} = 10 V		70	150	ns
		V_{DDx} = 10 V, V_{CCx} = 1.5 V		250	500	ns
		V_{DDx} = 10 V, V_{CCx} = 10 V		20	70	ns

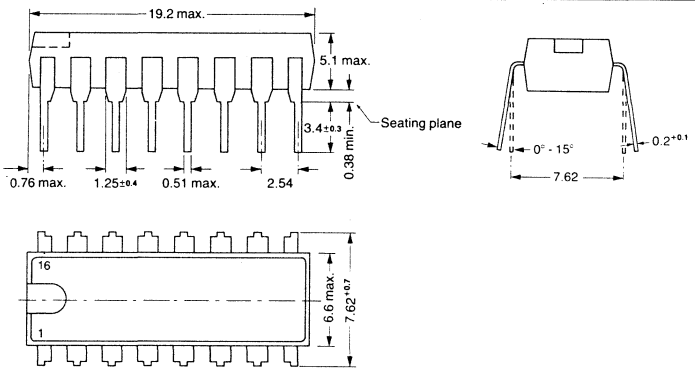
Table 4

[1] Test circuit: 1 kΩ connected to V_{SS}, test point at 80% of the output transition
[2] Test circuit: 1 kΩ connected to V_{CC}, test point at 20% of the output transition

9

Package and Ordering Information

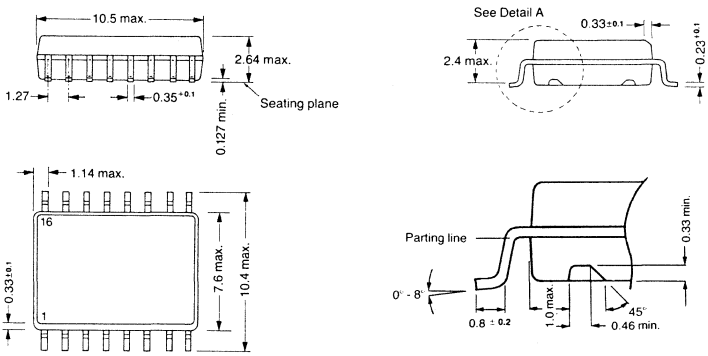
Dimensions of DIP16 Package



Dimensions in mm

Fig. 4

Dimensions of SO16 Package



Dimensions in mm

Fig. 5

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
V 6910 nn 16P	DIP16
V 6910 nn 16S	SO16

When ordering please specify complete part number.

Marking on package:

Package	Marking[1]
DIP16	V 6910 nn
SO16	6910 nn

[1] nn stands for the versions 10*, 20*

* On request

The V 6910 standard versions are:

Version	Outputs
10	Open drain
20	Push-pull

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Two Channel Level Shifter

Features

- Two bit wide TTL compatible with common $\overline{OE}$ pin for bus capability
- 2 separated Input / Output Power Supplies
- Fully operational from 1.5 V to 10 V
- Standby current: typ. 50 nA at $V_{DD} = V_{CC} = 10$ V
- TTL / CMOS compatibility
- Push-pull or Open drain outputs
- −40°C to +85°C temperature range
- DIP8 and SO8 packages

Description

The V 6912 is a CMOS device which shifts digital signal levels from V_{DD} to V_{CC}. The voltage of V_{DD} can be higher or lower than V_{CC}. The outputs can be set into a high impedance state by pulling the $\overline{OE}$ to "1". These functions allow a bidirectional communication between two systems which have different power supplies.

Applications

Any system needing a voltage interface, such as:

- Interface between peripherals or between peripherals and microprocessor
- To drive a D/A or an A/D converter from a 5 V control system
- Data communication
- Bus repeater

Typical Operating Configuration

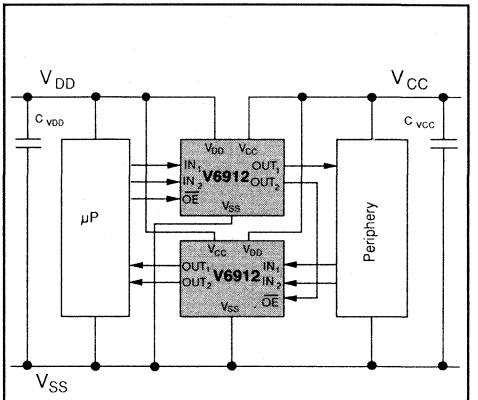


Fig. 1

Pin Assignment

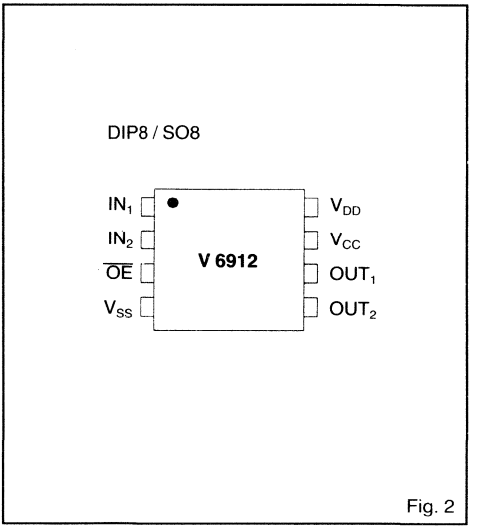


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Max. voltage at V_{DD}	V_{DDmax}	V_{SS} + 10 V
Max. voltage at V_{CC}	V_{CCmax}	V_{SS} + 10 V
Min. voltage at V_{DD}	V_{DDmin}	V_{SS} − 0.3 V
Min. voltage at V_{CC}	V_{CCmin}	V_{SS} − 0.3 V
Max. voltage at any input pin	V_{INmax}	V_{DD} + 0.3 V
Min. voltage at any input pin	V_{INmin}	V_{SS} − 0.3 V
Max. voltage at any output pin	V_{OUTmax}	V_{CC} + 0.3 V
Min. voltage at any output pin	V_{OUTmin}	V_{SS} − 0.3 V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40	+25	+85	°C
Supply voltage V_{DD} [1]	V_{DD}	1.5		10	V
Supply voltage V_{CC} [1]	V_{CC}	1.5		10	V
Frequency $V_{DD} = V_{CC} = 10$ V	f	DC		8	MHz

Table 2

[1] A 100 nF decoupling capacitor is required on both V_{DD} and V_{CC} for stability (see Fig. 1).

Electrical Characteristics

T_A = −40 to +85°C, C_{VDD} = 100 nF, C_{VCC} = 100 nF, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby current	I_{SB}	V_{DD} = 10 V, V_{CC} = 10 V, I_{OUT} = 0 mA		0.05	10	µA
V_{DD} current, operating	I_{DD}	V_{DD} = 1.5 V, V_{CC} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		2	35	µA
	I_{DD}	V_{DD} = 10 V, V_{CC} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		20	50	µA
V_{CC} current, operating	I_{CC}	V_{CC} = 1.5 V, V_{DD} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		20	50	µA
	I_{CC}	V_{CC} = 10 V, V_{DD} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		0.6	4.0	mA
Input Low Voltage	V_{IL}	V_{DD} = 10 V			1.5	V
	V_{IL}	V_{DD} = 4.5 V			0.8	V
	V_{IL}	V_{DD} = 1.5 V			0.3	V
Input High Voltage	V_{IH}	V_{DD} = 10 V	3.0			V
	V_{IH}	V_{DD} = 5.5 V	2.0			V
	V_{IH}	V_{DD} = 1.5 V	1.2			V
Output Low Voltage	V_{OL}	V_{CC} = 10 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{CC} = 1.5 V, I_{OL} = 250 µA		0.05	0.2	V
Output High Voltage (Push-pull version only)	V_{OH}	V_{CC} = 10 V, I_{OH} = −8 mA	9.5	9.75		V
	V_{OH}	V_{CC} = 4.5 V, I_{OH} = −4 mA	4.0	4.3		V
	V_{OH}	V_{CC} = 1.5V, I_{OH} = −250 µA	1.3	1.46		V
Input leakage current	I_{LI}	$0 V \le V_{IN} \le V_{DD}$			1	µA
Output leakage current	I_{LO}	$0 V \le V_{OUT} \le V_{CC}$, $\overline{OE} = V_{DD}$			1	µA

Table 3

Propagation Time

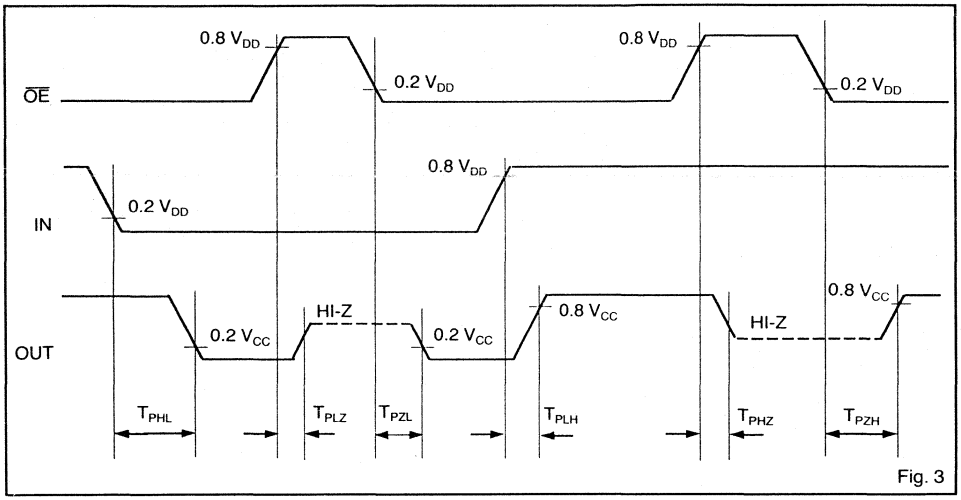


Fig. 3

Timing Characteristics

T_A = −40 to +85°C, C_{VDD} = 100 nF, C_{VCC} = 100 nF, R_L = 10 kΩ and C_L = 50 pF, unless otherwise specfied

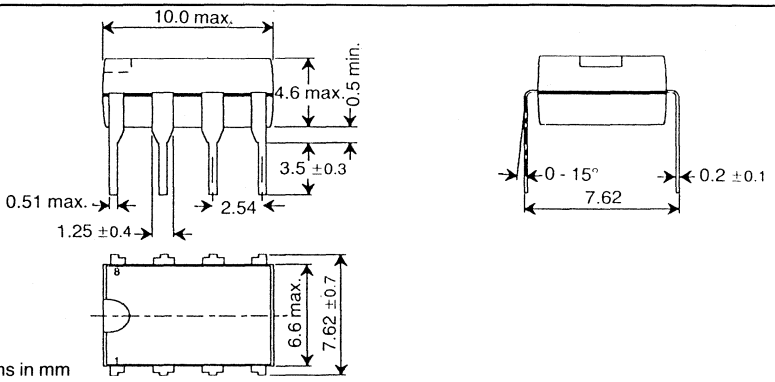
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delay: High to Low	T_{PHL}	V_{DD} = 1.5 V, V_{CC} = 1.5 V		350	600	ns
		V_{DD} = 1.5 V, V_{CC} = 10 V		70	150	ns
		V_{DD} = 10 V, V_{CC} = 1.5 V		350	600	ns
		V_{DD} = 10 V, V_{CC} = 10 V		30	70	ns
Propagation delay: Low to High	T_{PLH}	V_{DD} = 1.5 V, V_{CC} = 1.5 V		250	500	ns
		V_{DD} = 1.5 V, V_{CC} = 10 V		50	100	ns
		V_{DD} = 10 V, V_{CC} = 1.5 V		250	500	ns
		V_{DD} = 10 V, V_{CC} = 10 V		20	50	ns
Output disable time from High Level[1]	T_{PHZ}	V_{DD} = 1.5 V, V_{CC} = 1.5 V		100	200	ns
		V_{DD} = 1.5 V, V_{CC} = 10 V		70	150	ns
		V_{DD} = 10 V, V_{CC} = 1.5 V		80	150	ns
		V_{DD} = 10 V, V_{CC} = 10 V		35	70	ns
Output enable time to High Level	T_{PZH}	V_{DD} = 1.5 V, V_{CC} = 1.5 V		250	500	ns
		V_{DD} = 1.5 V, V_{CC} = 10 V		70	150	ns
		V_{DD} = 10 V, V_{CC} = 1.5 V		250	500	ns
		V_{DD} = 10 V, V_{CC} = 10 V		30	70	ns
Output disable time from Low Level[2]	T_{PLZ}	V_{DD} = 1.5 V, V_{CC} = 1.5 V		60	120	ns
		V_{DD} = 1.5 V, V_{CC} = 10 V		60	120	ns
		V_{DD} = 10 V, V_{CC} = 1.5 V		50	100	ns
		V_{DD} = 10 V, V_{CC} = 10 V		20	50	ns
Output enable time to Low Level	T_{PZL}	V_{DD} = 1.5 V, V_{CC} = 1.5 V		250	500	ns
		V_{DD} = 1.5 V, V_{CC} = 10 V		70	150	ns
		V_{DD} = 10 V, V_{CC} = 1.5 V		250	500	ns
		V_{DD} = 10 V, V_{CC} = 10 V		20	70	ns

Table 4

[1] Test circuit: 1 kΩ connected to V_{SS}, test point at 80% of the output transition
[2] Test circuit: 1 kΩ connected to V_{CC}, test point at 20% of the output transition

Package and Ordering Information

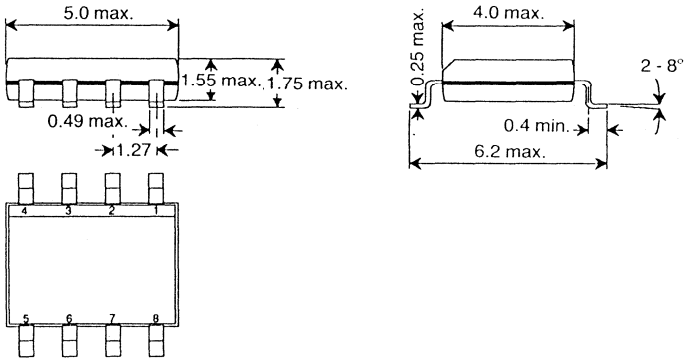
Dimensions of DIP8 Package



Dimensions in mm

Fig. 4

Dimensions of SO8 Package



Dimensions in mm

Fig. 5

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
V 6912 nn 8P	DIP8
V 6912 nn 8S	SO8

When ordering please specify complete part number.

Marking on package:

Package	Marking[1]
DIP8	V 6912 nn
SO8	6912 nn

[1] nn stands for the versions 10*, 20*

* On request

The V 6912 standard versions are:

Version	Outputs
10	Open drain
20	Push-pull

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DUAL Two Channel Level Shifter

Features

- DUAL two bit wide with 2 separated $\overline{OE}$ pin for bus capability
- Schmitt Trigger on the inputs
- High noise immunity
- 4 separated Input / Output Power Supplies
- Fully operational from 1.5 V to 10 V
- Standby current: typ. 100 nA at $V_{DD} = V_{CC} = 10$ V
- CMOS output compatibility
- Push-pull or Open drain outputs
- −40°C to +85°C temperature range
- DIP16 and SO16 packages

Description

The V 6915 is a CMOS device which shifts digital signal levels from V_{DDx} to V_{CCx}. The voltage of V_{DDx} can be higher or lower than V_{CCx}. The outputs can be set into a high impedance state by pulling the $\overline{OE}$ to "1". These functions allow a bidirectional communication between two systems which have different power supplies.

Applications

Any system needing a voltage interface, such as:

- Interface between peripherals or between peripherals and microprocessor
- To drive a D/A or an A/D converter from a 5 V control system
- Data communication (high noise immunity)
- Bus repeater

Typical Operating Configuration

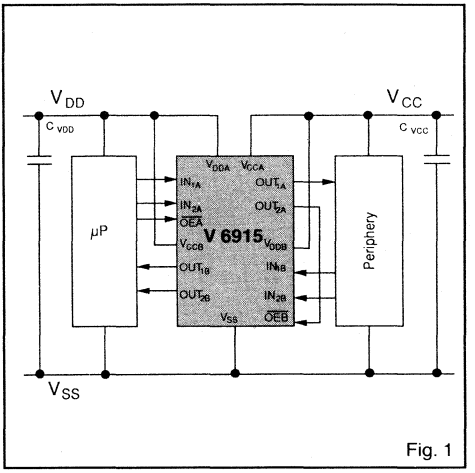


Fig. 1

Pin Assignment

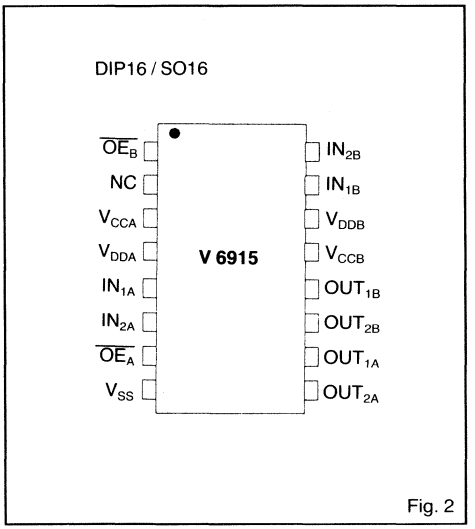


Fig. 2

9

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Max. voltage at V_{DDx}	V_{DDmax}	V_{SS} + 10 V
Max. voltage at V_{CCx}	V_{CCmax}	V_{SS} + 10 V
Min. voltage at V_{DDx}	V_{DDmin}	V_{SS} − 0.3 V
Min. voltage at V_{CCx}	V_{CCmin}	V_{SS} − 0.3 V
Max. voltage at any input pin	V_{INmax}	V_{DD} + 0.3 V
Min. voltage at any input pin	V_{INmin}	V_{SS} − 0.3 V
Max. voltage at any output pin	V_{OUTmax}	V_{CC} + 0.3 V
Min. voltage at any output pin	V_{OUTmin}	V_{SS} − 0.3 V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40	+25	+85	°C
Supply voltage V_{DDx} [1]	V_{DD}	1.5		10	V
Supply voltage V_{CCx} [1]	V_{CC}	1.5		10	V
Frequency $V_{DDx} = V_{CCx} = 10$ V	f	DC		5	MHz

Table 2

[1] A 100 nF decoupling capacitor is required on both V_{DDx} and V_{CCx} for stability (see Fig. 1).

Electrical Characteristics

T_A = −40 to +85°C, C_{VDDx} = 100 nF, C_{VCCx} = 100 nF, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby current	I_{SB}	V_{DDx} = 10 V, V_{CCx} = 10 V, I_{OUT} = 0 mA		0.1	20	µA
V_{DD} current, operating	I_{DD}	V_{DDx} = 1.5 V, V_{CCx} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		4	70	µA
	I_{DD}	V_{DDx} = 10 V, V_{CCx} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		60	100	µA
V_{CC} current, operating	I_{CC}	V_{CCx} = 1.5 V, V_{DDx} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		40	100	µA
	I_{CC}	V_{CCx} = 10 V, V_{DDx} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		1.2	4	mA
Input Low Voltage	V_{IL}	V_{DDx} = 10 V	2.0		3.0	
	V_{IL}	V_{DDx} = 5 V	1.0		1.8	V
	V_{IL}	V_{DDx} = 1.5 V	0.06		0.6	V
Input High Voltage	V_{IH}	V_{DDx} = 10 V	5.0		7.0	V
	V_{IH}	V_{DDx} = 5 V	2.5		3.8	V
	V_{IH}	V_{DDx} = 1.5 V	0.9		1.44	V
Output Low Voltage	V_{OL}	V_{CCx} = 10 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{CCx} = 4.5 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{CCx} = 1.5 V, I_{OL} = 250 µA		0.05	0.2	V
Output High Voltage (Push-pull version only)	V_{OH}	V_{CCx} = 10 V, I_{OH} = −8 mA	9.5	9.75		V
	V_{OH}	V_{CCx} = 4.5 V, I_{OH} = −4 mA	4.0	4.3		V
	V_{OH}	V_{CCx} = 1.5V, I_{OH} = −250 µA	1.3	1.46		V
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DDx}			1	µA
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CCx}, $\overline{OE_x}$ = V_{DDx}			1	µA

Table 3

Propagation Time

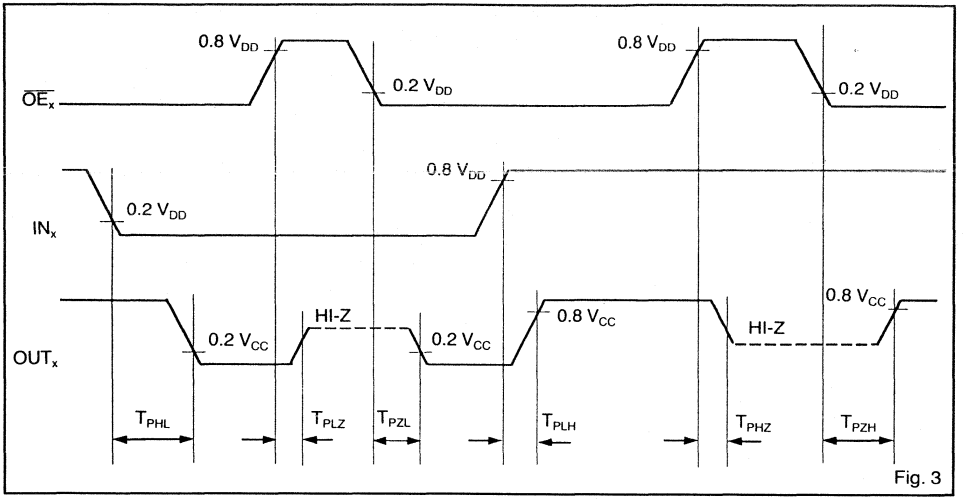


Fig. 3

Timing Characteristics

$T_A = -40$ to $+85°C$, $C_{VDDx} = 100$ nF, $C_{VCCx} = 100$ nF, $R_L = 10$ kΩ and $C_L = 50$ pF, unless otherwise specfied

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delay: High to Low	T_{PHL}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ V		600	900	ns
		$V_{DDx} = 1.5$ V, $V_{CCx} = 10$ V		300	600	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ V		350	700	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 10$ V		50	100	ns
Propagation delay: Low to High	T_{PLH}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ V		380	700	ns
		$V_{DDx} = 1.5$ V, $V_{CCx} = 10$ V		160	320	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ V		270	540	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 10$ V		30	70	ns
Output disable time from High Level[1]	T_{PHZ}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ V		250	500	ns
		$V_{DDx} = 1.5$ V, $V_{CCx} = 10$ V		220	440	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ V		90	180	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 10$ V		45	90	ns
Output enable time to High Level	T_{PZH}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ V		480	800	ns
		$V_{DDx} = 1.5$ V, $V_{CCx} = 10$ V		300	600	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ V		270	540	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 10$ V		40	80	ns
Output disable time from Low Level[2]	T_{PLZ}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ V		180	360	ns
		$V_{DDx} = 1.5$ V, $V_{CCx} = 10$ V		200	400	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ V		60	120	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 10$ V		30	70	ns
Output enable time to Low Level	T_{PZL}	$V_{DDx} = 1.5$ V, $V_{CCx} = 1.5$ V		450	800	ns
		$V_{DDx} = 1.5$ V, $V_{CCx} = 10$ V		300	600	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 1.5$ V		230	460	ns
		$V_{DDx} = 10$ V, $V_{CCx} = 10$ V		40	80	ns

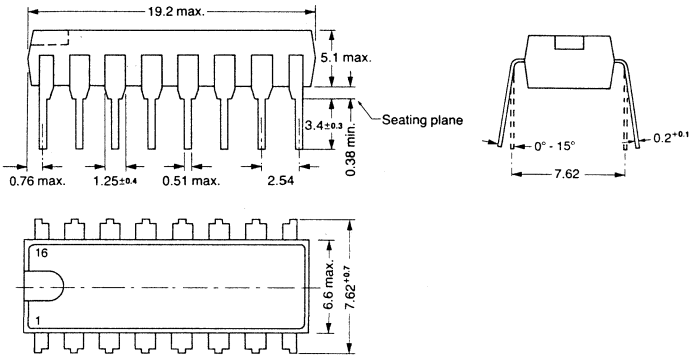
Table 4

[1] Test circuit: 1 kΩ connected to V_{SS}, test point at 80% of the output transition
[2] Test circuit: 1 kΩ connected to V_{CC}, test point at 20% of the output transition

9

Package and Ordering Information

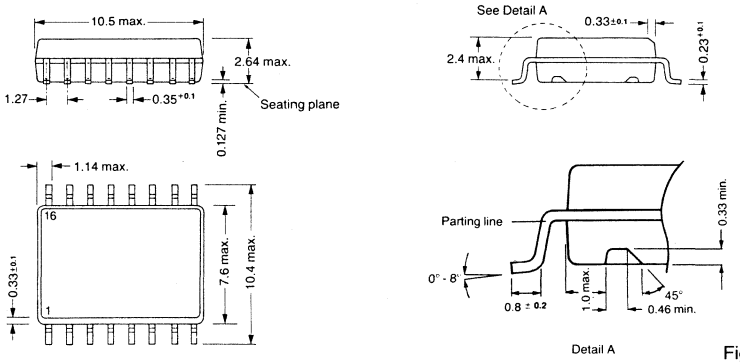
Dimensions of DIP16 Package



Dimensions in mm

Fig. 4

Dimensions of SO16 Package



Dimensions in mm

Fig. 5

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
V 6915 nn 16P	DIP16
V 6915 nn 16S	SO16

When ordering please specify complete part number.

Marking on package:

Package	Marking[1]
DIP16	V 6915 nn
SO16	6915 nn

[1] nn stands for the versions 10*, 20*

* On request

The V 6915 standard versions are:

Version	Outputs
10	Open drain
20	Push-pull

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Two Channel Level Shifter

Features

- Two bit wide with common $\overline{OE}$ pin for bus capability
- Schmitt Trigger on the inputs
- High noise immunity
- 2 separated Input / Output Power Supplies
- Fully operational from 1.5 V to 10 V
- Standby current: typ. 50 nA at $V_{DD} = V_{CC} = 10$ V
- CMOS output compatibility
- Push-pull or Open drain outputs
- −40°C to +85°C temperature range
- DIP8 and SO8 packages

Description

The V 6917 is a CMOS device which shifts digital signal levels from V_{DD} to V_{CC}. The voltage of V_{DD} can be higher or lower than V_{CC}. The outputs can be set into a high impedance state by pulling the $\overline{OE}$ to "1". These functions allow a bidirectional communication between two systems which have different power supplies.

Applications

Any system needing a voltage interface, such as:

- Interface between peripherals or between peripherals and microprocessor
- To drive a D/A or an A/D converter from a 5 V control system
- Data communication (high noise immunity)
- Bus repeater

Typical Operating Configuration

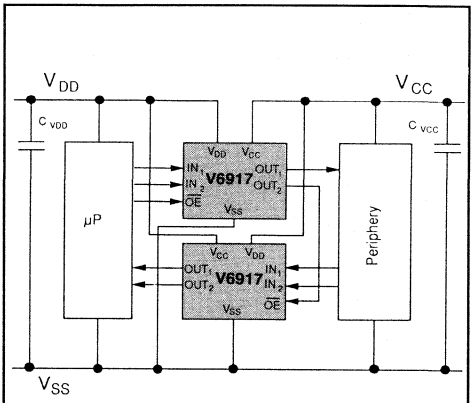


Fig. 1

Pin Assignment

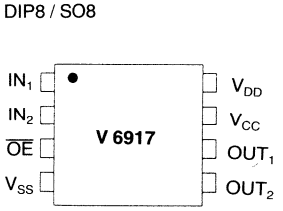


Fig. 2

9

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Max. voltage at V_{DD}	V_{DDmax}	V_{SS} + 10 V
Max. voltage at V_{CC}	V_{CCmax}	V_{SS} + 10 V
Min. voltage at V_{DD}	V_{DDmin}	V_{SS} − 0.3 V
Min. voltage at V_{CC}	V_{CCmin}	V_{SS} − 0.3 V
Max. voltage at any input pin	V_{INmax}	V_{DD} + 0.3 V
Min. voltage at any input pin	V_{INmin}	V_{SS} − 0.3 V
Max. voltage at any output pin	V_{OUTmax}	V_{CC} + 0.3 V
Min. voltage at any output pin	V_{OUTmin}	V_{SS} − 0.3 V
Storage temperature	T_{STO}	−65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40	+25	+85	°C
Supply voltage V_{DD} [1]	V_{DD}	1.5		10	V
Supply voltage V_{CC} [1]	V_{CC}	1.5		10	V
Frequency $V_{DD} = V_{CC} = 10$ V	f	DC		5	MHz

Table 2

[1] A 100 nF decoupling capacitor is required on both V_{DD} and V_{CC} for stability (see Fig. 1).

Electrical Characteristics

T_A = −40 to +85°C, C_{VDD} = 100 nF, C_{VCC} = 100 nF, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby current	I_{SB}	V_{DD} = 10 V, V_{CC} = 10 V, I_{OUT} = 0 mA		0.05	10	μA
V_{DD} current, operating	I_{DD}	V_{DD} = 1.5 V, V_{CC} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		2	35	μA
	I_{DD}	V_{DD} = 10 V, V_{CC} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		30	50	μA
V_{CC} current, operating	I_{CC}	V_{CC} = 1.5 V, V_{DD} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		20	50	μA
	I_{CC}	V_{CC} = 10 V, V_{DD} = 1.5 to 10 V, f = 500 kHz, I_{OUT} = 0 mA		0.6	2	mA
Input Low Voltage	V_{IL}	V_{DD} = 10 V	2.0		3.0	V
	V_{IL}	V_{DD} = 5 V	1.0		1.8	V
	V_{IL}	V_{DD} = 1.5 V	0.06		0.6	V
Input High Voltage	V_{IH}	V_{DD} = 10 V	5.0		7.0	V
	V_{IH}	V_{DD} = 5 V	2.5		3.8	V
	V_{IH}	V_{DD} = 1.5 V	0.9		1.44	V
Output Low Voltage	V_{OL}	V_{CC} = 10 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{CC} = 1.5 V, I_{OL} = 250 μA		0.05	0.2	V
Output High Voltage (Push-pull version only)	V_{OH}	V_{CC} = 10 V, I_{OH} = −8 mA	9.5	9.75		V
	V_{OH}	V_{CC} = 4.5 V, I_{OH} = −4 mA	4.0	4.3		V
	V_{OH}	V_{CC} = 1.5V, I_{OH} = −250 μA	1.3	1.46		V
Input leakage current	I_{LI}	$0 V \le V_{IN} \le V_{DD}$			1	μA
Output leakage current	I_{LO}	$0 V \le V_{OUT} \le V_{CC}$, $\overline{OE} = V_{DD}$			1	μA

Table 3

Propagation Time

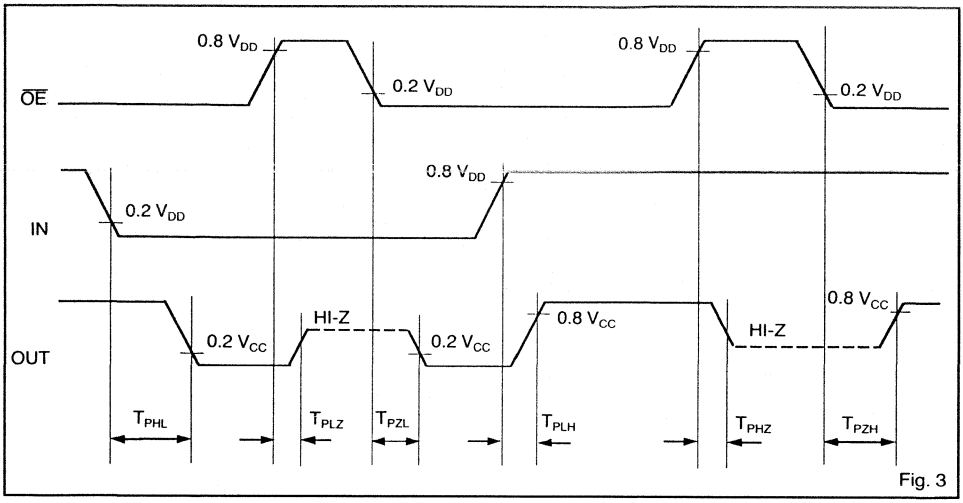


Fig. 3

Timing Characteristics

$T_A = -40$ to $+85°C$, $C_{VDD} = 100$ nF, $C_{VCC} = 100$ nF, $R_L = 10$ kΩ and $C_L = 50$ pF, unless otherwise specfied

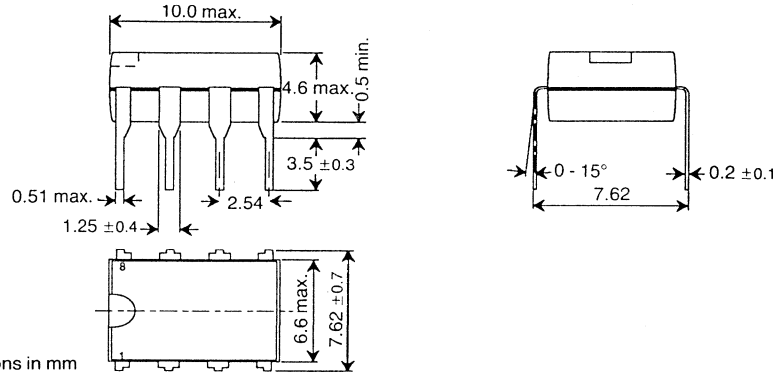
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delay: High to Low	T_{PHL}	$V_{DD} = 1.5$ V, $V_{CC} = 1.5$ V		600	900	ns
		$V_{DD} = 1.5$ V, $V_{CC} = 10$ V		300	600	ns
		$V_{DD} = 10$ V, $V_{CC} = 1.5$ V		350	700	ns
		$V_{DD} = 10$ V, $V_{CC} = 10$ V		50	100	ns
Propagation delay: Low to High	T_{PLH}	$V_{DD} = 1.5$ V, $V_{CC} = 1.5$ V		380	700	ns
		$V_{DD} = 1.5$ V, $V_{CC} = 10$ V		160	320	ns
		$V_{DD} = 10$ V, $V_{CC} = 1.5$ V		270	540	ns
		$V_{DD} = 10$ V, $V_{CC} = 10$ V		30	70	ns
Output disable time from High Level[1]	T_{PHZ}	$V_{DD} = 1.5$ V, $V_{CC} = 1.5$ V		250	500	ns
		$V_{DD} = 1.5$ V, $V_{CC} = 10$ V		220	440	ns
		$V_{DD} = 10$ V, $V_{CC} = 1.5$ V		90	180	ns
		$V_{DD} = 10$ V, $V_{CC} = 10$ V		45	90	ns
Output enable time to High Level	T_{PZH}	$V_{DD} = 1.5$ V, $V_{CC} = 1.5$ V		480	800	ns
		$V_{DD} = 1.5$ V, $V_{CC} = 10$ V		300	600	ns
		$V_{DD} = 10$ V, $V_{CC} = 1.5$ V		270	540	ns
		$V_{DD} = 10$ V, $V_{CC} = 10$ V		40	80	ns
Output disable time from Low Level[2]	T_{PLZ}	$V_{DD} = 1.5$ V, $V_{CC} = 1.5$ V		180	360	ns
		$V_{DD} = 1.5$ V, $V_{CC} = 10$ V		200	400	ns
		$V_{DD} = 10$ V, $V_{CC} = 1.5$ V		60	120	ns
		$V_{DD} = 10$ V, $V_{CC} = 10$ V		30	70	ns
Output enable time to Low Level	T_{PZL}	$V_{DD} = 1.5$ V, $V_{CC} = 1.5$ V		450	800	ns
		$V_{DD} = 1.5$ V, $V_{CC} = 10$ V		300	600	ns
		$V_{DD} = 10$ V, $V_{CC} = 1.5$ V		230	460	ns
		$V_{DD} = 10$ V, $V_{CC} = 10$ V		40	80	ns

Table 4

[1] Test circuit: 1 kΩ connected to V_{SS}, test point at 80% of the output transition
[2] Test circuit: 1 kΩ connected to V_{CC}, test point at 20% of the output transition

Package and Ordering Information

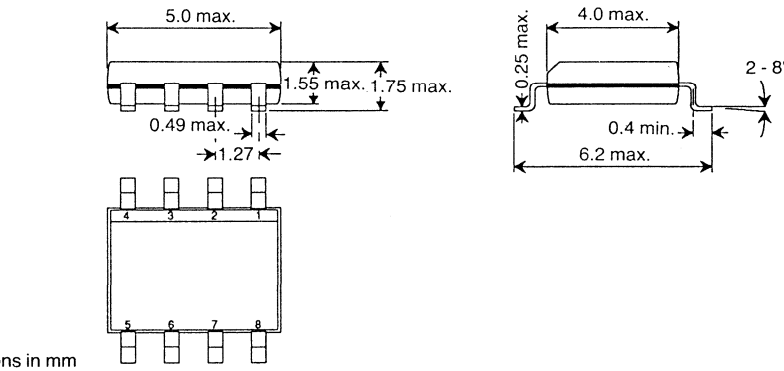
Dimensions of DIP8 Package



Dimensions in mm

Fig. 4

Dimensions of SO8 Package



Dimensions in mm

Fig. 5

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
V 6917 nn 8P	DIP8
V 6917 nn 8S	SO8

When ordering please specify complete part number.

Marking on package:

Package	Marking[1]
DIP8	V 6917 nn
SO8	6917 nn

[1] nn stands for the versions 10*, 20*

* On request

The V 6917 standard versions are:

Version	Outputs
10	Open drain
20	Push-pull

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Contactless Identification Devices (CID)

Table of Contents

Read-Only Contactless Identification Device

Features

- 64 bit memory array laser programmable
- Wide dynamic range due to on-chip buffer capacitance and voltage limiter on chip
- Full wave rectifier on chip
- Big modulation depth due to a low impedance modulation device
- 50'000 baud reading speed at 3 MHz
- Very small chip size convenient for implantation
- Unsensitive close to metal
- Large distance even without resonance capacitor
- No external buffer capacitance needed due to low power consumption

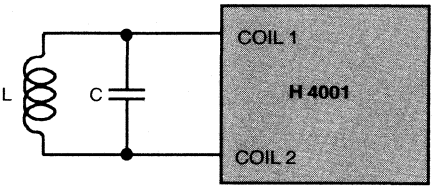
Description

The H 4001 is a CMOS integrated circuit for use in transponders. The circuit is powered by an external coil placed in a magnetic field, and gets its clock from the same field via one of the coil terminals. The other coil terminal is affected by the modulator, turning on and off the modulation current in order to send back the 64 bits of information contained in a factory pre-programmed memory array. The programming of the chip is performed by laser fusing of polysilicon links in order to store a unique code on each chip. The serial output data string contains a 9 bits header, 40 bits of data, 14 parity bits, and 1 stop bit. Due to the low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is required to obtain the chip function. A parallel capacitor adjusted with the coil to obtain resonance will increase the read distance.

Applications

- Industrial transponder
- Animal transponder
- ID cards
- Serial number identification ROM

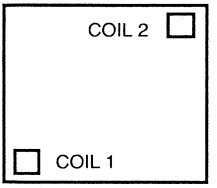
Typical Operating Configuration



Typical value of inductance at 125 kHz is 2 mH.
The capacitor is adjusted to the resonance.

Fig. 1

Pin Assignment



COIL 1 coil terminal / clock input
COIL 2 coil terminal / data transmission

Fig. 2

10

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak current induced on COIL1 and COIL2	I_{COIL}	30 mA
Max. storage temperature	$T_{STOREmax}$	+200° C
Min. storage temperature	$T_{STOREmin}$	− 55° C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	750 V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
AC supply voltage	V_{COIL}	3.5			V_{PP}
Supply frequency	f_{COIL}	50	130	400	kHz

Table 2

Electrical Characteristics

V_{COIL} = 3.5 V_{PP} ± 5%, f_{COIL} = 130 kHz sine wave, T_A = +25°C, unless otherwise specified

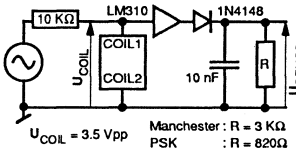
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Demodulated voltage	U_{DEMOD}		0.25			VAC
Dynamic current	I_{DYN}			50		µA

Table 3

Timing Characteristics

V_{COIL2} = 0 V, V_{COIL1} = 3.5 V_{PP} sine wave

Parameter	Symbol	Min.	Typ.	Max.	Units
Coil clock frequency	f_{COIL}	50	130	400	kHz
Ratio between coil period and bit period					
− Manchester code	R_{MCH}		64		
− PSK	R_{PSK}		16		

Table 4

Timing Waveforms

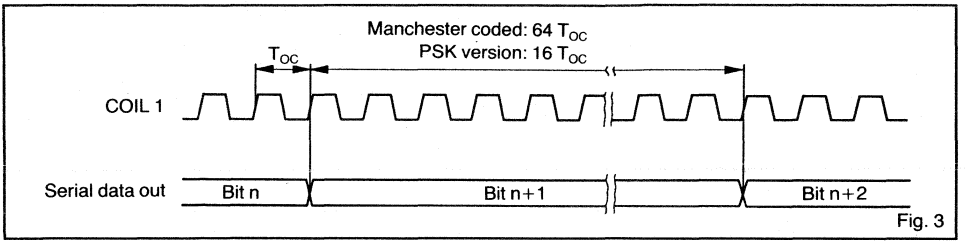


Fig. 3

Manchester Coded Version

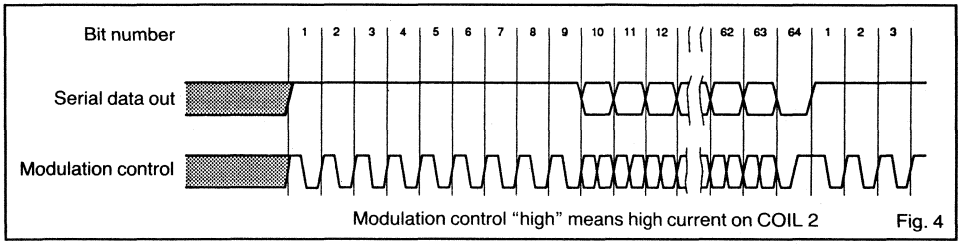


Fig. 4

PSK Version

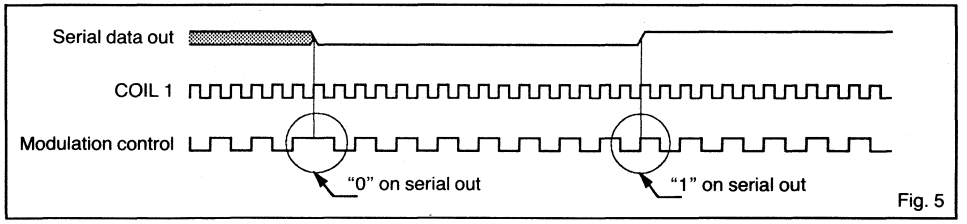


Fig. 5

10

Block Diagram

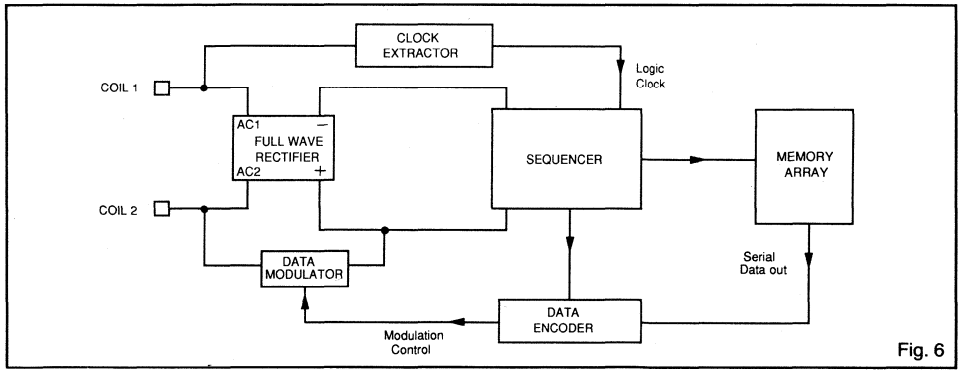


Fig. 6

Functional Description

Full Wave Rectifier

The AC input induced in the external coil by an incident magnetic field is rectified by a Graetz bridge.

Memory Array

The H 4001 contains 64 bits divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0 - P9), 4 column parity bits (PC0 - PC3), 40 data bits (D00 - D93), and 1 stop bit set to logic 0.

1 1 1 1 1 1 1 1 1			- 9 bits header
8 version bits or customer ID	D00 D01 D02 D03	P0	- 4 data bits and associated even row parity bit
	D10 D11 D12 D13	P1	
	D20 D21 D22 D23	P2	
	D30 D31 D32 D33	P3	
32 data bits allowing 4 billion of combinations	D40 D41 D42 D43	P4	
	D50 D51 D52 D53	P5	
	D60 D61 D62 D63	P6	
	D70 D71 D72 D73	P7	
	D80 D81 D82 D83	P8	
	D90 D91 D92 D93	P9	
	PC0 PC1 PC2 PC3	0	- 4 column even parity bits, NO row parity bit

The header is composed by the 9 first bits which are mask programmed to 1 1 1 1 1 1 1 1 1. Due to the data and parity organisation, this sequence cannot be reproduced in the data string. The header is followed by 10 groups of 4 data bits and 1 even row parity bit. Then, the last group consists of 4 even column parity bits without row parity bit.
Bits D00 to D03 and bits D10 to D13 are customer specific identification.

These 64 bits are outputted serially in order to control the modulator used to modify the current at one of the coil terminals. When the 64 bits data string is outputted, the output sequence is repeated continuously until power goes off.

Control Logic

Two mask programmed versions of logic are available. The first one will modulate the amplitude of the magnetic field with a bit rate correspondinng to 64 periods of the field frequency (Manchester coding). The second version is using half of the field frequency to transmit data by shifting the signal phase (PSK coding).
One of the coil terminals (COIL 1 in Fig. 6) is used to generate the clock signal for the logic. The output of the clock extractor drives a sequencer providing all necessary signals to address the memory array, and serially output the data.

PSK Version

The serial data output of the memory array connects the modulation control to the output or inverted output of a flip-flop which input is the signal from the clock extractor. When a logic 0 is output, the modulation control signal is changed to the other output of the flip-flop, and when a logic 1 is output, the modulation control signal remains on the same flip-flop output.

Data Modulator

The data modulator is controlled by the signal modulation control (see Fig. 4 and 5) in order to induce a high current on COIL 2 terminal when this signal is at logic 0. This will affect the magnetic field according to the data stored in the memory array.

Package and Ordering Information

Dimensions of Packages

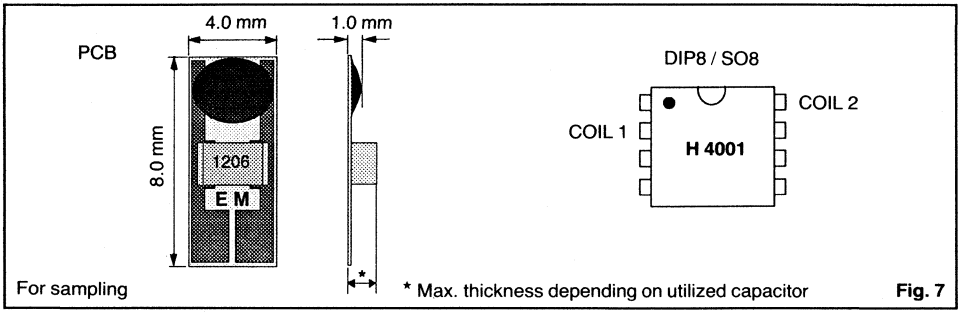


Fig. 7

Ordering Information

The H 4001 is available in chip form.
Others on request.

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Read-Only Contactless Identification Device for ISO Cards

Features

- 64 bit memory array laser programmable
- Wide dynamic range due to on-chip buffer capacitance and voltage limiter on chip
- Full wave rectifier on chip
- Big modulation depth due to a low impedance modulation device
- Reading speed up to 75'000 baud
- Very small chip size convenient for implantation
- Unsensitive close to metal
- Large reading distance
- No external buffer capacitance needed due to low power consumption
- 120 pF for high speed option (HS) or 170 pF for low speed option (LS) with an accuracy of ± 2%. The capacitor is integrated between COIL terminals to obtain a resonant system with the externally adapted coil. Optional metal mask capacitor programmed versions upon request
- 300 μm chip thickness well suited for assembly in ISO format cards

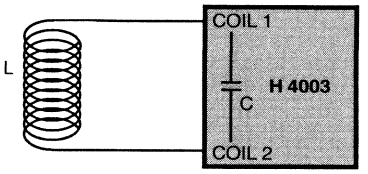
Description

The H 4003 is a CMOS integrated circuit for use in transponders. The circuit is powered by an external coil placed in a magnetic field, and gets its clock from the same field via one of the coil terminals. The other coil terminal is affected by the modulator, turning on and off the modulation current in order to send back the 64 bits of information contained in a factory pre-programmed memory array. The programming of the chip is performed by laser fusing of polysilicon links in order to store a unique code on each chip. The serial output data string contains a 9 bits header, 40 bits of data, 14 parity bits, and 1 stop bit. Due to the low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is required to obtain the chip function. A parallel capacitor is integrated on chipa to obtain increased reading distance.

Applications

- ISO ID cards
- Industrial transponder
- Animal transponder

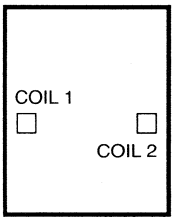
Typical Operating Configuration



Typical value of inductance at 125 kHz is 9.5 mH (170 pF)
Typical value of inductance at 3.25 MHz is 20 μH (120 pF)

Fig. 1

Pin Assignment



COIL 1 coil terminal / clock input
COIL 2 coil terminal / data transmission

Fig. 2

10

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak current induced on COIL1 and COIL2	I_{COIL}	30 mA
Max. storage temperature	$T_{STOREmax}$	+200° C
Min. storage temperature	$T_{STOREmin}$	− 55° C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	750 V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
AC supply voltage LS	$V_{COIL\,LS}$	3.5			V_{PP}
AC supply voltage HS	$V_{COIL\,HS}$	5.0			V_{PP}
Supply frequency LS	$f_{COIL\,LS}$	100		400	kHz
Supply frequency HS	$f_{COIL\,HS}$	2000		5000	kHz

Table 2

Electrical Characteristics

LS: V_{COIL} = 3.5 V_{PP} ± 5%, f_{COIL} = 130 kHz sine wave, T_A = +25°C, unless otherwise specified
HS: V_{COIL} = 5.0 V_{PP} ± 5%, f_{COIL} = 3.5 MHz sine wave, T_A = +25°C, unless otherwise specified

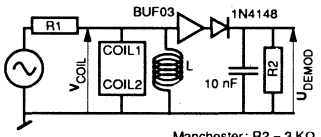
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Demodulated voltage	U_{DEMOD}	 Adapt L for w^2LC_{chip}= 1 Manchester: R2 = 3 KΩ PSK : R2 = 820Ω	0.25			VAC
Minimum AC voltage	V_{COIL}	Same test configuration as above				
HS version			4.5			V_{PP}
LS version			3.5			V_{PP}
Coil1 - Coil2 capacitance LS	C_{LS}		166.6	170	173.4	pF
Coil1 - Coil2 capacitance HS	C_{HS}		117.6	120	122.4	pF
Capacitor series resistance	R_S			5	10	Ω

Table 3

Timing Characteristics

V_{COIL2} = 0 V, LS: V_{COIL1} = 3.5 V_{PP}, HS: V_{COIL1} = 3.5 V_{PP}, sine wave

Parameter	Symbol	Min.	Typ.	Max.	Units
Coil clock frequency LS	$f_{COIL\,LS}$	100		400	kHz
Coil clock frequency HS	$f_{COIL\,HS}$	2000		5000	kHz
Ratio between coil period and bit period					
− Manchester code	R_{MCH}		64		
− PSK	R_{PSK}		16		

Table 4

Timing Waveforms

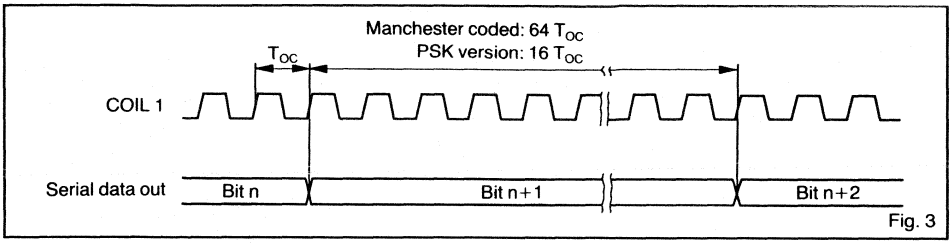


Fig. 3

Manchester Coded Version

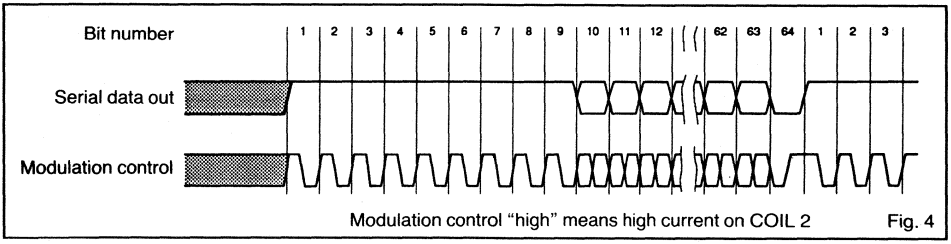


Fig. 4

PSK Version

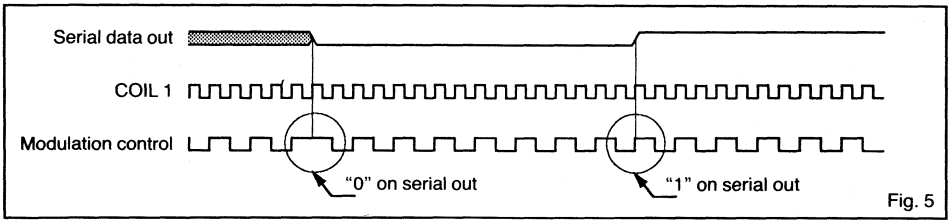


Fig. 5

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Block Diagram

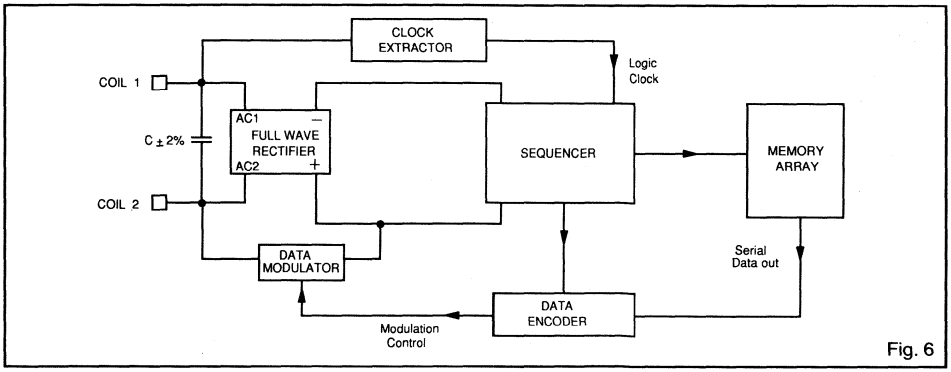

Fig. 6

Functional Description

Full Wave Rectifier

The AC input induced in the external coil by an incident magnetic field is rectified by a Graetz bridge.

Memory Array

The H 4003 contains 64 bits divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0 - P9), 4 column parity bits (PC0 - PC3), 40 data bits (D00 - D93), and 1 stop bit set to logic 0.

1 1 1 1 1 1 1 1 1		- 9 bits header
8 version bits or customer ID	D00 D01 D02 D03	P0 - 4 data bits and associated even row parity bit
	D10 D11 D12 D13	P1
	D20 D21 D22 D23	P2
	D30 D31 D32 D33	P3
32 data bits allowing 4 billion of combinations	D40 D41 D42 D43	P4
	D50 D51 D52 D53	P5
	D60 D61 D62 D63	P6
	D70 D71 D72 D73	P7
	D80 D81 D82 D83	P8
	D90 D91 D92 D93	P9
	PC0 PC1 PC2 PC3	0 - 4 column even parity bits, NO row parity bit (header not taken in account)

The header is composed by the 9 first bits which are mask programmed to 1 1 1 1 1 1 1 1 1. Due to the data and parity organisation, this sequence cannot be reproduced in the data string. The header is followed by 10 groups of 4 data bits and 1 even row parity bit. Then, the last group consists of 4 even column parity bits without row parity bit.

Bits D00 to D03 and bits D10 to D13 are customer specific identification. These 64 bits are outputted serially in order to control the modulator used to modify the current at one of the coil terminals. When the 64 bits data string is outputted, the output sequence is repeated continuously until power goes off.

Control Logic

Two mask programmed versions of logic are available. The first one will modulate the amplitude of the magnetic field with a bit rate correspondinng to 64 periods of the field frequency (Manchester coding). The second version is using half of the field frequency to transmit data by shifting the signal phase (PSK coding).

One of the coil terminals (COIL 1 in Fig. 6) is used to generate the clock signal for the logic. The output of the clock extractor drives a sequencer providing all necessary signals to address the memory array, and serially output the data.

PSK Version

The serial data output of the memory array connects the modulation control to the output or inverted output of a flip-flop which input is the signal from the clock extractor. When a logic 0 is output, the modulation control signal is changed to the other output of the flip-flop causing a phase shift, and when a logic 1 is output, the modulation control signal remains on the same flip-flop output.

Data Modulator

The data modulator is controlled by the signal modulation control (see Fig. 4 and 5) in order to induce a high current on COIL 2 terminal when this signal is at logic 0. This will affect the magnetic field according to the data stored in the memory array.

Resonance Capacitor

An on chip fuse trimmed ± 2% capacitor is provided to obtain a resonant LC circuit together with the externally connected coil. The integrated capacitor is set to 170 pF for the low speed version (LS) and 120 pF for the high speed version (HS), and optional metal mask programmed values can be provided upon request.

Package and Ordering Information

Dimensions of Packages

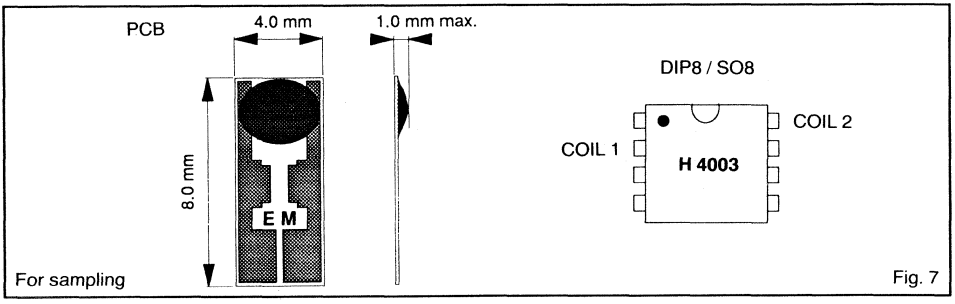

Fig. 7

Ordering Information

The H 4003 is available in chip form.
Others on request.

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ISO - Contactless Chipcard 125 kHz

Features

- Material: mix PUR / bright PVC on both sides
- Dimensions according to ISO norm:
  85.60 ± 0.12 x 53.98 ± 0.05 x 0.76 ± 0.08 mm
- Colour: white
- Physical characteristics:
  - Bending and torsion properties according to ISO norm 7816-1
  - Temperature stability: −35 to +50°C
- Electronic characteristics:
  EM H 4002, 64 bits Read Only integrated circuit
  - Manchester code
  - Coil diameter 45 mm: inductivity: 34 mH ± 3%
- Resonance frequency: 125 kHz ± 8%
- Typical reading distance: 0 to 300 mm depending on reader performance and coil characteristics

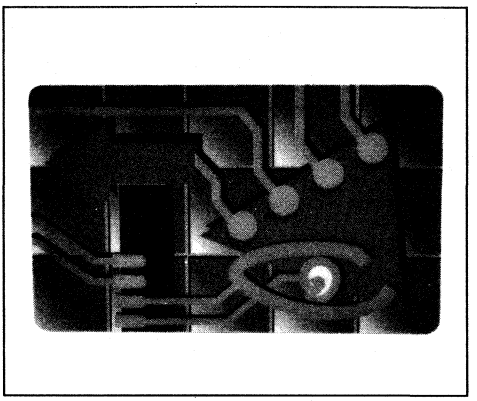
Description

This contactless chipcard is an application of the H 4002 EM device. It contains a code, which can be identified by specially adapted readers. Characteristics of the H 4002 device are given in a separate data sheet. Both sides are bright white PVC.

Applications

- Access control (control of restricted area, time management, etc.)
- Identification systems (driver's license, identity card, luggage, etc.)

ISO Card



Options

- Both sides of the card can be printed according to customer's wishes (for quantities larger than 20k pieces)
- Resonance frequency is adjusted with a standard tolerance of ± 8%. On request, by using H 4003 EM device, this tolerance can be adjusted to ± 3%
- Magnetic strip (high coercitivity 4000 Oe) available on request
- PSK code

10

Ordering Information

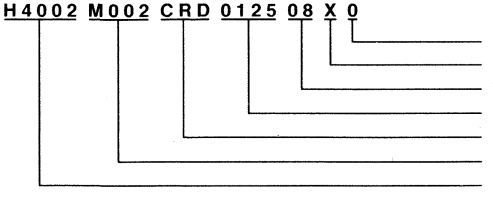


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Table of Contents

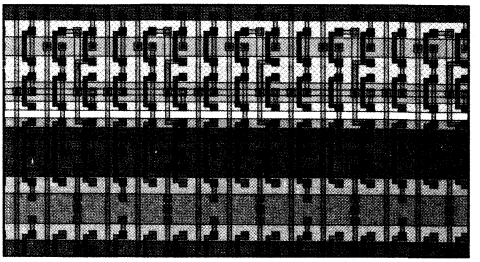
EMS V8300 / V8400

EMS Mixed-Mode Arrays

Features

- Available in seven sizes from 190 to 6,800 gates
- Mixed analog-digital and digital families
- 2 μ double-metal CMOS technology
- Operating supply voltage from 1 to 6 V
- Low power dissipation
- Worst-case gate delay of 1.6 ns at C = 0.16 pF, 4.5 V, 85°C
- Temperature compensated voltage reference
- Low power crystal oscillator
- Fast turnaround time
- Low development cost

Array Structure



Description

EMS V8300 Series is a family of transistor arrays for analog/digital applications, with limited capability in the analog domain. Its internal organization is based on a "Sea-of-Gates" architecture, offering a high degree of design flexbility and performance. This series is especially suitable for low-voltage low-power digital applications. It is aimed to cost-effectively meet the digital and mixed-mode circuit requirements of up to 6,000 gates complexity.

EMS V8400 Series is a family of arrays designed to meet mixed analog-digital circuit requirements. In addition to their "Sea-of-Gates" core, a dedicated analog array field is added, consisting of passive elements such as resistors, capacitors, lateral pnp's and long-channel transistors. A fully integrated, low-power amplitude-regulated crystal oscillator and a temperature compensated band-gap voltage reference are available. Due to its specific architecture, the EMS V8400 Series offers an excellent performance in mixed mode applications.

Product Summary

EMS V8300 Series

Device	Gate Complexity	Pads	Q-Osc.[2]
V8306	300	24	
V8309	800	36	
V8312	1300	48	
V8316	2500	64	●
V8320	4000	80	●
V8323	5200	92	●
V8326	6800	104	●

Table 1

EMS V8400 Series

Device	Gate complexity	Pads	R [x 20 kΩ]	C [x 4.6 pF]	Lat. pnp	Long-pmos	Long-nmos	V_{ref}[1]	Q-Osc.[2]
V8406	190	24	84	7	14	4	3		
V8409	600	36	84	7	14	4	3		●
V8412	1000	48	72	6	12	3	3	●	●
V8416	2200	64	132	11	22	6	5	●	●
V8420	3400	80	192	16	32	8	8	●	●
V8423	4700	92	240	20	40	10	10	●	●
V8426	6300	104	276	23	46	12	11	●	●

● Available on base

Table 2

1) Temperature compensated band-gap voltage reference: $\triangle Vo/\triangle T < 100$ ppm/°C, ± 3%

2) Low power amplitude regulated crystal oscillator: I_{DD} dynamic < 1 μA, at T = 25°C, f = 32 kHz

Array Organization

Base Elements	W/L [μm]	Min.	Typ.	Max.	Unit
Core Transistors					
PMOS Core	23/2				
NMOS Core	8/2				
PMOS Long	5/411				
NMOS Long	5/411				
Periphery Transistors					
PMOS Buffer (x 17)	62.5/2				
NMOS Buffer (x 17)	44/2				
Capacitors					
PMOS Core-Cap (½)*	44.5/60	2.1	2.2	2.3	pF
PMOS Perif-Cap L	140/140	33	34	36	pF
PMOS Perif-Cap S	298/140	15	16	17	pF
Resistors					
R n-well		16.1	21.8	24.5	kΩ
R p-poly		470	620	770	Ω
R n-poly		280	370	460	Ω
Lateral pnp's					
Beta (V_{BE} = 0.5 V)			1600		
(V_{BE} = 0.7 V)			330		
(V_{BE} = 1.0 V)			43		
I_S		0.4	0.7	1.0	fA
V_A		3		8	V

* Core capacitor is split into two halves with one terminal in common.

Table 3

Design Flow

A typical design interface between the customer and EM can be in a form of hierarchically described schematic using elements from our cell library, or in a form of a netlist. The following netlists are currently supported by EM: EDIF, HILO, VHDL, VLSI.

Logic verification is performed by using a simulator tool, with test vectors for the circuit supplied by the customer. When the design is verified, the design information is reviewed with EM prior to the initial approval.

The placement and routing process is performed by EM engineers. Final delay values are recalculated based on the actual interconnect. Based on these final values, a post-simulation is performed to verify the circuit performance. Upon customer's and EM's final signoff approval, the design is released for prototype fabrication, assembly and test.

Prototypes encapsulated in CERDIP package are delivered to the customer. Upon satisfactory prototype evaluation, EM requires the customer to submit a written approval of the prototypes.

Absolute Maximum Ratings

Parameter	Symbol	Conditions
DC Supply Voltage	V_{DD}	−0.5 to +7.0V
DC Input Voltage	V_I	V_{SS} −0.5 to V_{DD} +0.5V
DC Input Current	I_I	±30mA
Lead Soldering Temp.	T_L	+250°C x 10 s

Table 4

Stresses beyond these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may effect device reliability or cause malfunction.

Recommended Operating Conditions

Parameter	Symbol	Value	Units
Operating Junction Temperature:			
Military	T_J	−55 to +125	°C
Industrial	T_J	−40 to + 85	°C
Commercial	T_J	0 to + 70	°C
Storage Temperature	T_{STO}	−65 to +150	°C

Table 5

DC Electrical Characteristics

Input / Output Cells

T_A = 25°C, V_{SS} = 0V, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power supply	V_{DD}		4.5		5.5	V
Low Level Input Voltage						
CMOS Input	V_{IL}	Guaranteed input	−0.5		0.3 x V_{DD}	V
TTL Input	V_{iL}	low voltage	−0.5		0.8	V
High Level Input Voltage						
CMOS Input	V_{IH}	Guaranteed input	0.7 x V_{DD}		V_{DD}	V
TTL Input	V_{IH}	high voltage	2.0		V_{DD}	V
Low Level Output Voltage	V_{OL}					
pc7x01 and pc7c51		I_{OL} = 4 mA			0.4	V
pc7x02 and pc7c52		I_{OL} = 8 mA			0.4	V
pc7x03 and pc7c53		I_{OL} = 32 mA			0.4	V
High Level Output Voltage	V_{OH}					
pc7x01 and pc7c52		I_{OL} = − 4 mA	2.4			V
pc7x02 and pc7c52		I_{OL} = − 8 mA	2.4			V
pc7x03 and pc7c53		I_{OL} = −32 mA	2.4			V
Input Capacitance	C_{IN}	Excluding package			5	pF
Output Capacitance	C_{OUT}	Excluding package			5	pF

Table 6

Voltage Reference (VREFEMS2, typical values)

Parameter	Symbol	Test Conditions	Value	Tolerance	Units
Reference Output Voltage	V_{REF}	V_{DD} = 3 V, T = 25°C	1.350	± 0.040	V
Commercial Range Temperature Coefficient	T_C	0°C...+ 70°C	15	± 60	ppm/°C
Industrial Range Temperature Coefficient	T_C	−40°C...+ 85°C	15	± 70	ppm/°C
Military Range Temperature Coefficient	T_C	−55°C...+125°C	15	± 70	ppm/°C
Reference Voltage Stability	S_{VREF}	V_{DD} = 2.2...9 V	−1		mV/V
Minimum Supply Voltage	V_{DDmin}	T = −55...+125°C	2.2		V
Maximum Supply Voltage	V_{DDmax}	T = −55...+125°C	9		V
Current Consumption	I_{DD}	V_{DD} = 3 V, T = 25°C	3.0	± 0.3	μA

Table 7

Low-Power Quartz Oscillator (typical values)

Parameter	Value	Unit
Operating Supply Voltage	1.2 - 3.5	V
Frequency Stability	5	ppm/V
Static Current Consumption	< 100	nA
Dynamic Current Consumption at 32 kHz	< 500	nA
Power-down Mode		

Table 8

EMS Digital Library

Cell List

Function	No. of Types
Logic Gates	30
Internal Buffers	6
Latches	10
Flip-Flops	16
Input Buffers	4
Output Buffers	9

Table 9

AC Electrical Characteristics (Cell Examples)

V_{DD} = +4.5 V, T_J = +85°C, worst-case process, capacitive load = 2 std loads = 0.16 pF

Cell Name	Parameter	T_{PHL}	T_{PLH}	Other	Unit
IN01D1	Standard Inverter	1.9	1.5		ns
ND02D1	2-Input NAND	3.2	1.6		ns
NR02D1	2-Input NOR	2.2	3.1		ns
DFNTNN	Flip-Flop				
	CP → Q	11.5	9.5		ns
	t_{HOLD}			2.0	ns
	t_{SETUP}			0.5	ns
PC7C02	CMOS 8 mA Output Buffer				
	Capacitive Load = 10 pF	2.5	7.7		ns
	Capacitive Load = 50 pF	9.3	30.6		ns

Table 10

EMS Analog Library

Cell Examples

Description	Current Consumption at V_{DD} = 3 V (typ. values)	Supply Voltage Range		
		Min.	Typ.	Max.
Oscillators				
Low Power 32 kHz Quartz	< 0.5 µA dynamic	1.2 V		3.5 V
Low Power 4 MHz Quartz	100 µA dynamic	2.0 V		5.5 V
RC oscillator 10 kHz (ext. R)	< 3 µA dynamic	2.2 V		5.5 V
Relaxation RC oscillator 1 kHz ... 3 MHz	3 µA - 570 µA dynamic	2.2 V		5.5 V
Op-Amps, Comparators				
N-Type, Internally Compensated / Output Buffer	20 µA static	2.2 V		5.5 V
P-Type, Internally Compensated / Output Buffer	20 µA static	2.2 V		5.5 V
N-Type, Folded Cascode	240 µA static	2.2 V		5.5 V
Class AB, Rail-to-Rail Output Swing	20 µA static	2.4 V		5.5 V
Pulse Amplifier with AGC, 72 dB Dynamic Range	130 µA static	2.2 V		5.5 V
Sense Amplifier (Programmable I / V Converter)	1 µA static	2.2 V		5.5 V
Converters				
8-Bit Weighted Current DAC	60 µA static	2.0 V		5.5 V
8-Bit Successive Approximation ADC	70 µA static	2.5 V		5.5 V
Analog Multipliers				
4-Quadrant Voltage Multiplier	100 µA static	2.2 V		5.5 V
Miscellanous				
LCD Driver (amplitude-controlled output buffer)	0.5 µA static	2.2 V		5.5V

Table 11

Packaging Information

Device	DIL 8	DIL 14	DIL 16	DIL 18	DIL 20	DIL 22	DIL 22	DIL 24	DIL 24	DIL 28	DIL 32	DIL 40	DIL 48	DIL 64
	Package width [mils]													
	300	300	300	300	300	300	400	300	600	400/600	400/600	600	600	900
V8306 / V8406	●	●	●	●	●	●	●	●	●	●	●	●	●	●
V8309 / V8409	●	●	●	●	●	●	●	●	●	●	●	●	●	●
V8312 / V8412	●	●	●	●	●	●	●	●	●	●	●	●	●	●
V8316 / V8416			○			●	●	●	●	●	●	●	●	●
V8320 / V8420							●	●	●	●	●	●	●	●
V8323 / V8423							●		●	●	●	●	●	●
V8326 / V8426							●		●	●	●	●	●	●

Device	SO 8	SO 14	SO 16	SO 16	SO 18	SO 20	SO 24	SO 28	SO 32	PLCC 20
	Package width [mils]									
	150	150	150	300	300	300	300	300	300	square
V8306 / V8406	●	●	●	●	●	●	●	●	●	●
V8309 / V8409				●	●	●	●	●	●	●
V8312 / V8412				●	●	●	●	●	●	●
V8316 / V8416				●	●	●	●	●	●	●
V8320 / V8420				●	●	●	●	○	○	●
V8323 / V8423								○		●
V8326 / V8426										

Device	PLCC 28	PLCC 32	PLCC 44	PLCC 52	PLCC 68	PLCC 84	QFP 44	QFP 52	QFP 64	QFP 80	QFP 100	QFP 128
	square	rectang.	square	square	square	square						
V83xx / V84xx	●	●	●	●	●	●	●	●	●	●	●	●

○ On request. All other packages on request. Table 12

Quality and Reliability

Quality

The following aspects guarantee products of high quality:

- Simple design procedure
- Circuits are designed to satisfy at least 1000 V ESD, according to MIL-STD-883D, Method 3015
- Manufacturing under SPC (Statistical Process Control)
- Wafers 100% assessed for process parameters
- 100% wafer probe testing
- 100% final test on packaged devices

Reliability

- Representative products of the technology are assessed for reliability on a regular basis
- Design thoroughly proved by in-depth testing

Supplementary reliability assessment may be performed on request:

- Full screening to MIL-STD-883D, Method 5004 Class B
- Full qualification testing on specific product(s) may include: latch-up sensitivity, ESD evaluation, temperature dependence, parameter stability (e.g. high temperature bake), electrical life tests, temperature humidity tests for plastic packages, temperature cycling, mechanical tests.

Handling Procedures

EMS circuits are built with protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are maintained within the supply voltage range.

EM Products and Services

ASIC

- Low-power analog and digital cell-design with DC supply voltage between 1.2 and 12 V in different ranges
- Triple technology design:
  - analog
  - digital
  - E^2PROM
- Walk-in facility: Design your ICs yourself!
- Mixed-Mode Arrays

CID

- Contactless Identification Devices, Read-Only and Read-Write
- Development and production of Contactless Identification Systems (CID) and smart cards

MICRO-CONTROLLER

- 4 bit, low power, low voltage
- Standard and custom versions

FOUNDRY

- 3, 2 and 1 μm HCMOS

BUMPING

- Prepare your wafer for TAB and Flip Chip with our advanced bumping process

TAB

- Tape Automated Bonding - the smart package with high reliability and minimum package size
- Film layout
- Assembly (ILB, OLB) including testing

ADVANCED ASSEMBLY

- Development and production of modules using TAB, COB, conductive gluing , SMD

LCDs

- High spec. applications
- Prototype and small to medium production series
- Twisted Nematic, Super Twisted Nematic, Heilmeier and White Taylor

Ordering Information

Ordering No. [2]	Package	Version	Temperature Range
Display Driver			
M 6003 nn 40P	DIP40	01	−40 to +85°C
M 6003 nn 44Q	PLCC44	01	−40 to +85°C
M 6004 nn 52Q	PLCC52	02	−40 to +85°C
V 6118 n 52F	QFP52	2, 4, 8	−40 to +85°C
V 6118 n TAB	TAB	2, 4, 8	−40 to +85°C
Real Time Clock			
M 3002 16P	DIP16		−40 to +85°C
M 3002 16S	SO16		−40 to +85°C
M 3003 16P	DIP16		−40 to +85°C
M 3003 16S	SO16		−40 to +85°C
V 3021 8P	DIP8		−40 to +85°C
V 3021 8S	SO8		−40 to +85°C
V 3022 18P	DIP18		−40 to +85°C
V 3022 28S	SO28		−40 to +85°C
V 3023 18P	DIP18		−40 to +85°C
V 3023 28S	SO28		−40 to +85°C
Watch			
H 1063	CHIP		−20 to +70°C
H 1137	CHIP		−10 to +60°C
H 1344	CHIP		−20 to +70°C
H 1344	DIP8		−20 to +70°C
H 5050 nn SO28	SO28	1H, 2H, 4H	−40 to +85°C
Watchdog			
H 6006 nn 8P	DIP8	A2, A3, B1, B2, B3	−40 to +85°C
H 6006 nn 8S	SO8	A2, A3, B1, B2, B3	−40 to +85°C
H 6060 nn 8P	DIP8	14, 15, 16	−40 to +85°C
H 6060 nn 8S	SO8	14, 15, 16	−40 to +85°C
H 6061 nn 8P	DIP8	25	−40 to +85°C
H 6061 nn 8S	SO8	25	−40 to +85°C
V 6130 8P	DIP8		−40 to +70°C
V 6130 8S	SO8		−40 to +70°C
V 6133 14P	DIP14		−40 to +70°C
V 6133 14S	SO14		−40 to +70°C
V 6150 nn 8P	DIP8	01	−40 to +85°C
V 6150 nn 8S	SO8	01	−40 to +85°C
V 6170 8P	DIP8		−40 to +70°C
V 6170 8S	SO8		−40 to +70°C
V 6173 14P	DIP14		−40 to +70°C
V 6173 14S	SO14		−40 to +70°C

Ordering No. [2]	Package	Version	Temperature Range
Smart Reset			
H 6052 n TO-92	TO-92	1, 2	−40 to +85°C
H 6052 n SOT-223	SOT-223	1, 2	−40 to +85°C
V 6300 n TO-92	TO-92	I, O, P, (n[1])	−40 to +85°C
V 6300 n SOT-223	SOT-223	I, O, P, (n[1])	−40 to +85°C
V 6310 n TO-92	TO-92	O, (n[1])	−40 to +85°C
V 6310 n SOT-223	SOT-223	O, (n[1])	−40 to +85°C
V 6320 n TO-92	TO-92	P, R, (n[1])	−40 to +85°C
V 6330 n TO-92	TO-92	P, (n[1])	−40 to +85°C
Regulator and Surveillance Functions			
A 6130 8P	DIP8		−40 to +70°C
A 6130 8S	SO8		−40 to +70°C
A 6133 14P	DIP14		−40 to +70°C
A 6133 14S	SO14		−40 to +70°C
V 6139 16P	DIP16		−40 to +85°C
A 6139 16S	SO16		−40 to +85°C
A 6150 nn 8P	DIP8	A1	−40 to +85°C
A 6150 nn 8S	SO8	A1	−40 to +85°C
V 6170 8P	DIP8		−40 to +70°C
V 6170 8S	SO8		−40 to +70°C
A 6173 14P	DIP14		−40 to +70°C
A 6173 14S	SO14		−40 to +70°C
A 6300 nn 8P	DIP8	AP, AQ, (nn[1])	−40 to +85°C
A 6300 nn 8S	SO8	AP, AQ, (nn[1])	−40 to +85°C
Interface			
V 6910 nn 16P	DIP16	10[1], 20[1]	−40 to +85°C
V 6910 nn 16S	SO16	10[1], 20[1]	−40 to +85°C
V 6912 nn 8P	DIP8	10[1], 20[1]	−40 to +85°C
V 6912 nn 8S	SO8	10[1], 20[1]	−40 to +85°C
V 6915 nn 16P	DIP16	10[1], 20[1]	−40 to +85°C
V 6915 nn 16S	SO16	10[1], 20[1]	−40 to +85°C
V 6917 nn 8P	DIP8	10[1], 20[1]	−40 to +85°C
V 6917 nn 8S	SO8	10[1], 20[1]	−40 to +85°C
Contactless Identification Devices (CID)			
Please inquire before ordering			

[1] Non-stock items
[2] n or nn stands for the version

For many products, additional electrical and packaged versions are available on request. Minimum order 20k pieces.

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A Company of SMH

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	Great-Britain and Ireland	Pronto Electronic Systems Ltd., Gants Hill, Ilford, Essex IG2 6LR, Tel. 081 - 554 5700, Fax 081 - 518 3222
	Israel	Trust Electronics Ltd., 56500 Savion, Tel. 035 34 50 26, Fax 035 35 14 68
	Italy	Skylab S.r.l., 20125 Milano, Tel. 02 - 667 10 822, Fax 02 - 667 10 695
	Japan	Nippon Precision Device Corp., Tokyo 162, Tel. 03 - 3260 1411, Fax 03 - 3260 7100
	Korea	Shinhwa Corporation, Seoul, Tel. 02 - 554 64 31, Fax 02 - 554 76 49
	Norway	Heko-Elektronikk & Data A/S, 1472 Fjellhamar, Tel. 06 - 790 5244, Fax 06 - 790 0114
	Portugal	Amitron Arrow Electronica Lda, 1300 Lisboa, Tel. 01 - 3621 283/4, Fax 01 - 3637 655
	Spain	Amitron Arrow S.A., 28037 Madrid, Tel. 91 - 304 30 40, Fax 91 - 327 24 72
	Sweden	NC NordComp Sweden AB, 17104 Solna, Tel. 08 - 764 67 10, Fax 08 - 764 47 30
	Switzerland	Eurodis Electronic AG, 8105 Regensdorf, Tel. 01 - 843 31 11, Fax 01 - 843 34 75
	Taiwan	Solomon Technology Corp., Taipei, Tel. 02 - 788 89 89, Fax 02 - 788 80 29
	Turkey	Fudem Trading SA, CH - 1207 Geneva, Tel. 0041 22 - 700 24 60, Fax 0041 22 - 700 24 87
US Representatives	**AL, GA, DE, FL, MD, NC, SC, VA, WV, TN**	Glen White Associates, Tel. 804 385 6110, Fax 804 385 7196
	IL, IA, MI, WI	Greenslade Sales, Tel. 708 593 3450, Fax 708 593 3468
	IN, OH, KY	Phoenix Marketing, Tel. 317 577 4112, Fax 317 576 1155
	NY, NJ, PA	WD Sales, Tel. 914 779 8738, Fax 914 779 8840
	MA, ME, CT, NH, VT, RI	Conti-Younger Associates, Tel. 617 273 1582, Fax 617 270 0310
	MN, ND, SD	Grayden and Flemmer, Tel. 612 941 1120, Fax 612 941 2061
	TX, LA, OK, AR	RMS Associates, Tel. 512 502 0899, Fax 512 502 0083
US Distributor	**USA**	OmniPro Electronics, Tel. 800 926 8926, Fax 214 723 8743

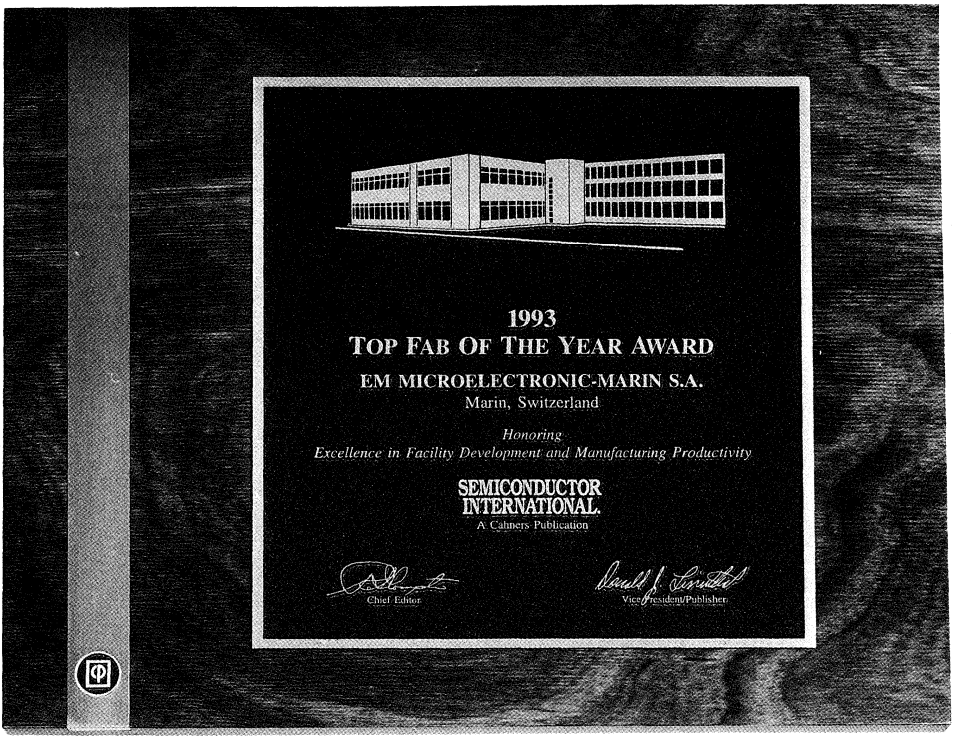
Notes

A Most Advanced Wafer Fab

The 6" wafer fab of EM Microelectronic-Marin SA is one of the most advanced fabs employing the revolutionary SMIF cleanroom concept, where only robots are working in a class 1 environment while men are operating in a class 1000 environment.

EM received as the first wafer fab in Europe the ISO 9001 certificate .

In 1993 "Semiconductor International", the world wide leading journal of the industry, honered EM with the "TOP FAB OF THE YEAR AWARD".



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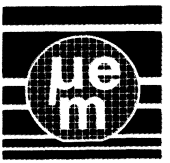

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EM MICROELECTRONIC-MARIN SA

A company of SMH – Swiss quality, ISO 9001 certified

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